TWINRELECT

TWINRELECT 1st Webinar

Bridging EU Innovation in Reliable Electronics Design

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UK Research and Innovation

TWIN-RELECT – Twinning for Excellence in Reliable Electronics

- **Why Reliable Electronics?**
  - **Critical for safety & mission-critical systems:**
    - Space, avionics, automotive, banking, medical, nuclear, manufacturing
- **Project Mission**
  - **Establish a cross-layer methodology for design of reliable Systems**
  - Elevate the University of Thessaly's capacity in reliable electronic design
    - Achieved through strategic collaborations with the partners
- **Project Timeline**
  - Start: 1 October 2024
  - End: 30 September 2027
- **Coordinated by:**
  - **University of Thessaly**
    - Circuits and Systems Lab (CAS lab)

The Partners

5 Partners – 23 Researchers

Circuits and Systems Lab research on custom-developed EDA/CAD tools focusing on reliability issues of electronics in radiation environments
9 Members

Advanced Processor Technologies group is devoting increasing attention to the development of a new generation of fault-tolerant neuromorphic computing technologies
2 Members

System Architectures Department research on modelling and analysis of fault mechanisms in digital circuits and the design of fault-tolerant circuits and systems
5 Members

Institute of Electronics and Systems, which is a joint research unit between University of Montpellier and CNRS, is specialized in sensors, devices and systems for hostile environments. Within IES, the RADIAC team is particularly focusing on reliability issues of electronics in radiation environments.
7 Members

Research Management & Administration

- **Mission:**
  - Elevate UTH's capacity at managing EU-funded research
- **Key Objectives:**
  - **Establish an Office at UTH for International Projects**
    - To support proposal development and project coordination
  - **Develop a Research Management Handbook**
    - A best-practices guide for EU project lifecycle management
  - **Implement Agile Management Tools**
    - Adopt digital tools to streamline operations
  - **Train Research & Admin Staff**
    - Organize 5 workshops and staff exchanges with top EU institutions
- **Outcome:**
  - UTH becomes more competitive in EU research calls
    - With enhanced administrative efficiency and project delivery capacity

Strategic Networking & Visibility

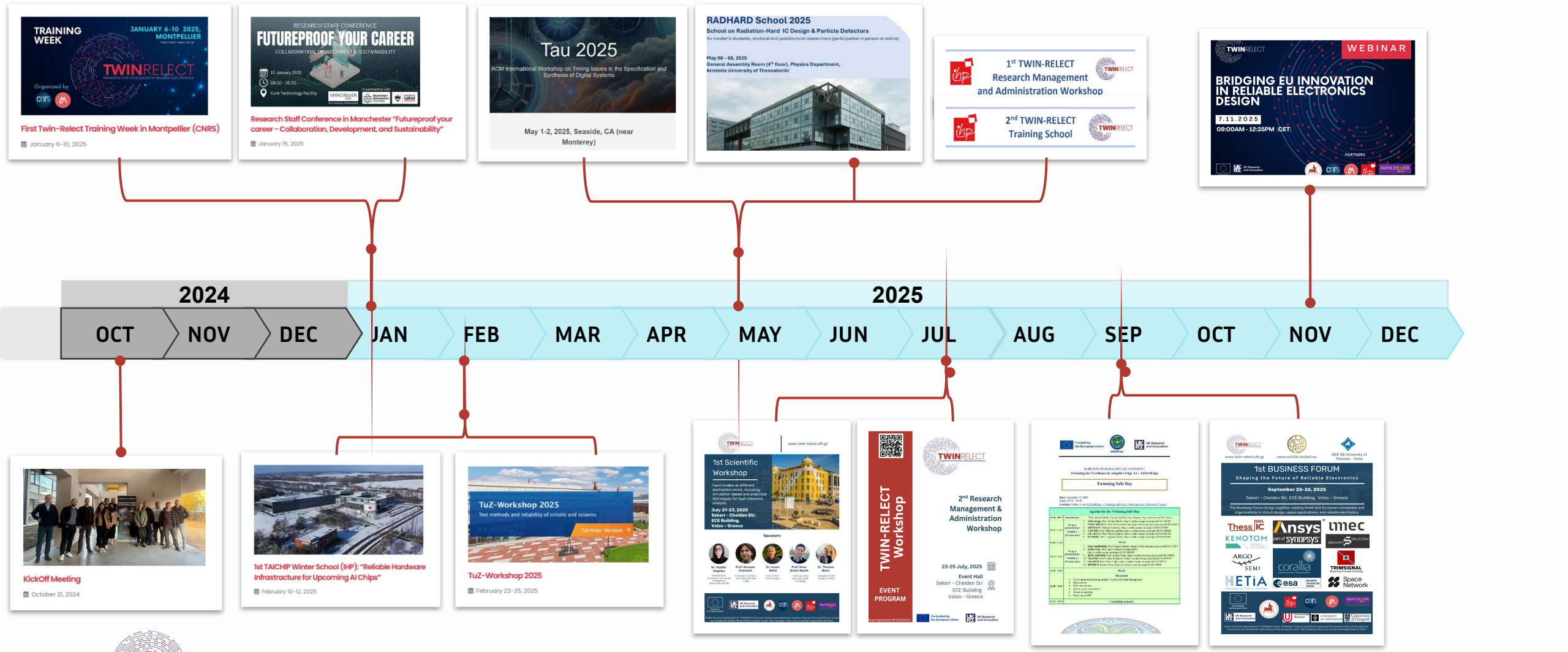
- **Mission:**
  - Strengthen UTH's research profile and international collaborations
- **Key Actions:**
  - **Host High-Impact Events**
    - Scientific Workshops
    - Business Forums
    - Special Sessions at major Conferences
    - International Symposium in Greece
  - **Build Stakeholders Networks**
    - Engage academia, industry, and policymakers across Europe
  - **Enhance Visibility**
    - Open-access publications, media outreach, project website, and social media
  - **Increase Educational Attractiveness**
    - Upgrade curricula and promote MSc/PhD co-supervision internationally

- **Outcome:**
  - UTH is positioned as a recognized hub in reliable electronics research
    - With deep integration into the EU R&I landscape.

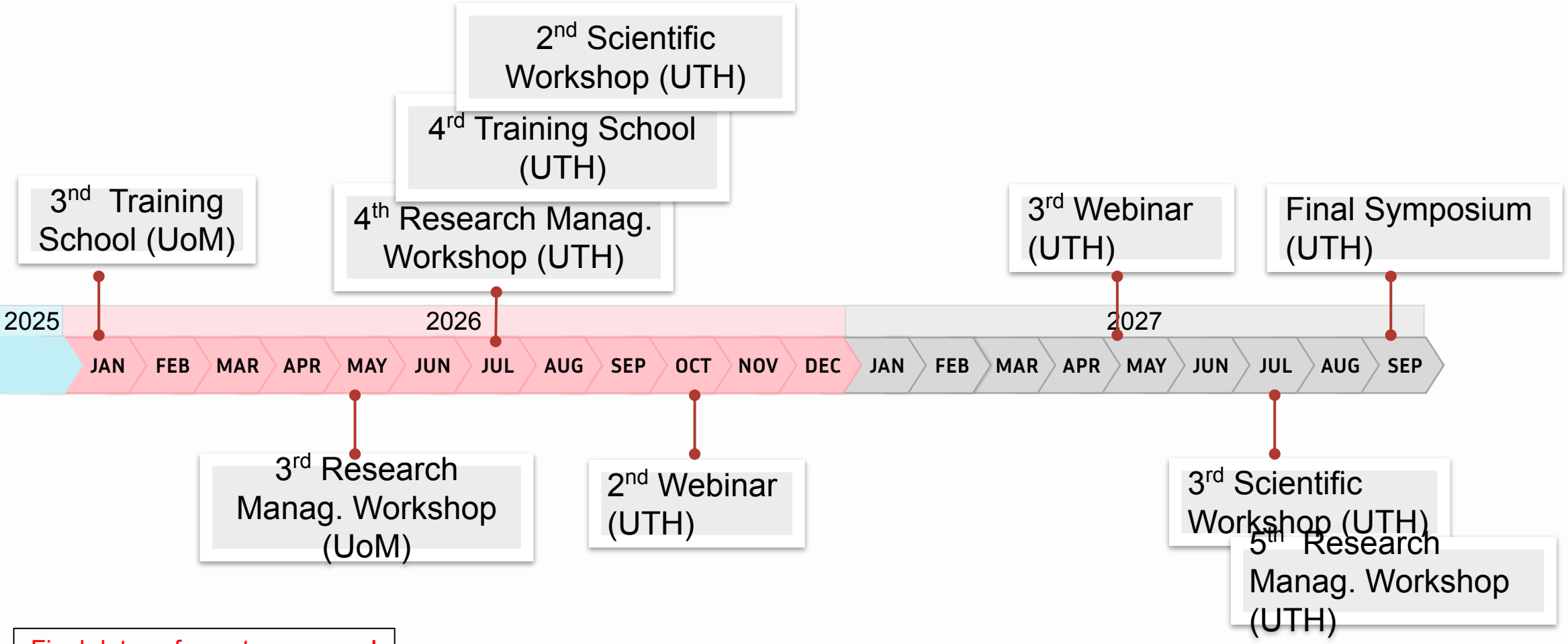
Main Activities Highlights

- **Publications:**
  - At least 12 Conference Papers
  - At least 10 Journal Publications
- **Organization of:**
  - 4 Training Schools
  - 3 Scientific Workshops
  - 5 Research Management & Administration Workshops
  - 2 Business forums
  - 3 Webinars
  - 2 Special Conference Sessions
  - Final International Symposium
- **Short-Term Visits to Partners**
  - UTH PhD students will spend up to 10 months at partner institutions
- **Short-Term Visits to UTH**
  - Experts from IHP, CNRS, and MAN will conduct short-term visits to UTH
- **Visits to Research Centers**
  - CERN, CNRS, ESA, etc.
- **Attendance at:**
  - Conferences
  - Workshops
  - Events, etc.
- **Joint Irradiation Experiments**
  - Ionizing Particle Irradiation
  - Gamma/X-ray irradiation
  - Laser irradiation
  - Accelerated aging
  - EMI

Events Roadmap



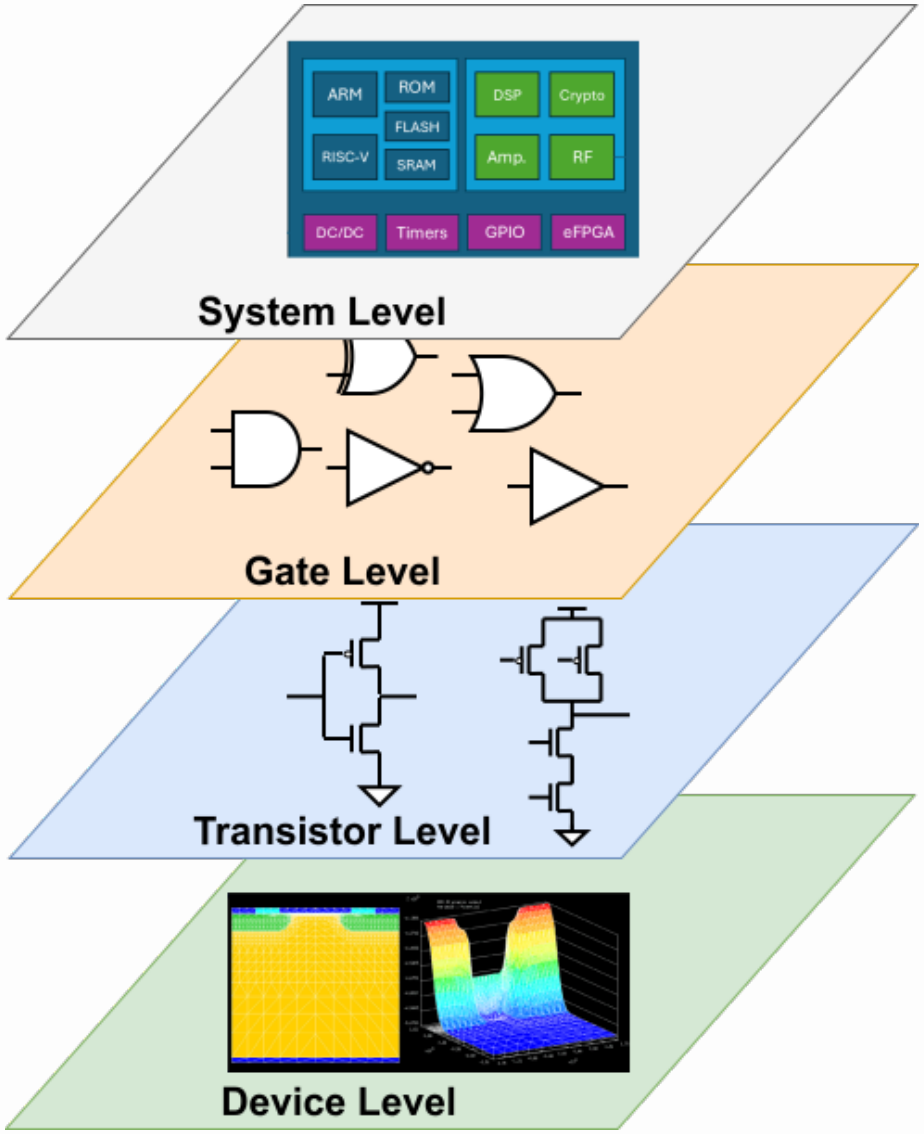
Events Roadmap



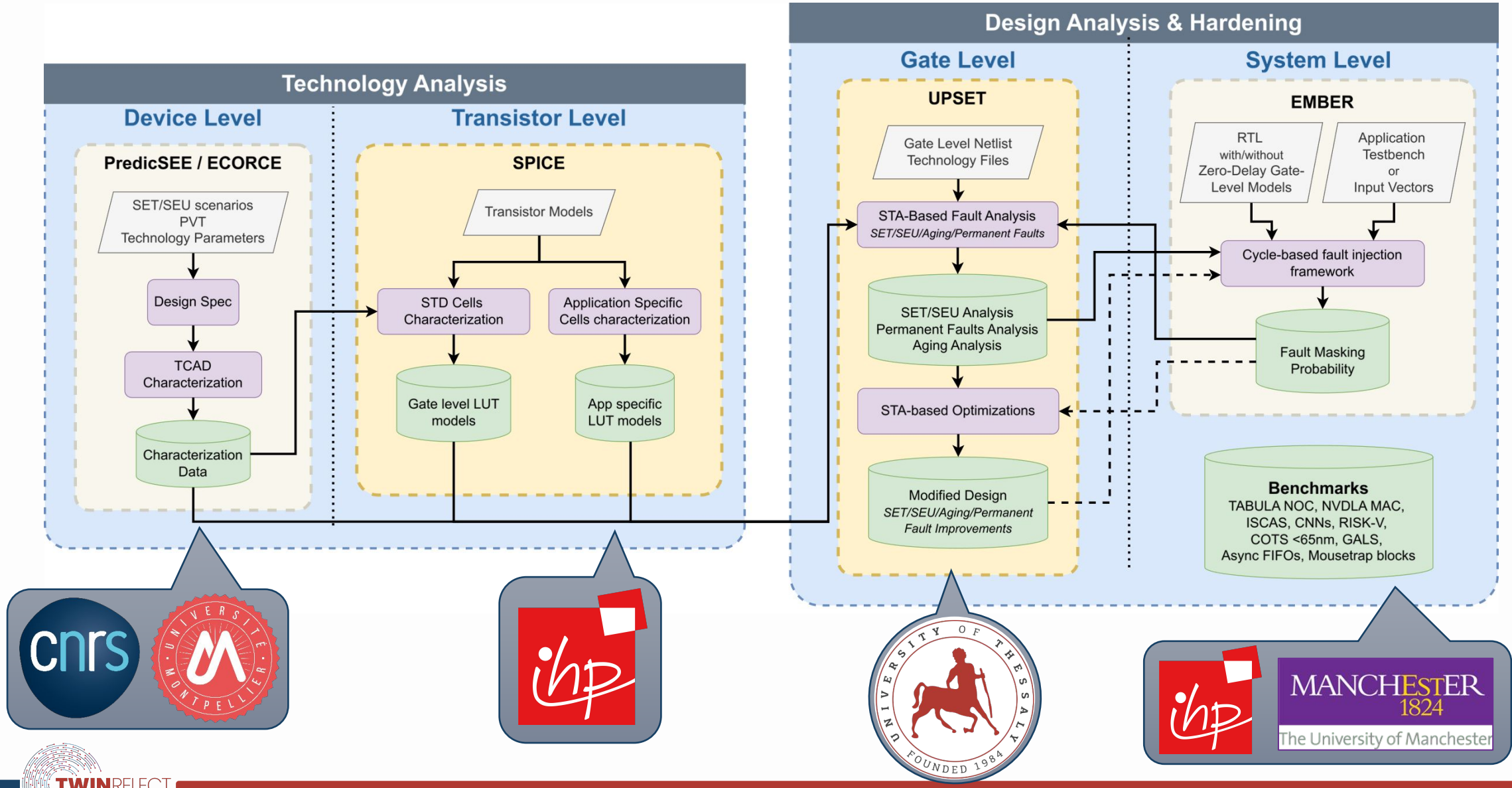
Final dates of events may vary!

Research Objectives

- **Why a cross-layer EDA Tool Flow for Reliability Analysis?**
  - Bridge the gap between fault analysis and design-for-reliability
- **Our Vision:**
  - Enable a comprehensive reliability analysis accross the entire design stack
    - By integrating fault modeling
      - **From device-level** physical simulations
      - **Up to sytem-level** fault injection
  - While incorporating **Fault-Mitigation Techniques**
    - Allowing designers to actively improve the resilience of electronic systems

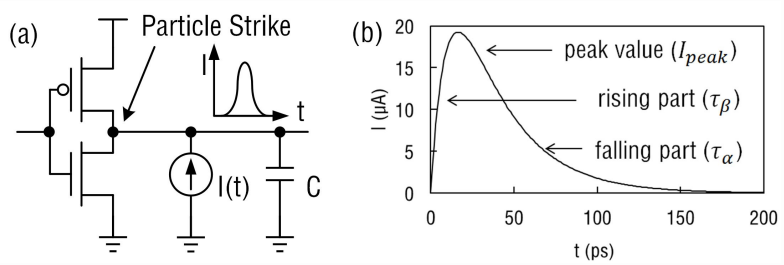


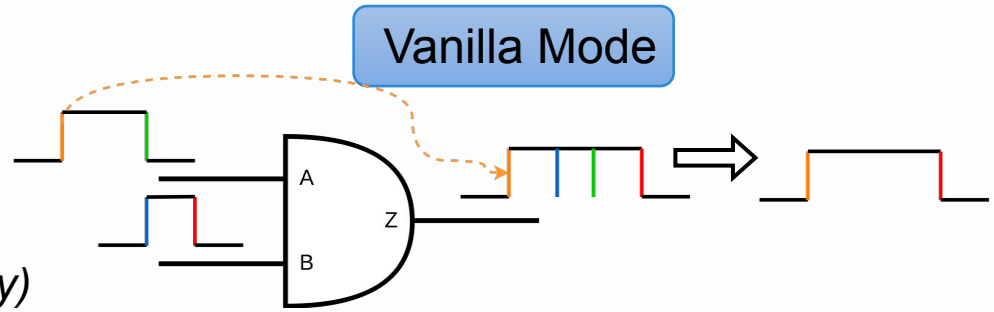
TWIN-RELECT EDA Tool Flow Diagram

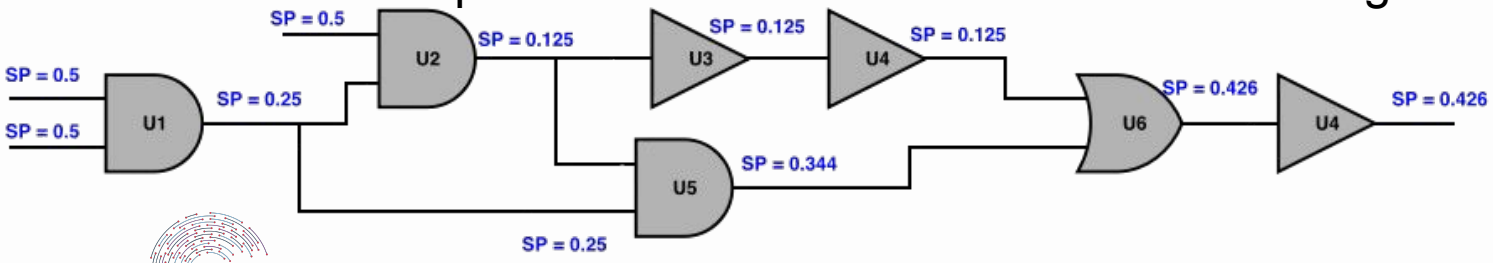


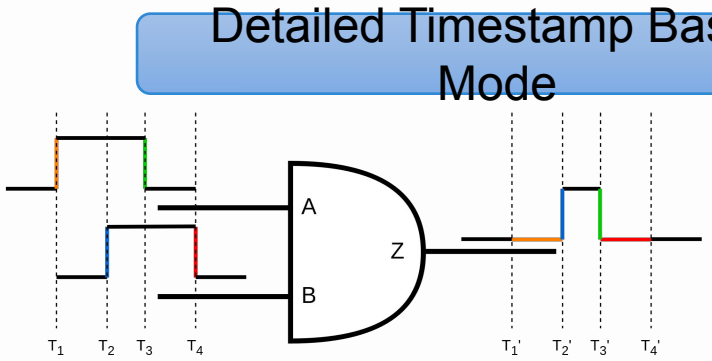
UPSET SET Analysis Framework

- **Upset is a Probabilistic STA-based SET Analysis Framework supporting:**
  - **SET Generation**
    - Double Exponential Current Source Model
  - **SET Propagation**
    - Using STA principles
      - NLDM, CCS
      - Lumped RC, Pi-Model, Detailed RC
    - Two propagation modes
      - **Vanilla mode** *(Worst case)*
      - **Detailed Timestamp Based Mode** *(Highest accuracy)*
  - **Probabilistic Analysis**
    - Use probabilities to model the state of the design





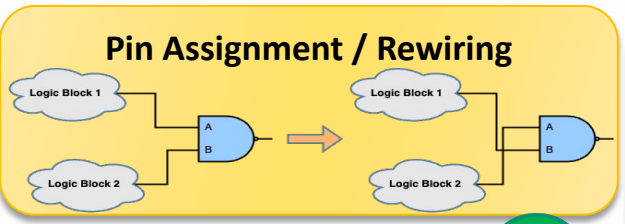


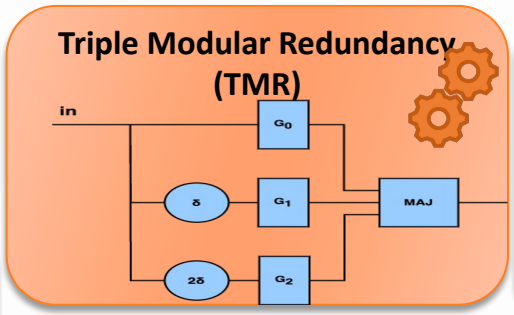


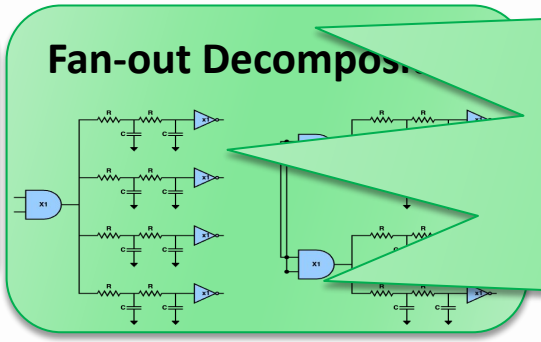
AND Truth Table		
0	0	0
0	1	0
1	0	0
1	1	1

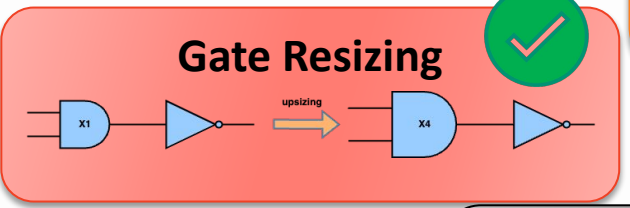
UPSET Design Hardening

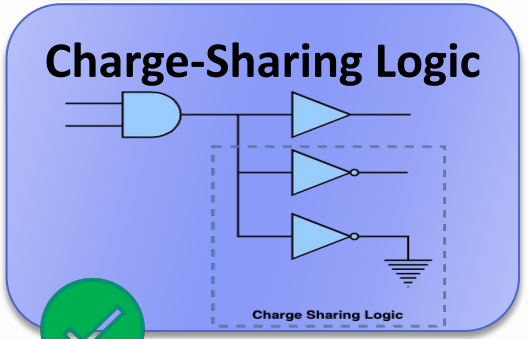
- Closed-Loop SET Optimisation - WIP
- Supports Gate-Level SET mitigation techniques
- **Goal**
  - Fast SET Optimisation
  - Minimum PPA overhead

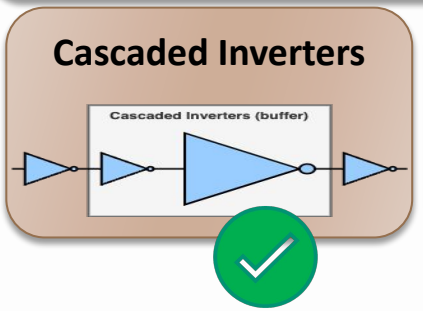


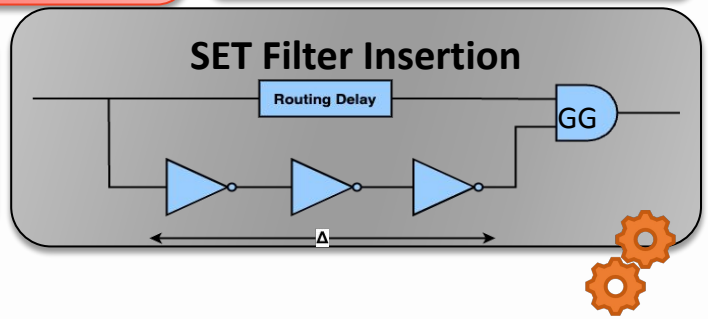


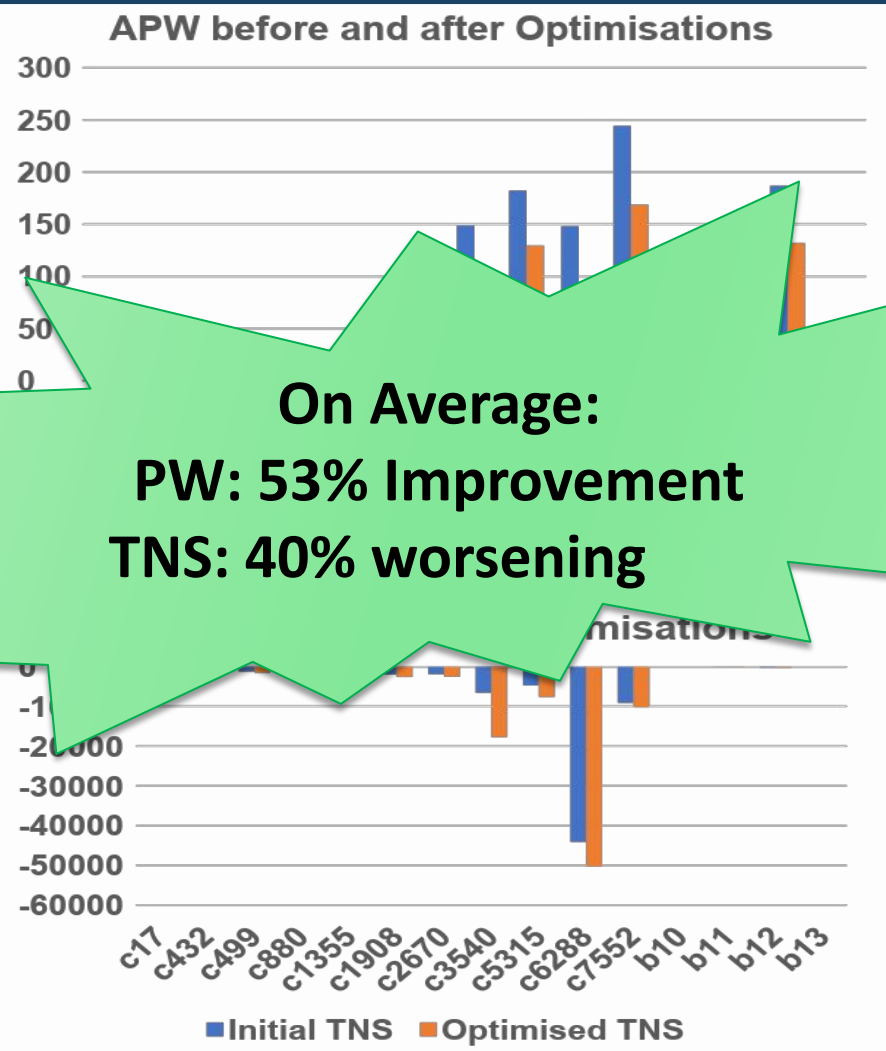








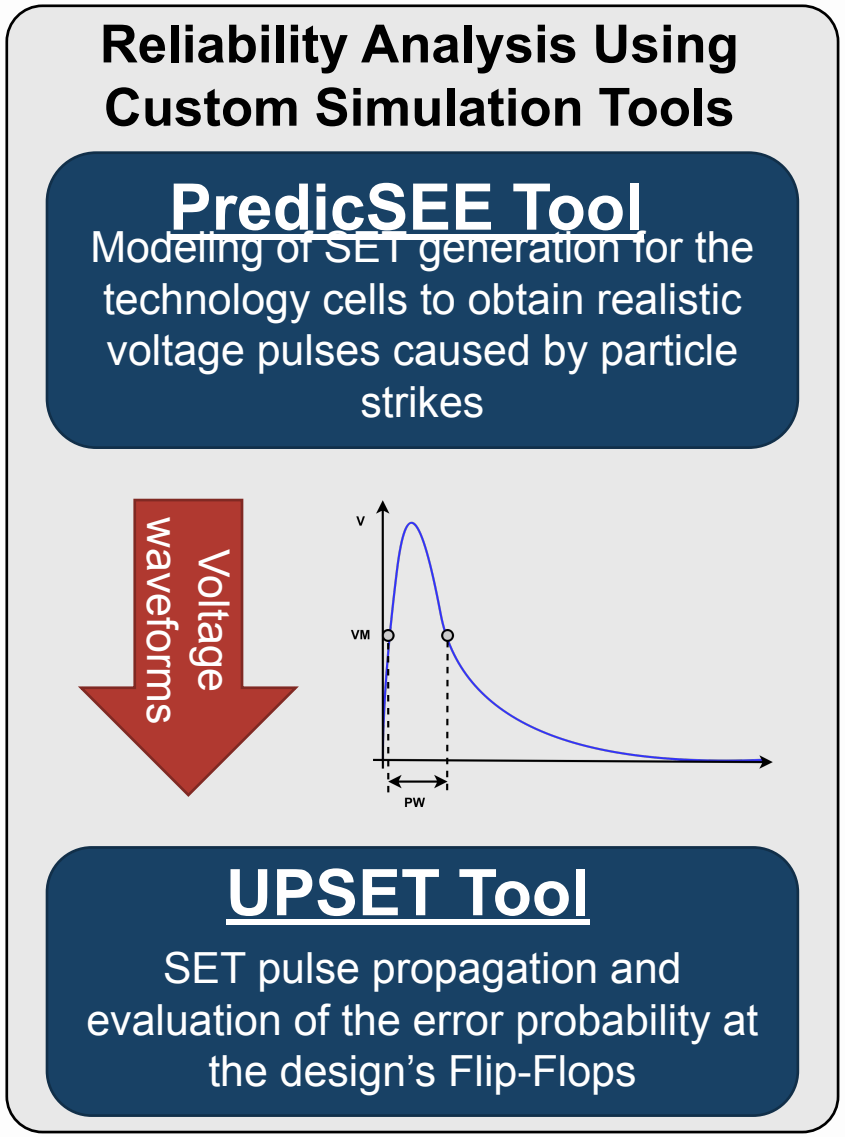




On Average:
PW: 53% Improvement
TNS: 40% worsening

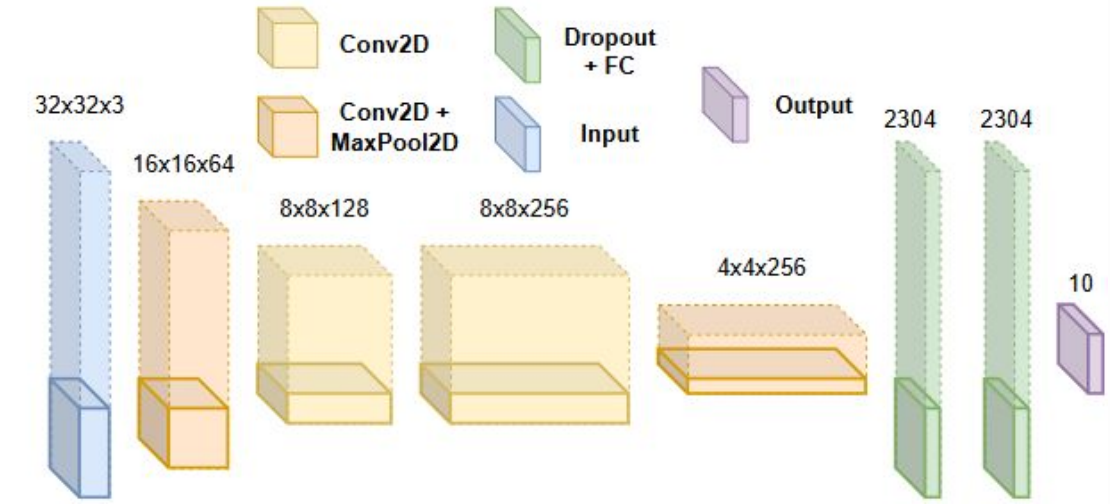
Reliability Analysis Using Custom Simulation Tools

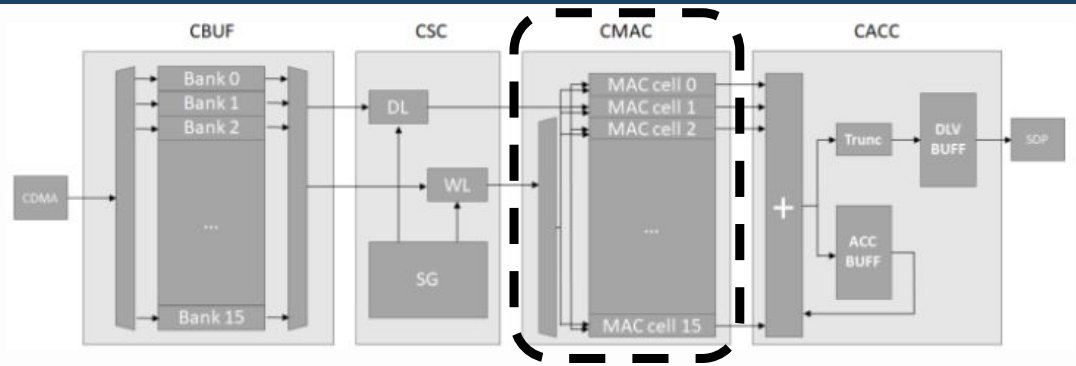
- **Combine two simulation tools to propose a more accurate analysis flow**
  - **PredicSEE**
    - For realistic SET generation modeling
  - **UPSET**
    - For fast SET propagation and SER estimation
    - Allowing to analyze large designs
- **Targeted with this flow clock networks**
  - Results showed that a SET at the clock network may have significant probability of causing errors at Flip-Flops

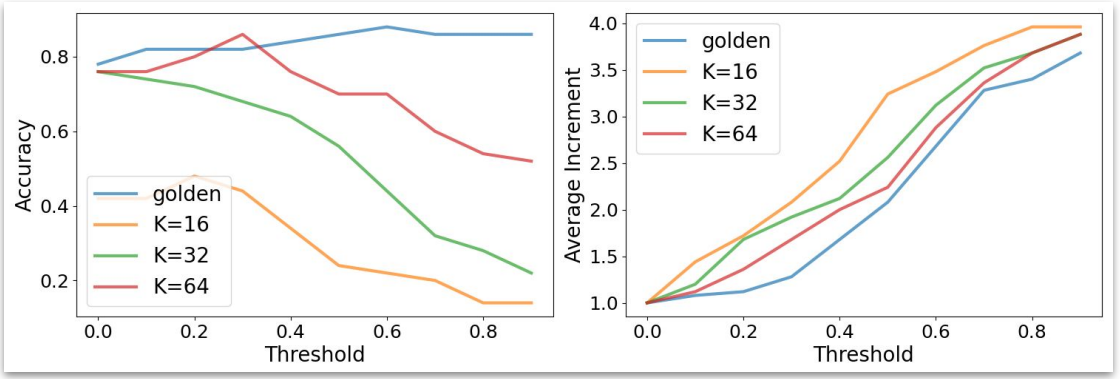


Reliability Analysis of DyNNs

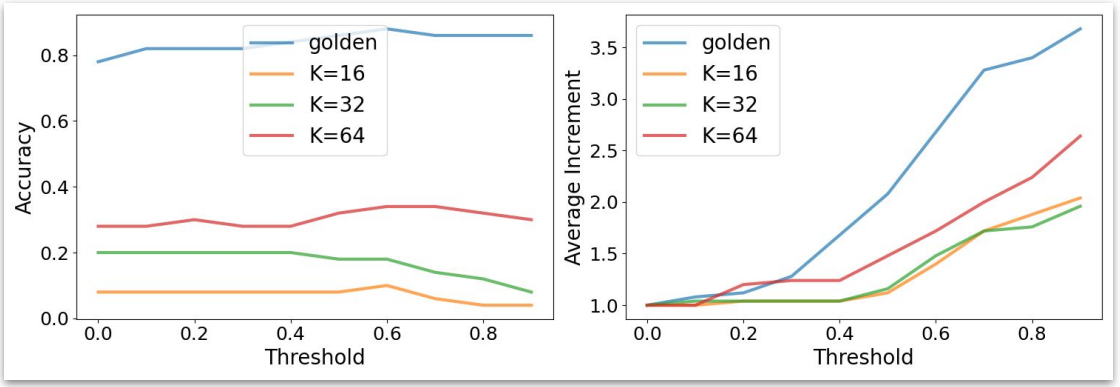
- **Emulation-based Fault Injection**
  - Simulating NVDLA MAC Arrays
  - Stuck-at Faults at Critical Gates
- **Case Study**
  - Slimmable AlexNet
  - Cifar-10 dataset







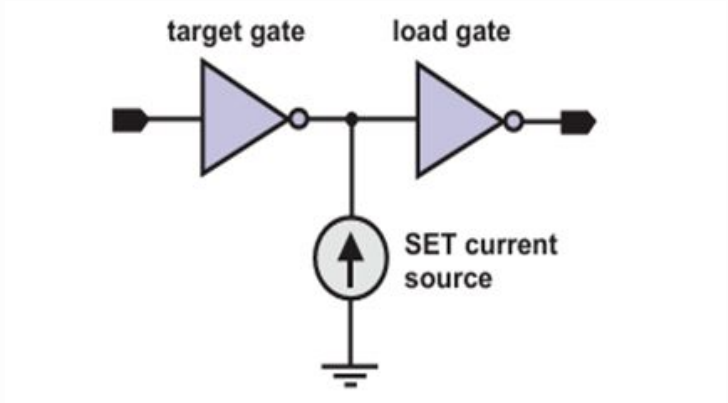
Stuck-at 1

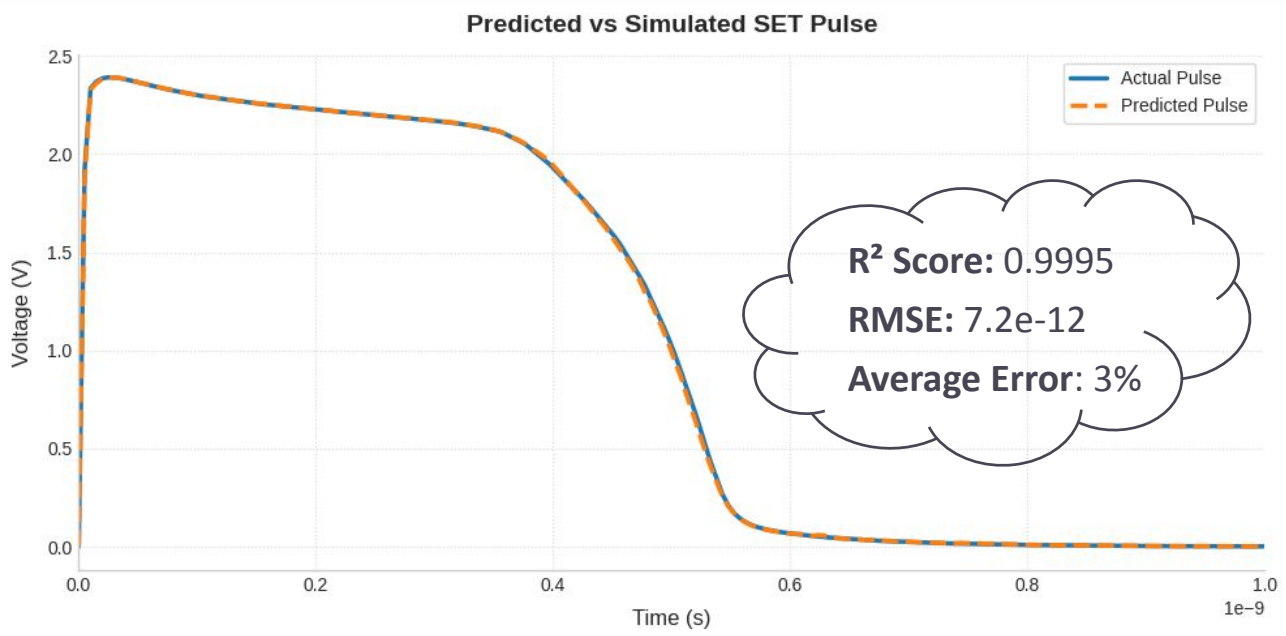


Stuck-at 0

ML Based SET Generation

- **Performed Spice Simulations**
  - **IHP 130nm PDK**
- **Utilized Machine Learning Models** to predict the generated SET Pulse
  - Based on Output Capacitance, Particle Charge, Cell Drive Strength and PVT corner
- **Developed SET Look-Up-Tables**
  - following liberty standards
- **Experimental Comparisons**
  - SPICE vs Machine Learning
  - SPICE vs LUT interpolations





What's Next?

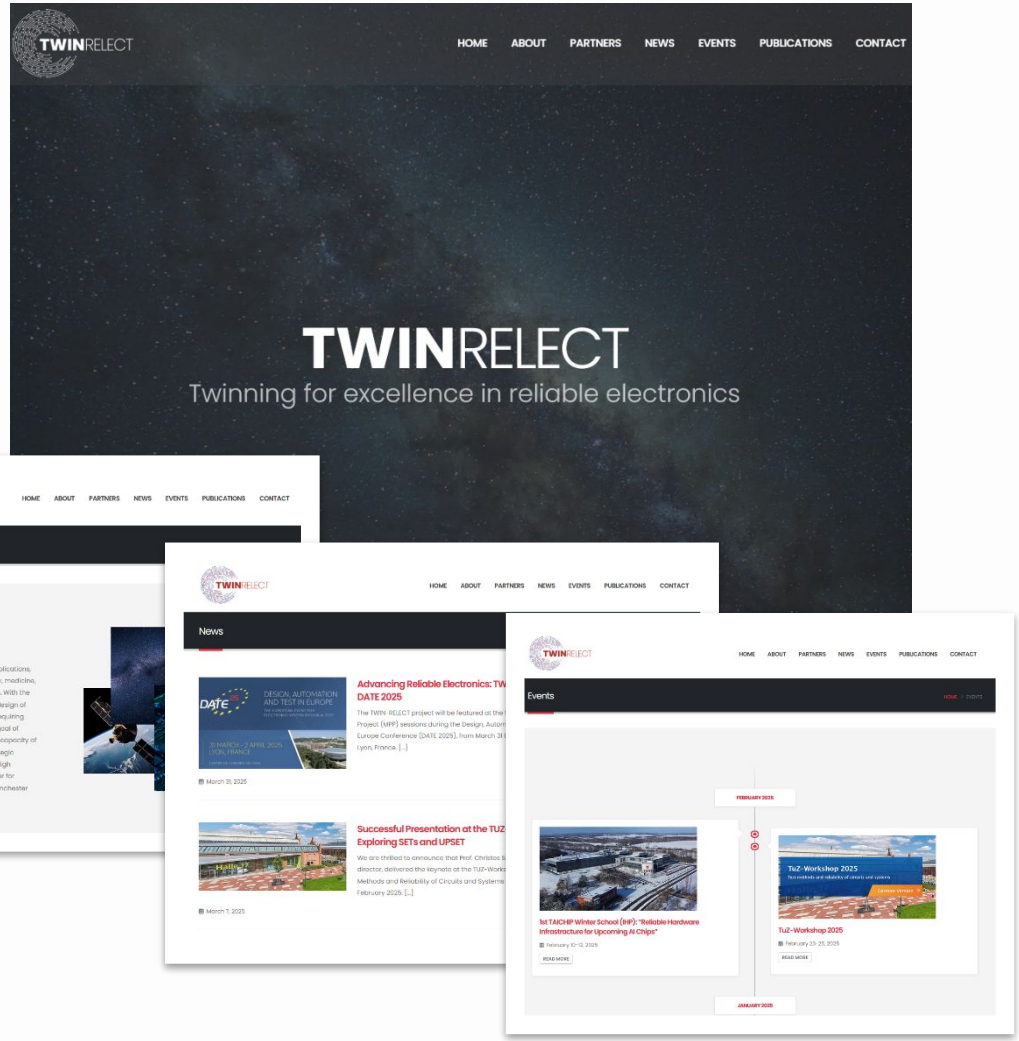
- **Irradiation test Campaigns**
  - TID and SEU evaluation of aging monitors
  - Neutron irradiation of a synchronous and an asynchronous Network on Chip
- **Aging analysis**
  - Parametric spice simulations
  - Utilize aging sensors
  - Aging-based STA
  - Aging-based SET analysis
- **Dynamic NN reconfiguration**
  - Detect Fault
  - Network reconfiguration to minimize output error
- **Integration into the EDA Tool Flow**
  - All methodologies and models developed during the project will be integrated into the EDA Tool Flow

Conclusion

- TWIN-RELECT: Twinning for Excellence in Reliable Electronics
- Started 12 months ago
- Research and innovation for Integrated Circuits (ICs)
  - Mission Critical Applications in Ionized Environments
- 5 Partners – 23 Researchers
  - Greece
  - France
  - United Kingdom
  - Germany
- Follow our actions
  - And stay tuned for the next events!!!

TWIN-RELECT Website & Mass Media

- URL: https://twin-relect.uth.gr/
- LinkedIn:
  - https://www.linkedin.com/company/twinrelect/
- Instagram:
  - https://www.instagram.com/twinrelect/
- Twitter/X:
  - https://x.com/twinrelect
- YouTube Channel:
  - https://www.youtube.com/@TWINRELECT



Thank you for Joining us today!

SCAN ME

TWINRELECT
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