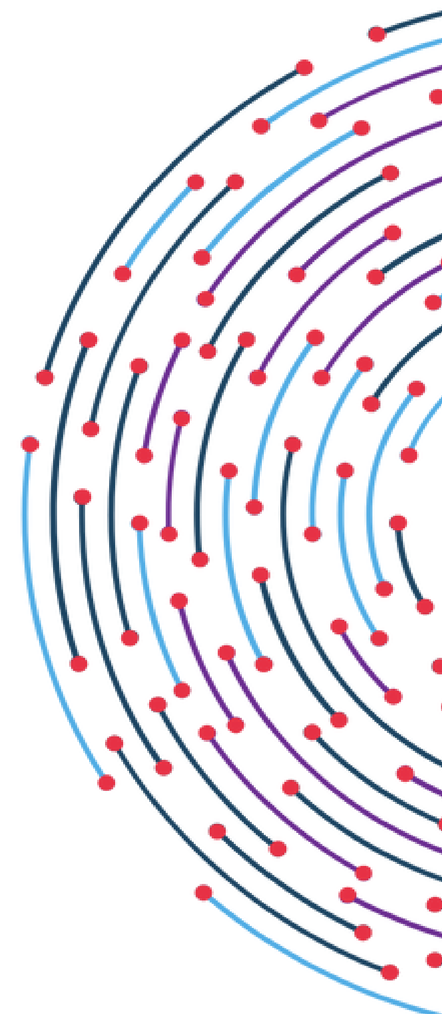
TWINRELECT

Twinning for excellence in reliable electronics



D1.2

DELIVERABLE REPORT

D1.2: 1st Report on Joint Research

WP1: Joint Research

Document information

Deliverable/Title	D1.2: 1st Report on Joint Research	**Work Package**	WP1
Leading Partner	UTH	**Participating Partner(s)**	IHP, CNRS, MAN
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Deliverable Type	R	**Dissemination Level**	PU
Official Submission Date	M17	**Actual Submission Date**	28/02/2026

Document history				
Version	**Date**	**Description**	**Editors**	**Comments**
0.1	11/11/2025	Initial draft – outline and Table of Contents	George Paliaroutis, Nikolaos Chatzivangelis	
0.2	13/1/2026	Progress on Tools Integration Finished	George Paliaroutis, Nikolaos Chatzivangelis, Nikolaos Zazatis	
0.3	28/01/2026	Added Conducted Work on 3.1	George Paliaroutis, Nikolaos Chatzivangelis	
0.5	23/02/2026	Updated Published & Accepted Papers	George Paliaroutis, Nikolaos Chatzivangelis, Nikolaos Zazatis	
1.0	27/02/2026	Final Official Version	All Authors & Editors	

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List of Acronyms

Description	Abbreviation
University of Thessaly	UTH
Leibniz Institute For High Performance Microelectronics	IHP
Centre National De La Recherche Scientifique	CNRS
University of Manchester	MAN
Work Package	WP
Integrated Circuit	IC
Static Timing Analysis	STA
Electronic Design Automation	EDA
Single Event Transient	SET
Single Event Multiple Transients	SEMTs
Register Transfer Level	RTL
Single Event Upset	SEU
Flip-Flop	FF
Look-Up Table	LUT
Dynamic Neural Network	DyNNs
Spiking Neural Network	SNN
System-On-Chip	SOC
Soft Error Rate	SER
Model Order Reduction	MOR
Technology Computer-Aided Design	TCAD
Error Propability	EP
Machine Learning	ML
Hardware Trojan	HT
Triple Modular Redundancy	TMR

Description	Abbreviation
Hardened RISC-V System-on-Chip	HARV-SoC
Error-Correcting Code	ECC
Network-on-Chip	NoC
Multiprocessor System-on-Chip	MPSoCs
Composite Current Source	CCS
Negative Bias Temperature Instability	NBTI
Electromagnetic Interference	EMI
Hot Carrier Injection	HCI
Performance, Power and Area	PPA
eXtensible Interconnect Network Architecture	XINA

1. Introduction and Overview of Research Activities

The continuous evolution of semiconductor technologies and the increasing complexity of modern integrated circuits (ICs) have been associated with reliability concerns across a wide range of critical application domains, such as medical systems, space, avionics, and industrial automation. As technology nodes continue to scale, electronic systems become increasingly vulnerable to radiation-induced transient faults, aging effects, and permanent degradation issues, generating a strong demand for advanced reliability-aware analysis and design methodologies.

The TWIN-RELECT project addresses these challenges by strengthening the research and innovation capacity of the University of Thessaly (UTH) in the field of reliable electronic systems through strategic collaboration with leading European research institutions; Leibniz Institute For High Performance Microelectronics (IHP) , Centre National De La Recherche Scientifique (CNRS)/University of Montpellier (UM), and the University of Manchester (MAN). A key pillar of the project is the execution of coordinated joint research activities that combine experimental characterization, fault modeling, fast reliability analysis based on Static Timing Analysis (STA) and artificial intelligence (AI) algorithms, as well as cross-layer EDA tool flow integration, aiming to enable scalable and accurate reliability evaluation of complex digital designs. The specific deliverable provides an overview of the joint scientific activities conducted within WP1 (Joint Research) during the first half of the project. It presents the technical progress achieved, the development of reliability analysis tools, and the collaborative research outcomes, including published, submitted, and ongoing scientific works.

1.1 Objectives and Scope of WP1

Joint Research is the core scientific work package of the TWIN-RELECT project and is primarily led by the UTH, which plays a central role in coordinating the research activities. One of the primary objectives is to design a unified cross-layer EDA tool flow methodology for analyzing and optimizing system reliability, modeling both transient and permanent faults across multiple abstraction levels, including device, circuit, gate, and architectural levels.

The scope of WP1 focuses on:

- the characterization and modeling of radiation-induced and aging fault effects in advanced technology nodes
- the modeling of fault generation and propagation based on simulations and irradiation experiments
- the design of a fast reliability analysis based on STA
- the integration of fault models, analysis techniques, and optimization methods into a unified cross-layer EDA design flow
- the validation of the complete EDA tool flow on a set of selected benchmark circuits

1.2 Summary of Work Conducted During the First Reporting Period

Significant advances were made in the characterization and modeling of fault effects using a combination of TCAD simulations, SPICE-level analyses, and experimental irradiation data. An initial version of the reliability analysis tool flow, including the integration of the PredicSEE, UPSET, SPICE, and EMBER tools, was designed and extended to support both transient and permanent fault modeling. In particular,

emphasis was placed on establishing consistent data exchange mechanisms between tools and ensuring common modeling assumptions among partners.

The primary focus of the first reporting period of the project was the generation of the joint research outputs, including the preparation and submission of scientific publications, collaborative studies, and experimental activities conducted in parallel with technical developments. These efforts established a significant basis for the subsequent project phases, enabling further optimization, tool integration, and validation. Also, the expansion and enhancement of joint publications and long-term research outcomes, as described in the following sections of this report, constitute the key future objectives of the project.

1.3 Deliverable Structure

This deliverable is organized into five main chapters that demonstrate the joint research activities of the TWIN-RELECT project during the first half reporting period. **Chapter 1** introduces the overall context and objectives of WP1 (Work Package) within the TWIN-RELECT project, and summarizes the scope of the joint research plan. **Chapter 2** discusses the progress made in the development and integration of the reliability analysis tool flow. It presents updates on the individual tools with emphasis on the modeling of radiation-induced fault effects and their combined use within the proposed tool flow. **Chapter 3** focuses on modeling, fault-tolerance techniques, and advanced analysis capabilities developed within the research plan, describing all work conducted in the context of conference papers and journal publications, as well as ongoing and targeted future studies. **Chapter 4** discusses the collaborative framework of the joint research activities, highlighting partner synergies and knowledge exchange. Also, it summarizes in tables the publications submitted to or published in journals and conferences. Finally, **Chapter 5** concludes the deliverable by summarizing the main scientific achievements of the reporting period, emphasizing the importance of collaboration among the TWIN-RELECT partners, and outlining the next milestones and long-term research directions.

2. Progress on Reliability Analysis Tool Flow

2.1 Cross-Level Reliability Methodology Refinement

2.1.1 Integration and Data Exchange Between Tools

The integration and data exchange process of the cross-layer methodology is based on the structure of the EDA flow, the connection of tools, and the determination of input/output interfaces. The proposed flow follows a tool integration framework, connecting device and transistor-level radiation modeling (PredicSEE, ECORCE, and SPICE simulations), with gate-level STA-based reliability analysis and optimisation (UPSET), and system-level fault-injection and masking evaluation (EMBER). As illustrated in Figure 1, the proposed flow facilitates the exchange of information across abstraction levels, allowing reliability data to propagate from device characterization to gate-level analysis and further to system-level evaluation.

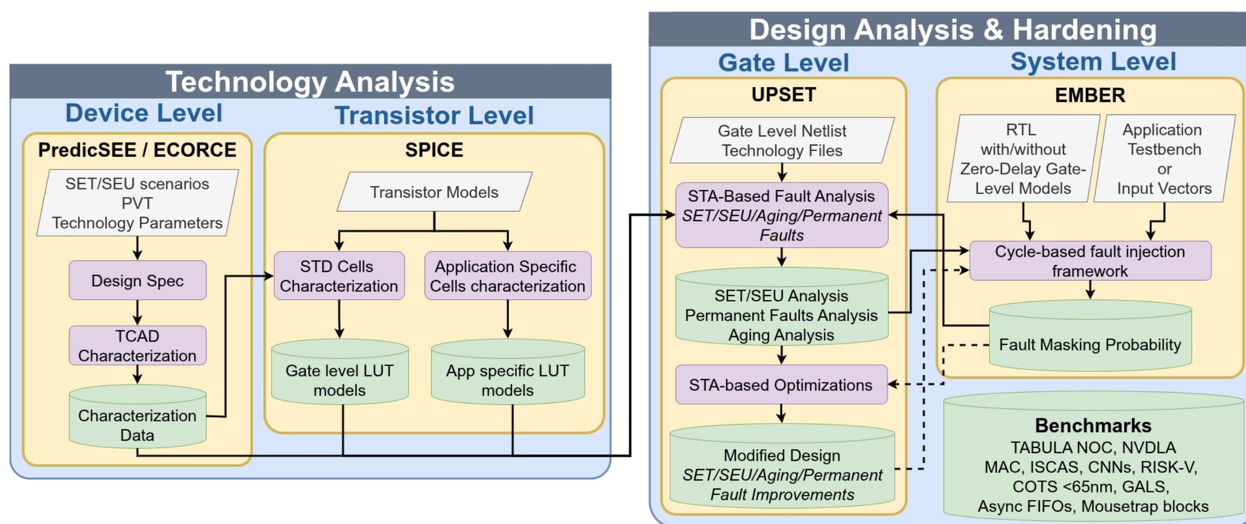

Figure 1: TWIN-RELECT EDA Tool Flow

The defined input data interface includes fault models derived from simulations and irradiation experiments, operating conditions, and circuit descriptions at multiple abstraction levels. On the other hand, data extracted from the output interface includes reliability metrics, fault sensitivity analyses, and hardened design solutions generated through optimization techniques. In parallel, internal information exchange among the tools is established across abstraction levels. Specifically, waveforms extracted by the PrediCSEE and ECORSE tools, corresponding to current and voltage pulses, together with LUT-based characterization obtained through SPICE simulations at device level, are provided as inputs to the UPSET tool for gate-level analysis. The gate-level analysis generates fault lists and critical-path information that are propagated to system-level evaluation provided by EMBER, while system-level feedback is returned to lower abstraction levels to support optimization refinement. This integration framework provides the foundation for the progressive automation and validation of the TWIN-RELECT reliability-aware EDA flow.

2.2 Updates on Tools Integration and Development

The key strength of the TWIN-RELECT tool flow is the integration of four cutting-edge software tools developed by the project partners into a unified EDA framework for the analysis and design of reliable ICs. In Deliverable D1.1 (Research Plan), a comprehensive description of the tools, their characteristics, and their role within the overall methodology was provided. PredicSEE and ECORSE tools are used at the device level to model radiation-induced effects and the generation of Single Event Transients (SETs) based on technology parameters and particle strike characteristics. SPICE simulations are utilized at the transistor level to characterize standard and application-specific circuit cells and to accurately model their electrical behavior under the impact of transient disturbances. At the gate level, UPSET conducts STA-based fault analysis to model SET propagation through combinational logic and clock distribution networks, analyzing the evaluation of circuit vulnerability. Finally, at the system level, EMBER provides fast, cycle-based fault injection and resilience analysis at the Register Transfer Level (RTL), modeling the evaluation of fault masking effects at the architectural and application level.

The present deliverable focuses on the first stage of the integration and combination of these tools into a cross-level reliability analysis flow. This initial integration effort is demonstrated through joint research activities and results reported in conference and journal publications, establishing the basis for further optimization in subsequent phases of the project.

2.2.1 PredicSEE - UPSET

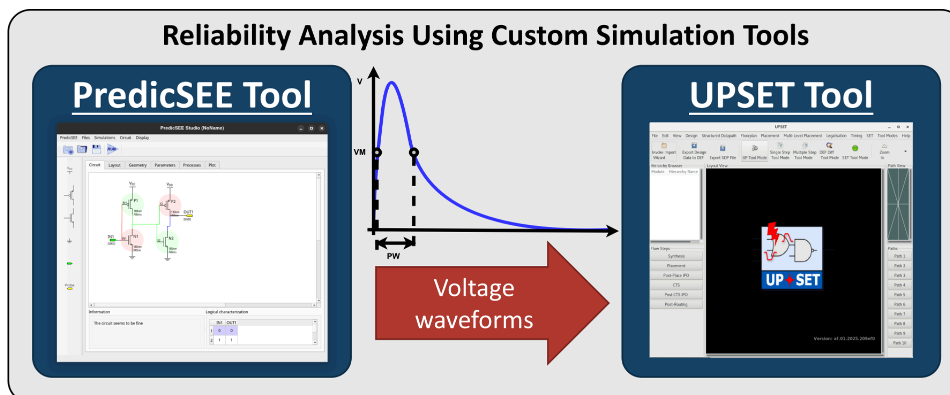

Figure 2: Reliability analysis flow using PredicSEE and UPSET simulation tools

In the context of the TWIN-RELECT project, an accurate cross-level SET reliability analysis is provided by combining two complementary simulation tools operating at different abstraction levels, as illustrated in Figure 2. Device-level SET pulse generation is performed using **PredicSEE**, while gate-level propagation and impact analysis is conducted using the **UPSET** framework. The extracted voltage pulses obtained from the characterization of components using the **PredicSEE** tool represent realistic SET pulses induced by particle strikes. These waveforms are used as inputs to the **UPSET** tool, i.e. the subsequent stage to model the propagation of SETs [3]. Accurate modeling of SET generation is a critical step, as it defines the actual shape and magnitude of the transients based on both particle strike characteristics and technology-dependent parameters. This process is essential for enabling reliable SET propagation analysis and for identifying which transient events are most likely to compromise the integrity of ICs.

2.2.2 EMBER - UPSET

Following the SET analysis, the latched pulses captured by the Flip-Flops (FFs) result in a Single Event Upset (SEU), necessitating a comprehensive flow that bridges SET and SEU analysis. This process initiates with the SET analysis provided by the **PredicSEE** and **UPSET** tools, as previously discussed in Section 2.1.1. Subsequently, **EMBER** is utilized to perform accurate multi-cycle SEU analysis on the most error-prone components, specifically those FFs with a high probability of latching an SET pulse, to assess their functional impact on the Primary Outputs. This stage is critical for identifying the most vulnerable FFs and calculating the Error Masking Probability, which quantifies the system's inherent resilience. Finally, this vulnerability data is loaded back into the **UPSET** tool to facilitate targeted gate-level mitigation techniques, with the ultimate goal of maximizing the Error Masking probability and hardening the circuit against transient-induced failures. This tool flow is currently a work in progress and a preliminary interface between the tools was established in [3], where UPSET provided a zero-delay gate level netlist to EMBER, enabling an automated communication framework in line with the TWIN-RELECT EDA tool flow specifications.

2.2.3 SPICE - UPSET

Analogous to the **PredicSEE-UPSET** methodology, our approach integrates transistor-level SET pulse generations, using SPICE models, with the **UPSET** tool to facilitate multi-level propagation and vulnerability analysis. To achieve high characterization accuracy, we perform exhaustive SPICE-based simulations across a comprehensive parameter space [14]. This includes the systematic variation of PVT (Process, Voltage, Temperature) corners, collected charge levels, input logic vectors, and output loading capacitances. The resulting transient data are post-processed to construct custom SET-based Look-Up Tables (LUTs), which are encapsulated within industry-standard **Liberty file formats** (.lib). By integrating these physics-informed libraries into the UPSET tool, we enable the framework to transition from generic pulse modeling to technology-specific, accurate SET generation. This enables a robust analysis of SET propagation and its ultimate impact on the reliability of complex IC designs under realistic operating conditions.

3. Modeling, Fault Tolerance, and Tool Integration

This section provides a comprehensive description of the work performed within the TWIN-RELECT research activities related to fault effect characterization and modeling, fault-tolerance techniques and reliability metrics, and STA-based fault analysis and optimization. The presented works follow the objective of advancing the cross-layer TWIN-RELECT EDA tool flow for reliability analysis and optimization of digital ICs, integrating modeling, analysis, and validation across multiple abstraction levels. Therefore, significant progress has been achieved during the first half of the project in consolidating the overall tool flow architecture, enhancing analysis and optimization capabilities, and advancing fault modeling and characterization activities supported by simulations and irradiation campaigns. Several outcomes have already been disseminated through well-known conferences and journals, whereas ongoing developments focus on more comprehensive modeling and further optimizations that constitute the basis for future work and improvements.

3.1 Characterization and Modeling of Fault Effects

3.1.1 Overall Progress

The design of accurate fault models constitutes a key target of the research studies conducted in the context of the project, supporting the modeling of transient and permanent reliability effects. Moreover, fault behavior across multiple abstraction levels is analyzed through device-level characterization, standard-cell reliability assessment, and application-specific circuit analysis, providing the appropriate framework for subsequent fault analysis and optimization processes within the integrated TWIN-RELECT EDA tool flow. Finally, the utilization of data obtained from irradiation campaigns in various works will be a crucial step toward achieving a realistic representation of effects such as radiation-induced and aging phenomena.

3.1.2 Description of Work Conducted

- **Special Session Paper: Simulation Methodologies and Experiments for Reliability Analysis of Devices in Radiation-Harsh Environments [3]**

  This work investigates reliability challenges in radiation-prone digital systems, combining simulation-based fault analysis with experimental validation. A novel methodology for modeling SETs and a cross-layer framework for analyzing the impact of hardware faults on Dynamic Neural Networks (DyNNs) are introduced. Neutron irradiation results on a fault-tolerant RISC-V SoC highlight the importance of architectural mitigation strategies against SEUs.

  - *PredicSEE, UPSET, SET Modeling, device, and gate-level analysis*

    This part of the special session represents the first work in which the PredicSEE and UPSET tools are combined. In particular, the radiation impact on ICs functionality consists of two complementary parts to address this challenge. The former focuses on SET generation using the PredicSEE tool, which offers a detailed physics-based simulation framework. In contrast, the latter examines SET propagation through the clock tree distribution network with the UPSET tool, enabling accurate assessment of timing violations and glitch effects in digital circuits. The main objective of this combined

methodology is to deliver a comprehensive evaluation of radiation-induced SET effects on clock tree networks, providing insight into their potential impact on the overall functionality of ICs.

- *Reliability Analysis on Dynamic Neural Networks*

  DyNNs offer efficiency for edge AI by adapting computation to input complexity, but their reliability under hardware faults remains largely underexplored. Unlike static neural network models, faults in DyNNs can affect both output tensors and prediction confidence, altering activation patterns of constituting subnetworks. This work introduces a cross-layer analysis framework to study how MAC-level faults in state-of-the-art accelerators like NVDLA impact DyNN accuracy, latency, and confidence—marking a first step toward dependable dynamic AI systems. In practice, dynamic DNNs are trained on CIFAR-10 using PyTorch. Then, NVDLA MAC unit faults are analyzed with EMBER tool using network weights and inputs as vectors. Derived fault models representing MAC unit reliability are mapped back into the PyTorch DNN. Finally, we evaluate the impact of these hardware faults on overall network accuracy and prediction confidence margin.

- *Characterization of a Reliable RISC-V SoC in an SRAM-Based FPGA for Neutron Irradiation*

  Advancements in avionic systems technology demand enhanced resilience against environmental hazards such as radiation, which can compromise the reliability of electronic components. In this work, we evaluated the Hardened RISC-V System-on-Chip (HARV-SoC) under radiation in an FPGA with an SRAM-based configuration memory. This approach allowed not only the observability of the processor but also the analysis of radiation-induced faults affecting the configuration memory. A fault injection campaign was carried out at the ChipIr neutron radiation facility to assess the system's reliability. We present a reliability analysis of the HARV-SoC and compare it with previous experiments performed on FPGAs with flash-based configuration memories, enabling a deeper understanding of the impact of memory technology on system robustness.

- **Reliability Analysis of Clock Networks under Radiation-Induced Transients Using Custom Simulation Tools - Extension of SET Analysis on Clock Networks [19]**

  This work is an extension of the first part of the special session presented at 38th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS 2025) [3] and has been submitted to the Microprocessors and Microsystems (MICPRO) journal. The proposed methodology combines physics-based SET generation using the PredicSEE tool with probabilistic STA-based propagation analysis implemented in the UPSET framework. Transient voltage waveforms corresponding to SETs are injected into clock distribution networks and critical paths, enabling the evaluation of radiation effects as well as logical, electrical, and timing masking mechanisms.

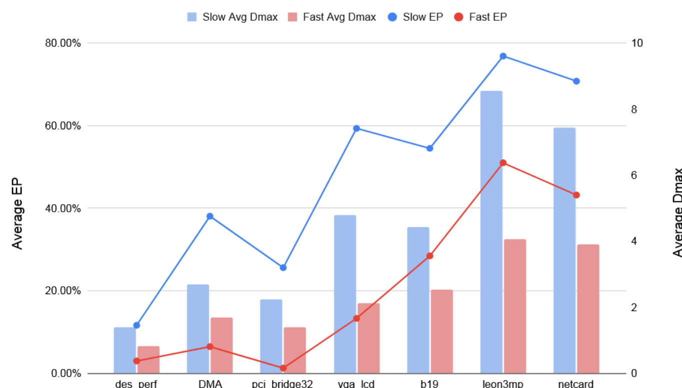

Figure 3: Correlation of Error Probability (EP) and Average Dmax for slow and fast designs

ISPD2012 benchmark circuits were utilized to evaluate the proposed approach, considering both low-effort and high-effort timing-optimized implementations. The experimental results indicate that clock networks comprise a highly critical subsystem. In other words, SETs injected at clock buffers can propagate to a large number of FFs with a high probability of disrupting synchronization, particularly in designs with larger data-path delays. The proposed Error Probability (EP) metric captures the interaction between clock-network disturbances and data-path timing, revealing a strong dependence on the average longest path delay (Dmax), as illustrated in Figure 3. In fast (high-effort) implementations, most data paths exhibit shorter delays, whereas the clock network delay increases due to the larger number of clock buffers, causing SET-induced disturbances to reach the clock inputs of FFs only after the longest data path has settled. Therefore, the FFs are more likely to latch correct values, resulting in lower average EP. For critical paths, logical masking is mainly affected by logic depth and functional properties, while electrical and timing masking are strongly affected by design performance and interconnect characteristics. These observations highlight the complex nature of SET susceptibility in modern circuits and highlight the challenges of radhard design, where power, performance, and area constraints must be carefully balanced against robustness requirements.

- **Compact SER Models for Line-Source-Induced Charge Collection Using Model Order Reduction [4]**

This work was conducted as part of the collaborative research activities of the EU-funded projects TWIN-RELECT and COIN-3D Project and was accepted and presented at the DFT 2025 conference. It contributes to the development of accurate and computationally efficient fault modeling techniques for radiation-induced reliability analysis. In particular, it addresses the modeling of radiation-induced charge collection phenomena, such as SETs in semiconductor technologies, which are traditionally analyzed using Technology Computer-Aided Design (TCAD) simulations. Therefore, the proposed work presents a Model Order Reduction (MOR) methodology for fast, compact, and efficient Soft Error Rate (SER) modeling. For TWIN-RELECT purposes, this work strengthens the cross-layer reliability modeling strategy by providing compact SER models that can be utilized for multiple radiation scenarios. This model provides a fast evaluation of collected charge and current pulses that can be used as inputs to higher-level analyses, such as gate-level SET modeling and STA-based fault propagation (UPSET tool). Also,

this contribution aligns with COIN-3D by supporting accurate EDA methodologies for reliability evaluation in advanced VLSI and 2.5D/3D integration scenarios.

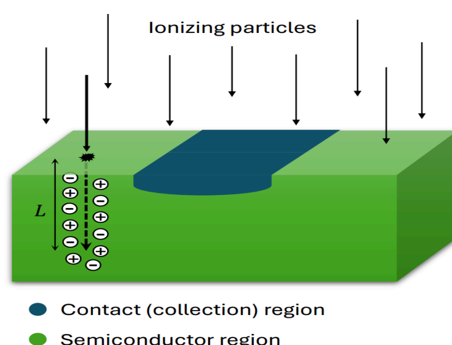

Figure 4: A semiconductor material with a collection region under ionizing particles strike

Following the description of charge generation and collection mechanisms as shown in Figure 4, the impact of the spatial proximity between the ion track and the sensitive node is additionally examined. The efficiency of charge collection depends on the distance between the track and the contact area. As depicted in Figure 5, when the ion track directly intersects the contact region (0 µm offset), the collected charge reaches its maximum value, exhibiting a steeper initial rise and a shorter total collection time. Increasing the offset up to 1.3 µm significantly reduces the collected charge due to weaker spatial coupling.

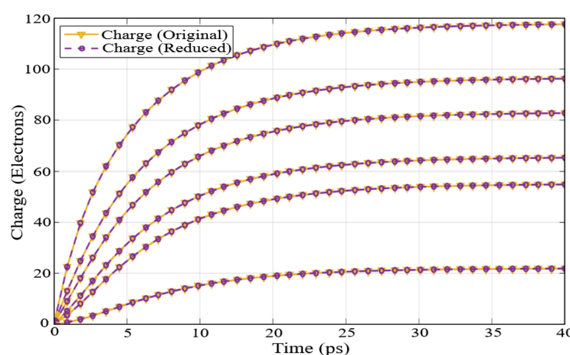

Figure 5: Collected charge at the contact area for benchmark B2 with different distances from the input track: 0, 0.2, 0.5, 0.7, 1.0, and 1.3µm (from top to bottom)

- **Compact SER Models via Model Order Reduction of Diffusion-Based Charge Collection [6]**

This work was presented at the 21st Interational Cnference of Synthesis, Modeling, Analysis and Simulation Methods, and Applications to Circuit Design (SMACD 2025) and, similarly to [4], was conducted in collaboration with members of the COIN-3D project. It presents a novel and efficient methodology for SER modeling in advanced VLSI technologies, handling the increasing need for reliable radiation-aware analysis. The primary contribution of this work is the development of compact physics-based SER models through the application of MOR techniques. In particular, it combines Moment Matching and Extended Krylov Subspace projection to

significantly reduce the complexity of diffusion-based charge transport modeling while maintaining high accuracy in charge collection prediction. It contributes to the characterization and modeling of radiation-induced fault effects, strengthening the TWIN-RELECT research objectives by connecting physics-level reliability modeling with accurate design analysis and enabling efficient reliability-aware design methodologies.

The work [4] extends the proposed compact SER modeling methodology from point-source charge deposition to a more realistic and practical line-source radiation model, providing the modeling of ion track impact on semiconductor devices.

- **Temperature-Aware Compact SER Modeling Using Model Order Reduction [20]**

  This work extends the work presented at DFT 2025 [4] and has been submitted to the Microprocessors and Microsystems (MICPRO) journal. It focuses on enhancing compact SER modeling by incorporating temperature-dependent charge transport into a parametric Model MOR framework, addressing the need for accurate and scalable reliability analysis under realistic operating conditions. Starting from the diffusion–collection equation, temperature dependence is introduced through key physical parameters, leading to a temperature-parameterized state formulation suitable for systematic analysis.

  To efficiently manage temperature variability, a parametric MOR approach based on the Extended Krylov Subspace combined with Moment Matching is proposed. This methodology enables the extraction of reduced-order models that remain accurate over a wide range of operating temperatures while significantly reducing computational complexity. Experimental validation on large three-dimensional benchmarks demonstrates substantial speedups compared to full-order simulations, with high accuracy preserved across the examined temperature range. These results support fast and reliable temperature-aware SER estimation, directly contributing to the project's objectives of developing efficient modeling and analysis techniques for large-scale reliability assessment of electronic systems.

- **Machine Learning Approach for Cross-Technology Prediction of the Generated Single Event Transient [14]**

  This work proposes a Novel Machine Learning pipeline for Cross-Technology Prediction of the Generated Single Event Transient, spanning form 130nm to 2nm technologies. It has been submitted and accepted to the 31st IEEE European Test Symposium (ETS2026). The dataset for the training of ML (Machine Learning) models is generated through extensive SPICE simulations utilizing the Macro BIAS model. The trained ML models demonstrate the capability to predict generated SET pulses even in unseen and advanced technologies, providing a scalable alternative to manual characterization. Moreover, the ML models support transfer learning, enabling rapid calibration to new and emerging technologies using only a limited set of inexpensive SPICE simulations, without requiring training from scratch. These results showcase the potential of ML-driven approaches to significantly accelerate the reliability-aware design cycle while maintaining the physical accuracy required for safety-critical applications.

- **Prediction of Single Event Transient Propagation Using Machine Learning Models [2]**

This work analyzes the applicability of ML models for predicting the variation of SET pulse width during propagation through standard combinational logic cells. The study is based on a dataset generated from SPICE simulations performed on INV, NAND2, and NOR2 gates from a 130 nm CMOS standard cell library, considering key parameters such as input SET pulse width and polarity, target and load gate driving strengths, temperature, as well as supply voltage. Ten regression models were trained and evaluated to assess their ability to predict SET propagation effects at the gate level accurately. The overall proposed flow for SET propagation analysis is illustrated in Figure 6, including dataset creation, model training, and application to circuit-level reliability assessment.

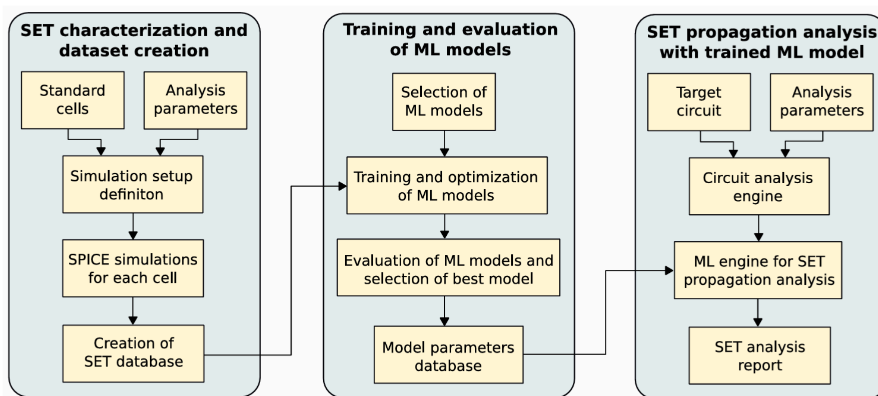

Figure 6: Flow for ML-based SET propagation analysis

The results obtained demonstrate that ML models can achieve very high prediction accuracy for individual standard cells, with different models providing a promising performance depending on the type of gates. Although prediction accuracy decreases when SET propagation is analyzed across combinational logic paths due to error accumulation, the approach provides a time-efficient analysis of SET effects in complex designs. Therefore, this work contributes to the project's objectives of developing an efficient method for reliability assessment of digital circuits operating under realistic conditions of temperature and voltage variability, enabling the fast and accurate SET propagation analysis.

- **On-Chip Reliability Sensor Analysis Under Combined Effects of Aging and Power-Supply Noise [15]**

This work analyzes the performance of On-Chip reliability sensor under the combined effects of aging and power supply noise. It has been submitted to the 29th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS2026). Building upon the evaluation of NVDLA MAC unit reliability, this work analyzes the performance of On-Chip reliability sensors under the combined effects of physical degradation and environmental interference. Specifically, we investigate the impact of NBTI(Negative Bias Temperature Instability)-induced aging (utilizing the IHP 130nm model) and Electromagnetic Interference (EMI) noise in compliance with IEC standards. Preliminary SPICE simulations and reliability monitor data, projected over a 20-year aging horizon, indicate that the concurrence of power supply noise and aging significantly intensifies critical path delays, which is depicted in Figure 7. Such degradation poses a high risk of functional failures and the subsequent propagation of

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erroneous signals through neural network architectures. This research provides a foundation for future multi-path analysis across diverse library characterizations and complex noise profiles.

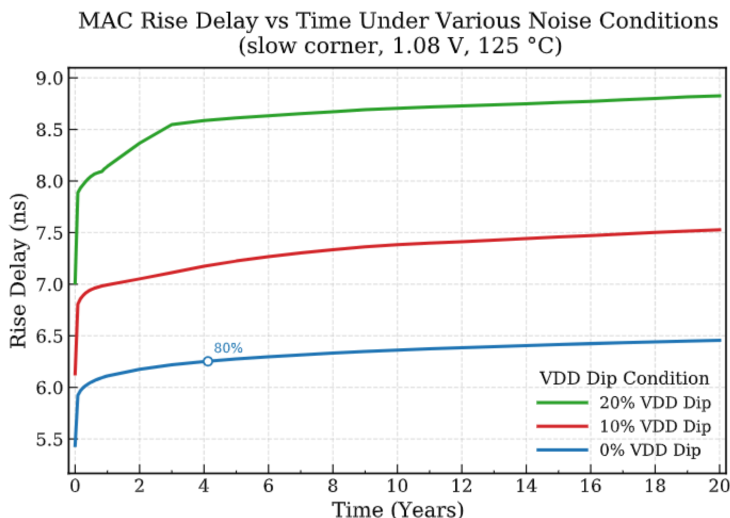

Figure 7: MAC Unit rise delay aging analysis (20 Years) under various noise conditions

- **An Ultra-Low Cost and Multicast-Enabled Asynchronous NoC for Neuromorphic Edge Computing [18]**

  This journal work, published in the IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), presents an ultra-low cost and multicast-enabled asynchronous NoC architecture designed for energy-efficient communication in neuromorphic edge computing systems. Its primary contribution is in the design of a lightweight asynchronous communication infrastructure that decreases energy consumption and area overhead while retaining high performance for event-driven, spike-based data transmission. Experimental evaluation indicates significant energy savings compared to state-of-the-art methods, emphasizing the advantages of architectural specialization and efficient asynchronous design techniques.

  This work, within the framework of the TWIN-RELECT project, contributes to the development of effective cross-layer design methodologies and scalable hardware architectures, supporting the project goals toward reliable and efficient electronic system design.

- **Aging Aware STA-Based Reliability Analysis [publication WIP]**

  This work is currently a WIP and the corresponding publication is in preparation. We are implementing an aging-aware STA flow for the IHP 130 nm library by integrating an NBTI aging model into the STA engine through standard-cell timing derate factors, enabling worst-case quantification of long-term slack reduction at scale.

  In parallel, we are extending the UPSET framework to support aging-aware SET analysis, so that SET propagation and endpoint vulnerability can be evaluated under the same aging-degraded timing conditions (i.e., reduced margins that can influence propagation, filtering, and capture likelihood). As next steps following the initial publication, we plan to broaden the study to include additional aging mechanisms and also analyze the combined effects of aging and EMI to provide a comprehensive reliability assessment that jointly addresses timing robustness and SET susceptibility in large-scale designs.

- **Layout-Based SET Generation and Propagation [publication WIP]**

  This work is planned as a significant optimization of the UPSET tool to support the analysis of Single Event Multiple Transients (SEMTs) and will constitute part of the ongoing research activities within the TWIN-RELECT project. It aligns with the goals of the project, strengthening UPSET's accuracy for advanced reliability evaluation of IC functionality by considering the impact of radiation. Until now, UPSET has focused on the analysis of SETs. In other words, a transient fault is generated at the output of a logic gate and subsequently propagated through the circuit to determine if it is latched by a memory element, potentially leading to a soft error. While this analysis is efficient, fast, and reliable, it does not fully model the physical effects of particle strikes in advanced technologies, where a single particle hit can affect multiple adjacent components.

  The proposed optimization aims to integrate detailed layout information into the SET modeling process, providing a more realistic analysis of radiation-induced phenomena. In particular, physical design data in DEF and GDSII formats will be utilized to extract placement information for logic gates within the circuit. Particle strikes will be modeled as random events occurring at arbitrary locations on the layout. Finally, the affected area will be treated as an oval shape, and all gates within this region will be considered simultaneously affected by the particle hit, generating multiple glitches at their outputs. Propagation of SEMTs will be based on UPSET's existing STA framework, which enables the evaluation of their effects on circuit behavior and the probability of soft error occurrence. By integrating SEMTs modeling, the improved UPSET tool will significantly enhance the accuracy of reliability analysis, approaching more closely the actual physical impact of radiation events in modern ICs.

3.2 Fault-Tolerance Techniques and Reliability Metrics

3.2.1 Overall Progress

The investigation of fault-tolerance techniques focuses on the evaluation of mitigation mechanisms at gate, circuit, and architectural levels, aiming to decrease susceptibility to transient and permanent faults while handling design overhead. Emphasis is placed on reliability assessment by fault-injection methodologies, enabling the comparison of different hardening approaches under realistic operating conditions. In parallel, the definition of reliability metrics supports a compatible evaluation of circuit vulnerability. Therefore, the combination of metric definition and mitigation modeling specifies a structured framework that reinforces the design of reliable approaches and optimization activities.

3.2.2 Description of Work Conducted

- **Fault Injection Attacks Based on Layout-Driven SER Analysis [5]**

  This work analyzes the combined impact of reliability-based Hardware Trojans (HTs) and soft errors, with particular emphasis on the generation and propagation of SEMTs in modern ICs. A layout-driven fault modeling methodology is presented, in which each circuit is divided into spatial regions (grids), and the reliability of each region is evaluated using the SER as a metric of sensitivity. Monte Carlo simulations, SEMT modeling, and masking mechanisms are integrated into the proposed analysis and contribute directly to the modeling of fault effects by accurately modeling the impact of SEMTs at physical, electrical, and timing abstraction levels. Furthermore,

the timing-aware modeling is utilized by the proposed methodology to evaluate fault propagation, supporting the STA-based fault analysis of WP1.4 without requiring exhaustive SPICE-level simulations. The use of grid-level SER analysis as a sensitivity metric provides a practical reliability assessment mechanism, enabling comparative evaluation of circuit susceptibility before and after HT injection.

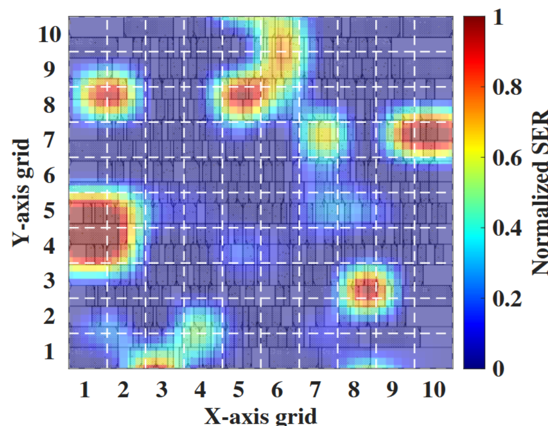

Figure 8: Grid-SER evaluation

In this work, each circuit is partitioned into smaller regions (grids) to evaluate its vulnerability. A sufficient number of particle hits is injected into each grid to ensure uniform excitation across the die area. Figure 8 presents the vulnerability profile of a representative benchmark, as obtained using the proposed methodology, where each grid is assigned a normalized SER value (with higher vulnerability indicated in red). Variations in vulnerability are influenced by factors such as gate density, masking effects, and proximity to FFs. This analysis is used to guide the selection of target sub-circuits for the injection of SEMT-driven HTs, which are placed at the outputs of the most sensitive gates. The objective is to evaluate whether the presence of SEMT-driven HTs increases the susceptibility of the grid, thereby worsening the circuit's vulnerability to soft errors. The proposed study provides realistic benchmarks that support the overall objectives of the project, in particular the development of cross-layer methodologies for reliability-aware IC analysis.

- **Implementation and Evaluation of a Sensitivity-aware Hardware Trojan for SET-induced Soft Error Rate [17]**

This journal article, published in the MDPI Electronics, investigates the combined impact of radiation-induced SETs and HTs on the reliability of digital circuits. The proposed methodology focuses on gate-level sensitivity evaluation to identify circuit locations where HT injection would be most impactful. The HTs implementation affects not only the sensitivity of individual gates but also the overall circuit vulnerability, since HTs can increase the IC's susceptibility to radiation-induced faults. Within the context of the project, this work constitutes a crucial modeling contribution, as the combined effect of SETs and HTs comprises a vital challenge for IC reliability and security. Furthermore, this work directly contributes to the project objectives by addressing the combined impact of multiple fault sources, providing novel modeling insights into how transient radiation effects and malicious hardware modifications interact. The experimental evaluation shows a significant increase in gate sensitivity and overall SER after HT injection,

highlighting the effectiveness of the proposed method in generating challenging benchmarks for reliability and security assessment tools. Overall, this contribution strengthens the cross-layer analysis approach promoted by TWIN-RELECT, connecting physical radiation effects, gate-level fault modeling, and system-level security implications within a unified evaluation framework.

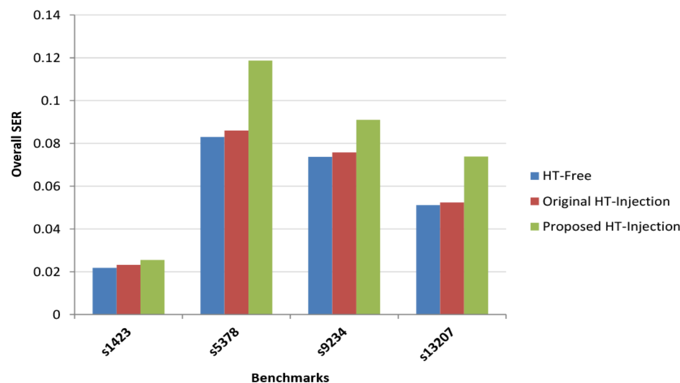

Figure 9: SER results highlight the stronger impact of the proposed HT-injection

This work constitutes an extension of the study in [21]. Figure 9 presents the SER evaluation for four ISCAS'89 benchmarks used in this article, comparing the SER of circuits without HTs, the theoretical HT-injection approach from [21], and the proposed methodology. The results indicate that the proposed method results in the highest increase in SER across all benchmarks, even if only a limited number of HTs is integrated. This observation confirms the conclusion that combining HTs with gates of moderate sensitivity significantly worsens overall circuit susceptibility. The inserted HTs strengthen the generated SETs, thereby increasing the vulnerability of the affected gates and elevating the likelihood that these transients will be captured by memory elements, ultimately amplifying the overall IC vulnerability.

- **Design and Reliability Analysis of a Pipeline RISC-V Processor Core [12]**

This work was submitted and accepted at the 27th IEEE Latin American Test Symposium (LATS 2026) and enhances the previously developed [22] HARV-SoC by implementing a pipelined architecture. Reliability and performance are key design concerns for embedded processors deployed in space and safety-critical environments. Therefore, the proposed implementation improves execution efficiency while maintaining a straightforward design to mitigate potential reliability issues. Although the pipeline enhances performance, it entails trade-offs between performance and reliability depending on the chosen design options. A detailed analysis is presented by performing fault-injection simulations in the processor core to model the effects of SEUs in the core's FF elements, and by estimating the effects in future irradiation experiments.

The results provide valuable insights into the processor's robustness and identify the critical elements for future hardening implementations targeting specific architectural components. Consequently, this work supports the objectives of the project, contributing to the analysis and modeling of transient fault effects and to the definition of reliability metrics. Furthermore, the processor core could be utilized as a representative benchmark for validating cross-layer reliability analysis approaches and supports the development of STA-based fault analysis and optimization techniques.

- **Characterization of a Fault-Tolerant RISC-V SoC in an SRAM-based FPGA under Proton Irradiation [11]**

  This work was submitted and accepted at the LATS 2026 and presents the characterization of a fault-tolerant RISC-V System-on-Chip implemented on an SRAM-based FPGA under proton irradiation. Radiation-induced faults, and in particular SEUs, are investigated due to their impact on both the logic and configuration memories of SRAM-based FPGAs. The HARV-SoC incorporates a fault-tolerant soft-core processor designed with in-circuit hardening techniques such as Triple Modular Redundancy (TMR) and Hamming Error-Correcting Code (ECC), combined with structured fault-observability mechanisms to enhance system resilience under radiation. In particular, a characterization of proton irradiation for the HARV-SoC implemented on an Xilinx Artix-7 FPGA is presented aiming to investigate the susceptibility of both the processor architecture and the FPGA configuration memory to radiation-induced faults.

  The experiments were conducted using proton beams at different energies to assess the impact of radiation on functional correctness and recovery behavior, providing insights into the reliability of SRAM-based FPGA platforms for space-grade and mission-critical applications. In addition, these experiments support project objectives related to fault characterization, fault-tolerance assessment, and validation through irradiation campaigns.

- **Resilience Analysis of a Fault-Tolerant MPSoC Interconnection Architecture under SEU Fault Injection [10]**

  This work was submitted and accepted at the LATS 2026 and investigates the fault-tolerance of the eXtensible Interconnect Network Architecture (XINA), a configurable Network-on-Chip integrated with an AMBA AXI-compatible Network Interface, targeting radiation-harsh environments. The architecture employs TMR in the control logic and Hamming ECC in the data buffers to enhance reliability. The evaluation focuses on the interconnection fabric of a 10×10 Multiprocessor System-on-Chip (MPSoC) prototype composed of 100 routers and 100 AXI-connected cores, where manager and subordinate IPs act as traffic generators and monitors data integrity under full load. A large-scale fault-injection campaign comprising 1,000 simulations with SEU injections was conducted to assess the impact of fault-tolerant mechanisms across four hardening configurations.

  The results demonstrate improved reliability, with the fully protected architecture achieving an 87.2% reduction in observed errors relative to the baseline while maintaining stable throughput and data integrity across all tests. These findings confirm the effectiveness of combining Network-on-Chip (NoC) and Network Interface (NI) hardening for resilient interconnect design, reinforcing XINA as a dependable and scalable solution for high-reliability MPSoCs in mission-critical applications. Finally, this study contributes to the objectives of the project related to fault-tolerance assessment, reliability evaluation, and the validation of resilient MPSoC architectures.

- **Testing Architecture for Bundled-Data Asynchronous NoC Switches [23]**

  This paper, submitted at AYNC 2026 and pending peer review, presents a test architecture that makes a modern 2-phase bundled-data asynchronous NoC switch (TaBuLA) compatible with

standard industrial scan-based production test, so unmodified commercial ATPG tools can be used and patterns can be applied on conventional ATE. The motivation is that asynchronous NoCs offer strong energy/area/modularity benefits, but their lack of a global clock plus feedback loops, asynchronous control (set/reset/enables), and mixed latch/FF state elements typically cause standard DFT rule checks to fail—so the baseline design is effectively "untestable" by conventional ATPG (reported as ~0 coverage).

The core contribution is a systematic, bottom-up method that converts each TaBuLA switch building block into a synchronous, scan-testable abstraction while preserving functional asynchronous behavior outside test mode. The approach uses LSSD-style scan for the latch-dominated parts (two non-overlapping scan clocks) and a separate scan chain for flip-flops, and it resolves key issues by inserting scan-capable latch pairs, cutting combinational feedback cycles (e.g., in C-elements), and restructuring arbiter MUTEX and other control elements so that internal state becomes controllable/observable under ATPG. Two DFT versions are explored: v1 achieves full coverage by exposing many internal async control points as top-level IOs (impractical in pad count), while v2 removes this by expanding the "DFT horizon" to the full NoC and using a small set of shared test controls (e.g., a special testmode for internal clock multiplexing) so controllability/observability is achieved through scan rather than extra pins.

Experimental results on an 8×8, 37-bit TaBuLA switch synthesized in SAED14nm and tested with a Synopsys flow show whole-NoC stuck-at coverage of 96.53% for the refined v2 solution with only a marginal ~2 IO pin overhead (and 88 ATPG patterns). The paper also quantifies costs: unoptimized overheads are reported as ~2.6× area, ~1.9× performance impact, and up to ~2× power, with more detailed breakdowns showing v2 trading higher combinational area/timing penalties for a realistic top-level test interface. Overall, it demonstrates that bundled-data asynchronous NoCs can be brought into mainstream production test flows without custom DFT infrastructures, at a measured and explicitly reported implementation cost.

- **Efficient TinyML Inference on a Fault-Tolerant RISC-V SoC with Vector Extension [7]**

  This work was presented at the 10th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI 2025) and evaluates the inference performance of a quantized convolutional neural network on HARV-SoC, a fault-tolerant RISC-V System-on-Chip with vector extension support. The SoC features a port of TensorFlow Lite for Microcontrollers, which includes accelerated vectorized convolution functions, enabling data-level parallelism while preserving reliability mechanisms such as TMR and ECC. Inference was performed directly on the target platform, supporting near-sensor computing and low-latency execution in constrained and reliability-critical environments.

  The study compares RGB and grayscale input formats to analyze how input structure affects vectorization efficiency. Two vectorized versions of the convolution kernel were implemented to match the memory layout of single-channel and multi-channel inputs. Results show that, compared to the original scalar implementation, the vectorized versions achieved speedups of 1.80 times for RGB inputs and 2.05 times for grayscale inputs.

3.3 STA-Based Fault Analysis and Optimization

3.3.1 Overall Progress

Notable progress has been made in extending STA-based methodologies to support efficient and scalable reliability analysis for large-scale digital designs. The enhanced modeling framework enables the evaluation of radiation-induced transient fault mechanisms, including combined fault scenarios, while maintaining compatibility with standard industrial EDA flows. Furthermore, optimization techniques are applied to enhance circuit robustness by implementing fault-tolerance mechanisms while considering performance, power, and area (PPA) constraints and leveraging the analysis results.

3.3.2 Description of Work Conducted

- **UPSET: A Comprehensive Probabilistic SET Analysis Flow for VLSI Circuits using STA [16]**
  This journal paper extends the original UPSET conference publication by adding three major novelties that make the overall SET-analysis flow more complete and less pessimistic. First, it incorporates *timing-window masking* into the probabilistic analysis, i.e., it models whether a propagated SET that reaches a sequential endpoint is actually latched depending on its pulse width, the setup/hold latching window, and the clock period (a probabilistic latching formulation). This addition upgrades the method from “can a glitch reach an endpoint?” to “what is the probability it becomes a real SEU via latching?”, which is critical for system-level reliability reporting.

  Second, the paper introduces the *Electrical Masking Window (EMW)* criterion to improve electrical masking decisions in an STA-based setting where signals are implicitly treated as full-swing. EMW uses only timing descriptors (arrival/transition times) and flags pulses as electrically filtered when the input closing edge arrives no later than the output opening edge (EMW ≤ 0), complementing the classic pulse-width-to-zero rule that can miss non-full-rail attenuation—especially through reconvergent logic. In the large experimental campaign, enabling EMW reduces pessimism in the sensitivity metrics across most benchmarks; the paper reports average reductions on the order of ~17–22% for ASET/LASET and ~25% for APW depending on mode, producing tighter upper bounds while remaining scalable.

  Third, compared to the original work, this article provides substantially more implementation-level detail and validation: it presents detailed algorithms for crucial flow components (e.g., reconvergence handling in Vanilla vs. TimeStamp STA modes, and explicit Boolean/timestamp evaluation procedures), and it broadens the experimental analysis well beyond a small set of examples. This added algorithmic/implementation transparency supports EU open-science/FAIR goals by improving reproducibility and practical reusability of the method across teams and toolflows. The paper includes correlation against SPICE (reporting ~4.56% average pulse-width error at endpoints in the TimeStamp mode after derating, alongside >25,000× speedup in featured benchmarks) and a more comprehensive evaluation across 50 benchmarks of varying complexity, including sensitivity-metric trends and runtime breakdowns with/without EMW.

- **STA-Based Single Event Transient Propagation in Advanced Technology Nodes [13]**

This paper accepted at the 31st IEEE European Test Symposium (ETS 2026) extends STA-based SET analysis by systematically upgrading and then quantifying the impact of timing and interconnect modeling choices on SET propagation accuracy in advanced nodes. Using UPSET as the analysis backbone, it performs a correlation study against SPICE across combinations of cell-delay models (NLDM vs. CCS) and interconnect abstractions (Lumped-RC vs. pi-model), motivated by the fact that in sub-20 nm technologies effects like the Miller capacitance and resistive shielding increasingly dominate transient behavior and are not well captured by simpler STA abstractions. The work positions these choices as key determinants of whether STA-based SET propagation remains predictive when moving from mature to highly scaled processes.

Methodologically, the paper introduces a more "waveform-aware" propagation flow within STA, by proposing CCS timing (current-source waveforms and receiver Miller effect modeling) and pi-model interconnect representation. It describes how to make these usable for SET propagation by converting CCS current vectors into voltage waveforms (via numerical integration) and by applying dynamic/effective capacitance concepts to reflect distributed RC behavior during the transition. For NLDM + pi-model it adopts an iterative, segmented (piecewise-linear) waveform reconstruction that updates region-specific dynamic capacitances to reduce NLDM pessimism under distributed interconnect loading. It also presents an automated STA vs SPICE correlation/validation flow. In this flow, a SPICE deck for the SET traversed logic cone is automatically created, including side-input assignments chosen to enable propagation and interconnect wire RC parasitics at each node of the cone. The UPSET-generated SET pulses are used as PWL input voltage sources, and stage-by-stage comparison of arrival, slew, pulse-width, and voltage extrema is performed between the SPICE simulator and UPSET.

Experimentally, the paper validates these modeling choices across three technology nodes (IHP 130 nm, ASAP7 7 nm, and an IMEC 2 nm PDK) on buffer/inverter chains and ISCAS85-derived logic cones (c499, c1908), using Cadence Spectre as the SPICE reference. Results indicate that pi-model representation generally improves correlation in interconnect-dominated cases (e.g., reducing slew/pulse-width errors by capturing resistive shielding effect), and CCS tends to improve arrival-time accuracy particularly in advanced nodes (notably ASAP7), albeit with a runtime trade-off versus simpler NLDM + Lumped-RC configurations. The paper explicitly frames these outcomes as practical guidance on how to select STA models to trade speed for SPICE-correlated realism in SET vulnerability prediction.

- **Extension of UPSET to support Single Event Upset (SEU) Analysis [publication WIP]**
  The work-in-progress extends UPSET with a dedicated SEU (Single Event Upset) observability analysis for gate-level designs, complementing the tool's existing SET-focused capabilities. The new flow models an SEU as a bit-flip at an internal flip-flop (FF) outputs and estimates the probability that this fault becomes observable at architectural observation points, specifically primary outputs (POs) and FF inputs in the forward logic cone. This allows designers to rank FFs by their likelihood of producing an error at system-visible endpoints. This probability-driven view aligns with UPSET's broader probabilistic philosophy (e.g., using activity-derived probabilities rather than exhaustive vector simulation) and is compatible with industrial flows where switching activity is already available.

  Methodologically, the analysis is based on Boolean derivative principles: the Boolean derivative of an endpoint function with respect to a candidate fault site captures whether toggling that site

can affect the endpoint under a given input condition, i.e., whether the fault can propagate logically. To make this scalable and exact at the logic level, the implementation uses Binary Decision Diagrams (BDDs) to represent the relevant Boolean functions/derivatives and to compute observability probabilities efficiently over the input space (or equivalently, under a probability distribution). Endpoint and internal signal probabilities required by the probabilistic computation are provided either by a SAIF file (activity extracted from simulation/emulation) or as user-defined probabilities, mirroring UPSET's existing support for importing static probabilities from SAIF or specifying them at key starting points.

Practically, the outcome of the work is an automated SEU criticality metric per candidate node (or per region), defined as the probability that an SEU at that node is observable at POs/FF inputs, enabling targeted hardening (e.g., selective redundancy, gate-level protection, or cone restructuring) where it matters most. Because the method is BDD-based, it can provide exact logical propagation conditions while avoiding brute-force fault injection, and because probabilities are sourced from SAIF or user constraints, it can be tuned to realistic workloads rather than assuming uniform random inputs.

- **UPSET SET Optimizations [publication WIP]**

UPSET has evolved from a tool focused mainly on STA-driven SET assessment into a platform that also supports robustness-oriented optimization at the gate level, explicitly accounting for the resulting performance and area impacts. The latest version can apply a broad set of netlist-level transformations to harden circuits against radiation-induced transients. These include conventional sizing and structure edits (e.g., pin assignment, gate resizing, intentional load unbalancing, and fan-out decomposition) as well as resilience mechanisms based on redundancy or pulse attenuation, such as selective TMR, SET filters, and cascaded inverter structures. The workflow is designed to be flexible: users can target these techniques to selected regions of a design rather than applying blanket hardening across the whole circuit.

On top of these individual actions, we have implemented an initial prototype of an automated, closed-loop optimization flow. In each iteration, UPSET runs SET analysis to identify and rank the most critical gates and nets, then chooses and applies candidate hardening actions subject to user-specified constraints, and finally reassesses the design to quantify the impact. The loop continues until either the desired reduction in sensitivity is achieved or the optimization violates timing/area limits, enabling systematic exploration of "what works where" and how localized edits accumulate into circuit-level reliability gains.

Early results on representative benchmark circuits indicate that this optimization flow can substantially reduce SET sensitivity, while also making the associated PPA trade-offs explicit. In the current configuration, the loop achieves average improvements of roughly 41% reduction in ASET and 53% reduction in APW across the evaluated designs, at the cost of about 12% mean area overhead and around 40% performance degradation. These outcomes underline the need for stronger multi-objective optimization to balance robustness against PPA more effectively . In the next reporting period of TWIN-RELECT, we plan to enhance the loop with improved cost functions for tighter control of timing and area, broaden the experimental evaluation, and

consolidate the methodology and results into a peer-reviewed conference submission.

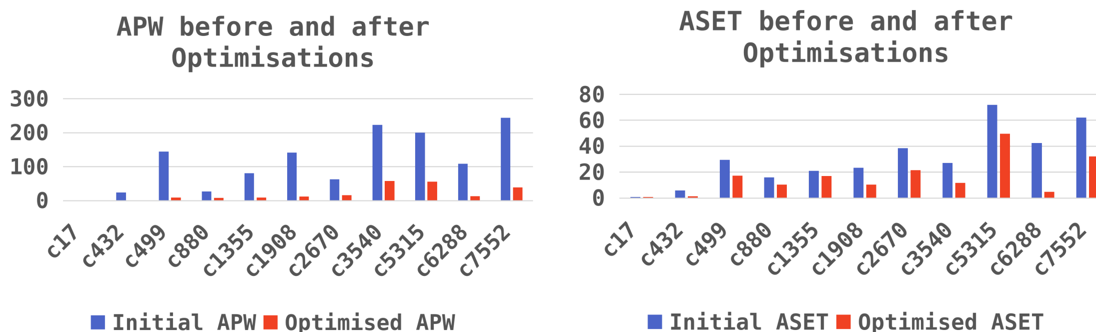

Figure 10: Preliminary results of UPSET SET optimization on ISCAS85

- **Layout-Based SET Generation & Propagation [publication WIP]**

  This work, as previously noted, constitutes a significant optimization of the UPSET reliability analysis tool, extending its methodology to support the modeling of SEMTs. The enhanced UPSET framework incorporates layout-aware information to model radiation particles as localized physical events, enabling the simultaneous impact on multiple neighboring logic components. Another key aspect of this analysis will be the partitioning of each circuit layout into grids (sub-circuits), allowing particle hits to be injected into specific regions of the design. As described previously, all components located within the affected area will be considered concurrently affected, generating SEMTs whose propagation will be analyzed using UPSET's existing timing-aware infrastructure. This grid-based SEMT modeling will enhance the efficiency of the analysis, enabling more accurate identification of susceptible regions and generally more reliable estimation of modern ICs' vulnerability.

4. Collaboration, Joint Research Outcomes, and Future Steps

4.1 Partner Synergies and Knowledge Exchange

A strong and efficient synergy among the partners exchanging their expertise and knowledge to address reliability challenges across multiple abstraction levels comprises a primary element. The joint research activities have been structured to promote continuous knowledge exchange between partners specializing in experimental characterization, physics-based modeling, circuit and gate-level analysis, EDA tool development, and application-driven system evaluation. The UTH, as WP1 leader, plays a coordinating role in integrating the contributions of all partners within a unified reliability analysis and optimization framework. This role is supported by close collaboration with CNRS, which contributes expertise in radiation effects, irradiation experiments, and TCAD-based modeling; IHP, which provides in-depth knowledge in standard-cell characterization, SPICE-level simulations, and reliability-aware modeling; and the MAN, which contributes application-specific circuits and system-level perspectives, particularly in AI accelerators and asynchronous designs.

The joint multi-partner paper [1] was accepted at the 28th Design Automation and Test in Europe Conference (DATE 2025) conference and constitutes the first collaborative research work of the TWIN-RELECT project. This work presents the scientific vision and joint research goals of the TWIN-RELECT project, with a focus on cross-layer reliability analysis and reliability-aware EDA tool flows. It summarizes the main research challenges handled in WP1, including STA-based analysis and optimization, fault modeling, and integration of various reliability techniques.

4.2 Joint Publications

Several conference papers have already been published or accepted during the first half of the project, as summarized in Tables 1 and 2. In particular, the consortium achieved strong visibility, with 14 conference papers presented/accepted at high-impact IEEE venues such as DATE 2025, SMACD 2025, ASYNC 2025, and DFTS 2025, and 3 journal articles already published in major journals. Additionally, two conference papers and two journals have already been submitted by the consortium and are pending peer review. Generally, these outcomes highlight the effective collaboration among partners and contribute significantly to knowledge transfer within the consortium.

These works present both methodological and application-oriented contributions, ranging from high-level overviews of the TWIN-RELECT project objectives and research directions to detailed studies on SET generation, propagation, and mitigation. Notably, collaborative papers involving multiple partners demonstrate the integration of experimental characterization, physics-based modeling, and EDA-level analysis techniques, validating the cross-layer approach promoted in WP1. In parallel, a number of works focus on the development of compact and scalable fault models, including charge collection and SER estimation techniques, enabling fast reliability analysis of large-scale designs. These contributions directly support the STA-based analysis and optimization engines developed within WP1.4 and WP1.5, and provide a solid foundation for tool-flow integration and validation activities. Beyond published and accepted papers listed in Tables 1 and 2, several works are currently under preparation or work-in-progress (WIP), targeting upcoming international conferences and journal submissions. These

ongoing efforts address advanced topics such as layout-aware SET generation and propagation, reliability-driven optimizations, and extensions of fault analysis to clock networks and asynchronous designs. Furthermore, the UPSET framework is being extended to support SEU analysis and the integration of various optimization techniques, enabling a more comprehensive reliability evaluation across different fault mechanisms, as well as the further integration of partner-developed tools within a unified analysis flow. Further developments include the integration of aging models to account for long-term degradation effects and their impact on circuit robustness. Overall, these activities aim to consolidate the outcomes into mature, high-impact scientific contributions while establishing the foundation for future collaborative developments and publications in the next project phase.

No.	Paper Title	Status	Conf.
1	Multi-Partner Project: Twinning for Excellence in Reliable Electronics (TWIN-RELECT)	Published	DATE 2025
2	Prediction of Single Event Transient Propagation Using Machine Learning Models	Published	SMACD 2025
3	Simulation Methodologies and Experiments for Reliability Analysis of Devices in Radiation Harsh Environments	Published	DFTS 2025
4	Compact SER Models for Line-Source-Induced Charge Collection Using Model Order Reduction	Published	DFTS 2025
5	Fault Injection Attacks Based on Layout-Driven SER Analysis	Published	SMACD 2025
6	Compact SER Models via Model Order Reduction of Diffusion-Based Charge Collection	Published	SMACD 2025
7	Efficient TinyML Inference on a Fault-Tolerant RISC-V SoC with Vector Extension	Published	IWASI 2025
8	A Synthesis Toolflow for the Predictable Implementation of High-Performance Bundled-Data Asynchronous NoCs on FPGA	Published	ASYNC 2025
9	Post-Placement Timing Optimisations on Asynchronous Designs	Published	ASYNC 2025
10	Resilience Analysis of a Fault-Tolerant MPSoC Interconnection Architecture under SEU Fault Injection	Accepted	LATS 2026
11	Characterization of a Fault-Tolerant RISC-V SoC in an SRAM-based FPGA under Proton Irradiation	Accepted	LATS 2026
12	Design and Reliability Analysis of a Pipeline RISC-V Processor Core	Accepted	LATS 2026
13	STA-Based Single Event Transient Propagation in Advanced Technology Nodes	Accepted	ETS 2026
14	Machine Learning Approach for Cross-Technology Prediction of the Generated Single Event Transient	Accepted	ETS 2026
15	On-Chip Reliability Sensor Analysis Under Combined Effects of Aging and Power-Supply Noise	Submitted	DDECS 2026
16	A Test Architecture for Bundled-Data Asynchronous NoC Switches Using Commercial ATPG Tools	Submitted	ASYNC 2026

Table 1: Conference Papers

No.	Journal Title	Status	Journal
1	UPSET: A Comprehensive Probabilistic SET Analysis Flow for VLSI Circuits using STA	Published	MDPI/ Electronics
2	Implementation and Evaluation of a Sensitivity-aware Hardware Trojan for SET-induced Soft Error Rate	Published	MDPI/ Electronics
3	An Ultra-Low Cost and Multicast-Enabled Asynchronous NoC for Neuromorphic Edge	Published	JETCAS

No.	Journal Title	Status	Journal
	Computing		
4	Reliability Analysis of Clock Networks under Radiation-Induced Transients Using Custom Simulation Tools	Submitted	MICPRO
5	Temperature-Aware Compact SER Modeling Using Model Order Reduction	Submitted	MICPRO

Table 2: Journal Publications

5. Conclusions

Deliverable D1.2 presents the methodologies and tools developed within the framework of Joint Research in the TWIN-RELECT project, reporting the initial outcomes achieved through the strategic collaboration between UTH and the advanced partner institutions. The activities described in this deliverable directly contribute to the objective of TWIN-RELECT, which is to strengthen the scientific and innovation capacity of UTH in designing reliable electronic systems. For this reason, WP1 focuses on the establishment of a cross-layer tool-flow methodology for the analysis and enhancement of reliability in ICs. Therefore, the proposed methodology supports the modeling, analysis, and mitigation of reliability effects in custom digital designs, addressing multiple abstraction levels and implementing optimization techniques. UTH has a major role in the coordination and integration of joint research activities, leading this process through strategic networking with the advanced partners.

5.1 Summary of Achievements

The primary target of the TWIN-RELECT project, beyond its specific technical purposes, is to contribute to the more comprehensive improvement of reliability-aware electronic system design through active knowledge exchange, strengthened collaboration among highly experienced partners, and the dissemination of research progress via publications in international conferences and journals.

Through the works presented in the previous sections, a significant joint scientific advance has been achieved, directly aligned with the defined research objectives. These approaches have led to a comprehensive analysis and accurate modeling of both transient and permanent effects, including effects caused by soft error, aging phenomena, and the combination of HTs with SETs. Furthermore, for efficient fault generation, propagation analysis, and fast reliability assessment in large-scale digital designs, STA-based analysis methods and ML techniques have been thoroughly investigated. Therefore, these research studies have resulted in published and submitted works on compact modeling of SET generation and propagation, layout-driven SET analysis, combined fault-effect modeling, efficient charge-collection modeling approaches, and prediction of fault behavior using ML methods for advanced technology nodes. Finally, reliability optimization and fault-tolerance techniques were designed and assessed for RISC-V architectures, MPSoCs, and NoCs, with validation performed via simulations, fault injection, and irradiation experiments.

5.2 Next Milestones and Long-Term Research Outlook

Future research activities will focus on extending the TWIN-RELECT project objectives to more comprehensive and scalable reliability analysis and optimization. The integration of aging-aware timing

characterization into STA engines to evaluate long-term degradation effects and their interaction with SET propagation constitutes a key direction. In parallel, the UPSET framework will be further enhanced to support advanced gate-level optimization and automated closed-loop hardening flows, enabling multi-objective balancing between radiation robustness and PPA constraints. Additional developments will address layout-aware modeling of SEMTs, combining grid-based particle injection and localized fault analysis to improve accuracy and scalability. Our goal is to integrate the current and future methods into the proposed unified, cross-layer TWIN-RELECT EDA flow, facilitating the accurate reliability assessment across the physical, electrical, and logical design levels.

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