TWINRELECT

Twinning for excellence in reliable electronics

D5.1

DELIVERABLE REPORT

D5.1 1st Scientific Collaboration Strategy

WP5: Establishment of Sustainability Framework

TWINRELECT
TWINNING FOR EXCELLENCE IN RELIABLE ELECTRONICS

Document information

Deliverable/Title	D5.1 1st Scientific Collaboration Strategy	**Work Package**	WP5
Leading Partner	UTH	**Participating Partner(s)**	MAN, IHP, CNRS
Authors	Nikolaos Sketopoulos		
Editors	Christos Sotiriou, Marko Andjelkovic, Luigi Dilillo, Davide Bertozzi		
Deliverable Type	R	**Dissemination Level**	PU
Official Submission Date	M17 of Project	**Actual Submission Date**	

Document history				
Version	**Date**	**Description**	**Editors**	**Comments**
0.1	05/12/2025	Initial Draft	Nikolaos Sketopoulos	
0.2	07/12/2025	Extend Future Research Directions and Roadmap	Nikolaos Sketopoulos	
0.5	14/02/2026	Extend Future Research	Nikolaos Sketopoulos	
1.0	27/02/2026	Final Reviewed Version	All Authors & Editors	

Disclaimer

Funded by the European Union (Grant Agreement № 101160314). Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union. Neither the European Union nor the granting authority can be held responsible for them.

Contents

1. Introduction

The TWIN-RELECT project is the first EU-funded initiative coordinated by the research team of the University of Thessaly (UTH), establishing a cornerstone for future research project submissions and collaborations. Sustaining the research excellence achieved through the coordination of TWIN-RELECT is essential for both the UTH team and all project partners, ensuring that high research and management standards are maintained.

To secure the long-term sustainability of TWIN-RELECT's research achievements, the project partners—UTH, the Leibniz Institute for High Performance Microelectronics (IHP), the French National Centre for Scientific Research (CNRS), and the University of Manchester (MAN)—will undertake a series of actions before the project concludes. These actions aim to guarantee that the research efforts continue beyond the project's official end.

By establishing a well-structured collaboration framework that includes shared tool repositories, laboratory facilities, services, and expertise, the partners aim to pave the way for future joint activities in the field of reliable electronics. Furthermore, upon completing the TWIN-RELECT project and disseminating its outcomes, we expect that new partners will be attracted for participation in future research initiatives.

From the outset, one of the primary objectives of TWIN-RELECT has been to expand networking and research collaboration both among the existing partners and with external stakeholders—such as academic institutions, legal entities, SMEs, established companies, and other relevant actors.

Our plan is not only to continue research activities in reliable electronics—the core topic of TWIN-RELECT—but also to build strong collaborations across additional research areas pursued by the partners, and to broaden activities based on discussions with external entities and stakeholders. To achieve this, the partners have, since the first year of the project, initiated discussions, arranged face-to-face meetings, participated in events, and actively explored opportunities for future collaboration.

In this context, the UTH team—being among the primary beneficiaries of future collaborations and committed to maintaining its research excellence—has already begun developing a strategy for continued cooperation among the current project partners as well as with potential new partners.

2. Shared-Assets Repository

2.1 Digital Tools and Software

To enhance and assess the reliability of electronics throughout the TWIN-RELECT project, a range of tools will be used, improved, or newly developed. These tools, provided by different partners, will be integrated to form complete design and analysis flows.

The table below lists each tool along with the partner responsible for providing it. Some tools are already publicly available—or will be made publicly available—while others will remain accessible only to the project partners during and after the completion of TWIN-RELECT. The "Status" column specifies whether each tool, software package, or library is (or will be) publicly accessible or restricted to project partners even beyond the project's end.

Tool/Software/Library Name	Provider Partner	Status
UPSET	UTH	Publicly Available
130nm PDK	IHP	Under NDA or Publicly Available
EMBER	MAN & IHP	Publicly Available
PredicSEE	CNRS	Restricted to partners
ECORCE	CNRS	Restricted to partners
FsimNNs	IHP	Publicly Available

UPSET

UPSET is a Single Event Transient (SET) analysis tool developed at **UTH**, designed to model both SET generation and propagation across entire circuits using Static Timing Analysis (STA). The STA framework emulates signal propagation from all timing path startpoints through the combinational logic to the endpoints, accounting for both rise/fall delays and slews. It supports the standard NLDM (Non-Linear Delay Model) as well as the more advanced CCS (Composite Current Source) timing model. By leveraging UTH's STA engine for SET generation and propagation, UPSET is able to model transient faults caused by particle strikes with (i) only a modest reduction in accuracy compared to SPICE and (ii) a dramatic speedup by relying on static rather than simulation-based analysis. A key advantage of the tool is its compatibility with widely used industry formats—such as Verilog, SPEF, and LEF—which enables seamless integration into established EDA workflows. This interoperability facilitates efficient collaboration with commercial tool environments and supports straightforward adoption in industrial design processes.

Open Source PDK

IHP provides its complete suite of process design kits (PDKs) free of charge, including access to all proprietary technologies under NDA, enabling researchers and industry partners to design advanced mixed-signal, RF, and digital ICs using validated manufacturing processes. Complementing these offerings, IHP also distributes an **open-source PDK** for the SG13G2 130 nm BiCMOS technology, which

significantly broadens accessibility, supports reproducible research, and strengthens the impact of open hardware development within the European and global semiconductor ecosystem.

EMBER

EMBER (Extensible Microarchitectural Benchmark for Error Resilience) is a C++ class library for register-transfer-level (RTL) fault injection that strikes an effective balance between hardware modeling accuracy and simulation performance. Developed jointly by the **University of Manchester** and **IHP**, it supports cycle-based simulation and provides built-in mechanisms for injecting faults into parameterized designs. By assuming zero gate delays—effectively ignoring intra-cycle timing—EMBER enables cycle-based hardware simulation, which offers significantly higher performance than traditional event-driven approaches. The framework is designed for rapid resilience analysis of highly configurable microarchitectures. It extends the conventional RTL simulation flow with a *design initialization* phase, allowing changes in design parameters without requiring recompilation of the simulator. EMBER leverages C++ meta-programming techniques to decouple datapath descriptions from unit implementations, making architectural adaptation and exploration straightforward. Unlike traditional fault-injection techniques that rely on hardware or software saboteurs, EMBER employs *mutant components* whose behavior dynamically changes under fault injection. This approach avoids the need for intrusive modifications to the design or simulation environment, while supporting flexible and extensible fault models.

PredicSEE

PredicSEE is a Monte Carlo–based simulation tool, developed at **CNRS**, designed to predict the Single Event Upset (SEU) cross-section of electronic structures such as memory cells, logic gates, and small circuit blocks. By simulating the interaction between incident particles and semiconductor devices, PredicSEE evaluates the likelihood that a single ionizing particle will induce a bit flip or functional disturbance. The tool incorporates detailed physical models of charge generation, transport, and collection within the device, enabling accurate estimation of SEU sensitivity under different radiation environments and technology parameters. PredicSEE is particularly well suited for early-stage reliability assessment, allowing designers to compare device architectures, evaluate technology scaling effects, and estimate SEU susceptibility without requiring expensive irradiation experiments. Its Monte Carlo engine provides statistical robustness, generating predictive cross-sections that support the development of radiation-tolerant circuit designs and inform hardening strategies.

ECORCE

ECORCE is a TCAD simulation tool developed at **CNRS** and distributed under the GPL license. It is based on the classical drift–diffusion model and provides a user-friendly graphical interface that simplifies TCAD device modeling. Through this interface, users can define device geometry and physical models, run simulations, and analyze results. The tool also incorporates a dynamic mesh generator, eliminating the need for manual meshing in both DC and transient analyses. In addition to standard device modeling, ECORCE supports Single Event Effect (SEE) simulation and includes a restricted-diffusion add-on that captures the kinetics of charge trapping and detrapping in insulators. The tool is capable of modeling both the SEE and Total Ionizing Dose (TID) responses of MOS devices, offering quantitative agreement with experimental data.

FsimNNs Platform

FsimNNs is an open-source platform developed to accelerate simulation-based Single Event Upset (SEU) fault analysis using Spatio-Temporal Graph Neural Networks (STGNNs), addressing the significant computational cost typically associated with SEU fault injection in complex digital circuits. The platform

integrates three STGNN architectures specifically designed for reliability prediction in electronic systems, incorporating advanced deep learning components such as Atrous Spatial Pyramid Pooling and attention mechanisms to enhance spatio-temporal feature extraction from circuit activity graphs. By leveraging learning from simulation data, the models can accurately predict SEU fault simulation outcomes while substantially reducing computational overhead compared to exhaustive fault injection approaches. To facilitate training and benchmarking, the platform includes structured datasets derived from six open-source circuits of varying complexity, enabling comprehensive evaluation of predictive performance, scalability, and generalization capability. The tool supports training and evaluation of STGNN models for SEU prediction, comparative analysis across multiple circuit benchmarks, investigation of model generalization to unseen test cases within the same circuit, and performance assessment in cross-test scenarios. The complete implementation, trained models, and datasets are made publicly available to ensure reproducibility and to promote further research in reliability-aware machine learning for hardware systems.

All tools will be uploaded to the **Virtual Knowledge Platform (VKP)**, developed specifically for the TWIN-RELECT project, and will be accessible to all partners. The UTH team will be responsible for keeping the tools up to date by uploading newer versions to the VKP as they become available. For tools that are intended to be publicly accessible, each partner will be responsible for hosting the tool on a platform of its choice—such as GitHub—where the broader community will be able to access, use, and evaluate the corresponding software or library.

2.2 Laboratory Facilities, Services, and Support

CNRS/University of Montpellier IES Irradiation Facilities

During the TWIN-RELECT project, a strong and structured collaboration has been established between all partner institutions. A key element of this collaboration has been the introduction and integration of UTH personnel into the use of irradiation facilities, and more specifically the facilities hosted at the IES laboratory under the name **PRESERVE platform**. This platform hosts a Cobalt irradiator and an X-ray irradiator dedicated to Total Ionizing Dose (TID) tests, as well as two alpha-particle sources used for single-event effects (SEE) test campaigns. In the context of TWIN-RELECT, UTH personnel have received dedicated training for the access to, and safe and effective use of, these facilities, enabling them to actively participate in irradiation experiments and related research activities:

All TWIN-RELECT partners have expressed their intention to extend this collaboration on a stable and long-term basis beyond the duration of the TWIN-RELECT project. The aim is to pursue joint studies focused on the effects of radiation on electronic devices and systems, targeting aerospace applications as well as other radiation-sensitive domains. Within the framework of these collaborative research activities, the RADIAC team (CNRS) will propose access to the PRESERVE platform whenever such access is relevant and beneficial to the scientific objectives of the joint studies.

The PRESERVE platform has been developed and is operated by the RADIAC team. Consequently, the booking and access to the platform will be granted when the proposed irradiation test campaigns align with common research goals shared with RADIAC, and subject to the availability and scheduling constraints of the facility.

Laser Fault Injection Facilities at IHP

IHP owns an in-house developed setup for laser fault injection. The setup allows precise fault injection in manufactured chips, and is suitable for studying soft error and side channel attack effects. For research collaboration between the TWIN-RELECT project partners, the laser setup would be available free of charge. The setup is integrated into the Security Lab within the System Architectures Department. For use of the setup, an experimental plan would have to be provided to the responsible Lab personnel at least 3 months prior to the experiment. Details of the experiment should be well aligned with the research strategies of all involved partners.

Thermal Stress Facilities and Experiments at IHP

IHP owns a commercial thermal chamber suitable for performing aging experiments on manufactured chips. This chamber would be available free of charge for joint research collaboration between the TWIN-RELECT project partners. Booking of the experiment should be done at least 3 months in advance, by contacting directly the responsible personnel at IHP.

SpiNNaker Facilities from University of Manchester

During the TWIN-RELECT project, the University of Manchester (MAN) has played a key role in transferring technical and scientific knowledge in the field of neuromorphic computing, with a particular focus on the architectures and circuits relevant to this domain. As part of the training school held in Manchester, the project partners were exposed to a series of tutorials covering neuromorphic hardware and software platforms, as well as key challenges related to reliability analysis and fault tolerance in neuromorphic systems. The program also included the introduction of the large-scale neuromorphic supercomputer SpiNNaker, accompanied by a guided visit of the underlying infrastructure. This knowledge transfer enables the project partners to apply their existing tools and methodologies in a new application domain. To this end, MAN introduced the partners to the use of major open-source tools for the description and modeling of spiking neural networks, in particular PyNN and snnTorch. These are two frameworks, respectively targeting neuroscientific simulation and the training of spiking neural networks in a machine-learning context. It also provided access to the mapping framework of spiking networks onto the SpiNNaker platform. After the end of the project, MAN will continue to provide open access to its neuromorphic computing infrastructures and to its design and mapping tools to the project partners. While access to SpiNNaker is ensured through the EBRAINS 2.0 project, in which Manchester is a partner and commits to providing open access to the SpiNNaker infrastructure, and the modelling tools are available as open source, MANwill offer specific, non-generic support to the partners for concrete use cases, fostering collaboration on fault-tolerance issues in neuromorphic computing, which are becoming increasingly relevant given the growing adoption of neuromorphic vision in space and automotive applications.

PredicSEE and ECORCE Support

The tools PredicSEE and ECORCE that are currently proposed by the partner CNRS (IES), they will continue to be developed and available also after the end of TWIN-RELECT project with the following precisions:

- PredicSEE will be available through licenses released by the University of Montpellier. In case of scientific collaboration between RADIAC/IES/CNRS and UTH/IHP/MAN beyond the duration of project TWIN-RELECT, free of charge licenses could be released to UTH/IHP/MAN students.

- ECORCE will be available through licenses released by the company DELPHEA. In case of scientific collaboration among RADIAC (IES/CNRS team), DELPHEA and any of the TWIN-RELECT partners beyond the duration of project TWIN-RELECT, free of charge licenses could be released.

UPSET Support

The UPSET tool, proposed and developed by the partner UTH, will remain available and continue its development beyond the duration of the TWIN-RELECT project. Furthermore, UTH commits to providing technical support and bug fixing services to the project partners, ensuring long-term sustainability and reliability of the tool.

3. Future Research Directions

As outlined in the introduction, the TWIN-RELECT consortium aims to sustain and further expand the collaboration established during the project, both among the existing partners and with new collaborators working in the same research domain or in complementary fields. TWIN-RELECT has already provided multiple opportunities for face-to-face meetings through its completed events and will continue to do so in upcoming activities, enabling partners to connect with researchers from various institutions and explore new collaboration possibilities.

As a result, the consortium has developed both a short-term and a long-term plan to broaden its research activities, deepen its involvement in the field of reliable electronics, and explore emerging topics of mutual interest. In the short term, several proposals for new projects have already been submitted to European and national funding programmes.

The table below summarises the future research directions envisioned by the TWIN-RELECT partners for both the short- and long-term horizon.

Project Name	Field	TWIN-RELECT Partners Involved	Status	Project Duration (Months)
Open Design Environment for European Chips – Digital SoC Design	General Purpose Electronic Design Automation	IHP, UTH	Approved	36
Open Design Environment for European Chips - Analog and Mixed Signal	General Purpose Electronic Design Automation	IHP, UTH	Approved	36
NEXUS-AI	Edge AI	IHP, MAN, UTH	Under Review	60
RESYST-CHIP	Resilient SoCs	IHP, CNRS, MAN, UTH	Under Review	48

The research directions are presented in the next section. However, these directions may evolve, and new topics may be explored as the TWIN-RELECT project progresses. Likewise, additional partners may be included in future project proposals as new collaboration opportunities emerge.

3.1 Open Design Environment for European Chips – Digital SoC Design

Open-source EDA tools provide a powerful alternative to traditional proprietary design environments. They allow companies, universities, and independent teams to explore architectures, test design flows, and validate concepts without the heavy upfront investment normally required for commercial toolchains. Even when final signoff transitions to proprietary solutions, early-stage exploration becomes dramatically more accessible. In this way, open-source tools lower not only financial barriers but also

opportunity barriers, enabling a broader community of innovators to engage in microelectronics design without requiring the scale of a major semiconductor corporation.

Despite this potential, the European open-source EDA landscape remains fragmented. Tools are often developed in isolation, lack unified integration layers, and provide limited interoperability across the design stack. To reach industrial maturity, they must evolve from research prototypes into robust, scalable solutions that support mainstream process nodes, complete RTL-to-GDSII flows, advanced system-level packaging, and efficient cross-abstraction interoperability. Achieving this requires coordinated development, governance, shared benchmarks, and industrial-calibre validation. Without such coordination, progress risks remaining fragmented and misaligned with the strategic objectives of the European Chips Act.

Mission of Open Design Environment for European Chips – Digital SoC Design (ODE4EC-DIG)

ODE4EC-DIG aims to address these gaps by enabling researchers and SMEs across Europe to access cost-effective, open-source EDA tools and validated design flows. By reducing dependency on proprietary technologies and strengthening Europe's technological sovereignty, the project fosters innovation and lowers the entry barrier for digital SoC design at 65–28 nm nodes.

To ensure adoption and measurable progress, ODE4EC-DIG follows a staged scalability path, progressively validating capabilities at increasing complexity levels. This structured approach supports a controlled evolution from academic-scale prototypes to SME-scale, production-ready SoCs, ensuring robustness, trust, and industrial applicability.

Six technical domains form the backbone of the project's development strategy:

1. Tool integration, interoperability, and infrastructure
2. Design entry and high-level modeling
3. Improvements of core EDA tools
4. Physical integration and packaging
5. Validation and demonstration
6. Dissemination, training, and ecosystem development

These domains represent areas where coordinated, European-scale effort is essential to reduce fragmentation and deliver an end-to-end open-source design flow.

Key Partner Contributions: IHP and UTH

Within this framework, **IHP** and **UTH** play critical roles in strengthening Europe's open-source EDA foundation:

- **IHP** will develop the *first openly available Assembly Design Kit (ADK)* for heterogeneous and advanced packaging. This represents a transformative step for the open-source ecosystem, enabling for the first time the exploration, modeling, and validation of multi-die and system-in-package designs without proprietary restrictions. The ADK will provide open packaging rules, bonding constraints, interconnect models, and verification checks—filling one of the most

significant missing elements in today's open-source design landscape.

- **UTH** will contribute its existing and evolving suite of EDA tools, focusing on key timing and extraction capabilities that are essential at 65–28 nm. This includes the UTH Timer STA engine, the STA-to-SPICE interface, and a parasitic extraction flow built around field solvers such as FasterCap or Caplet. UTH will collaborate deeply with other tool developers within ODE4EC-DIG to enhance timing-driven synthesis, strengthen static timing analysis, improve parasitic extraction accuracy, and integrate these capabilities into the broader open-source flow. These contributions directly advance the project's goals for interoperability, accuracy, and cross-stage optimisation.

In ODE4EC-DIG, **IHP** and **UTH** will have the opportunity to collaborate with 26 additional partners from across Europe, significantly expanding their research network and impact. This achievement builds directly on the strong foundation established through their close collaboration in the TWIN-RELECT project, where the two institutions developed deep technical synergies and effective joint working practices. The trust, expertise, and coordination mechanisms formed in TWIN-RELECT now enable IHP and UTH to engage confidently in a much larger consortium and contribute meaningfully to a Europe-wide open-source EDA ecosystem.

3.2 Open Design Environment for European Chips - Analog and Mixed Signal

Open Design Environment for European Chips - Analog and Mixed Signal (ODE4EC-AMS) aims to unlock the full potential of open-source tools, flows, and frameworks for analogue–mixed-signal (AMS) design by addressing long-standing gaps in the current open-source EDA landscape. The project will deliver innovative methodologies tailored specifically to AMS ASIC development in mature technology nodes, fully aligned with the cross-cutting priorities of the ECS-SRIA and seamlessly integrated into the emerging European Design Platform envisioned by the Chips Act.

The urgency is clear: the productivity gap in analogue design is widening, while today's proprietary AMS frameworks—built on legacy methodologies and outdated software architectures—struggle with poor interoperability and limited compatibility with modern AI/ML-driven automation. ODE4EC-AMS responds to these structural bottlenecks through two complementary strategies:

1. Standardising the analogue design abstraction stack from device level to system level.
2. Developing an agile, modular infrastructure capable of supporting next-generation AI/ML-enabled EDA tools.

Mission and Ambition

Our mission is to close critical gaps in the open-source AMS design ecosystem and enable rapid, efficient ASIC development in mature nodes. Through seamless integration with emerging AI/ML capabilities, the project will enable on-the-fly exploration, optimisation, and innovation—creating a foundation for strengthened European leadership across the semiconductor value chain.

ODE4EC-AMS advances the next generation of open-source AMS design tools, methodologies, and IPs through 12 strategic objectives spanning the entire AMS design value chain. These objectives target:

1. Development of open-source AMS tools and PDKs,
2. Automation of analogue design workflows from circuit to system level, and
3. Creation of reusable IP libraries with hard macros and parameterised templates to enable scalable design reuse.

Key Contributions of IHP and UTH

As the **coordinator of ODE4EC-AMS**, **IHP** plays a central role in steering technical, scientific, and administrative success across the consortium. IHP shaping both the project's core technical outcomes and its long-term impact.

- IHP develops and maintains the open-source SG13G2 130 nm BiCMOS PDK, a cornerstone for enabling industrial-grade AMS design in mature nodes. IHP will integrate tool innovations emerging, ensure compatibility across the open-source ecosystem, and coordinate multiproject wafer runs to validate tools, flows, and IP. IHP also contributes to creating a vendor-independent middleware abstraction layer, ensuring robust tool interoperability and reducing dependence on proprietary infrastructure.

- IHP leads strategic outreach, academic and industrial engagement, and ecosystem building. This includes ensuring sustainability through a clear exploitation plan and aligning activities with broader European initiatives.

- IHP ensures efficient project coordination, financial oversight, risk management, and alignment with Chips JU and related consortia.

Complementing these efforts, **UTH** strengthens the analogue and RF design flow with advanced field-solver technologies. UTH will integrate and support a comprehensive set of field-solver back-ends for KLayout, including:

- FasterCap 2D (Boundary Element Method),
- FasterCap 2.5D (2D with conductor-height modelling),
- FasterCap 3D (full 3D BEM formulation), and
- 3D Floating Random Walk (FRW), a high-accuracy stochastic approach for complex geometries.

These solvers enable more accurate parasitic extraction, improved modelling fidelity, and tighter coupling between layout, device physics, and circuit simulation—essential capabilities for next-generation AMS methodologies.

A Strong Collaborative Foundation

ODE4EC-AMS also provides IHP and UTH with the opportunity to collaborate with more than two dozen European partners. Their close and effective collaboration in the TWIN-RELECT project has created a

strong technical and organisational foundation, now enabling them to lead and contribute confidently within a much larger European effort.

3.3 Edge AI for Agrifood Sustainability, Disaster Resilience, and Natural Resource Management

The proposed project seeks to elevate the scientific and institutional excellence of European higher education institutions (HEIs), with particular emphasis on Widening countries, by establishing a transformative framework for research, education, and governance in the field of Edge AI. Fully aligned with the ERA priorities of climate resilience and digital transformation, the initiative recognises that the ability to conduct AI-enhanced, resource-efficient, and locally relevant research is now a defining factor for competitiveness, technological sovereignty, and inclusive societal progress. The project's guiding ethos—diversity, sustainability, openness, and responsible research culture—ensures that all activities contribute to a fair, human-centred research and innovation ecosystem in line with the objectives of the European Excellence Initiative.

The initiative targets three interlinked societal domains that are both high priority for Europe and particularly relevant for the participating regions: agrifood sustainability, disaster resilience, and natural resource management. These domains serve as living laboratories where institutions can test new methodologies, strengthen interdisciplinary collaboration, and apply Edge AI solutions to real-world challenges. The project is structured around a dual-axis transformation model. The first axis strengthens joint Research & Innovation (R&I) capacities by activating shared research infrastructures, promoting scientific co-creation, and fostering excellence across disciplines. The second axis embeds modern management practices and open-science governance within participating institutions to ensure that scientific capacity building results in durable structural change and organisational renewal.

This proposal has been formally submitted and is currently pending evaluation. Its consortium unites six institutions whose collaboration reflects both continuity and strategic expansion. **IHP, the University of Manchester (MAN), and the University of Thessaly (UTH)**—all partners in the TWIN-RELECT project—serve as the core scientific drivers of the initiative. Their established cooperation and shared experience in strengthening research excellence provide a solid foundation for the proposed Edge AI transformation.

In addition, the consortium includes **Tallinn University of Technology** and the **University of Niš with its Faculty of Electronic Engineering**, two institutions leading the Twinning projects **TAICHIP** and **AIDA4Edge**, respectively. UTH became aware of their complementary expertise and ongoing efforts through the dissemination and networking activities of TWIN-RELECT, TAICHIP, and AIDA4Edge. These interactions enabled the formation of a broader, well-aligned partnership that connects multiple European capacity-building initiatives into a coherent effort.

Together, the partners aim to establish a forward-looking framework that advances research excellence, accelerates institutional modernisation, and ensures long-term sustainability in Edge AI capabilities.

More detailed information about the project will be released following the official evaluation and acceptance of the proposal.

3.4 RESYST-CHIP

Reliable electronics is essential in safety- and mission-critical domains, such as space missions, aviation, automotive, wireless communications, data centers, healthcare, and the automated industry. With increase in complexity of Integrated Circuit (ICs), advancement in semiconductor technology and evolving market trends and application requirements, the IC design paradigm is shifting from classic "reliable systems" to "resilient systems". A resilient IC has the ability to monitor its own state, detect and predict faulty scenarios, and perform self-reconfiguration/self-healing to maintain the required functionality. Besides ensuring enhanced reliability and safety, resilient systems aim to provide a balance between performance, fault tolerance and power consumption, resulting in extended system lifetime. Given the strategic goal of the EU to enhance its capacities in the semiconductor domain (European Chips Act), as well as the shortage of highly skilled personnel for IC design, there is an urgent need for creating a new generation of skilled experts for ICs design. As the demand for safety- and mission-critical applications is projected to increase in coming years, particularly with new space missions and adoption of 6G wireless communications across numerous domains, special attention should be given to boosting the European capacities in the design of resilient Systems-on-Chip (SoC).

The RESYST-CHIP project was submitted for Marie Skłodowska-Curie Actions (MSCA) funding and aims to train 15 highly skilled and entrepreneurially oriented researchers in the design of resilient Systems-on-Chip (SoCs). The project brings together 20 leading research institutes, universities, and companies, including **all partners of the TWIN-RELECT project**, **with IHP as the coordinating institution**. Its objective is to synergistically address the critical challenges across four research domains: reliability characterization and modeling, CAD tools for resilience-by-design, on-chip sensing and analytics, and the design of resilient architectures. The RESYST-CHIP network will implement a comprehensive training program that combines advanced scientific training with complementary transferable skills development.

More detailed information about the project will be released following the official evaluation and acceptance of the proposal.

4. Roadmap

Based on the submitted project proposals described in the previous section, Figure 1 illustrates the expected roadmap of the joint initiatives planned by the TWIN-RELECT partners. The exact start and end dates of these projects are not yet known at the time of writing this document; however, the estimated timelines are based on discussions with the respective coordinators and on the partners' prior experience with similar projects.

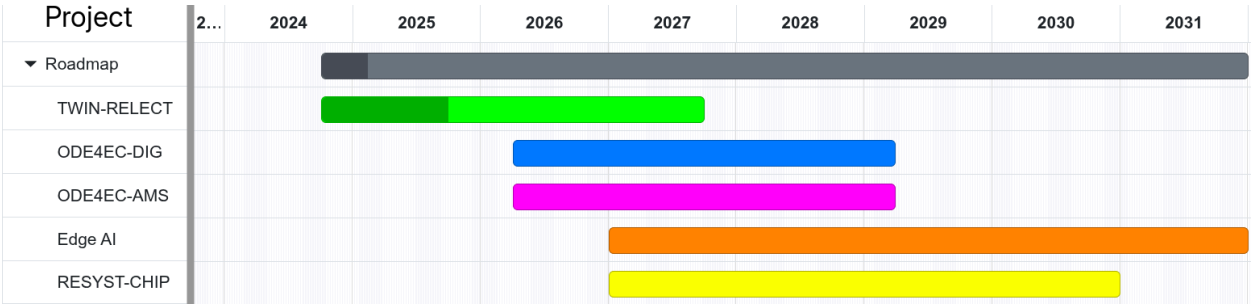

Figure 1: Gantt chart of future collaborative projects roadmap.

Note that projects which have not yet been submitted do not appear in the Gantt chart, as their dates, duration, and feasibility have not yet been defined. Furthermore, some of the research directions described in the previous section are not intended to be submitted as project proposals; instead, they are expected to be pursued as joint research activities during or after the completion of the TWIN-RELECT project by researchers from the participating institutes.

5. Conclusions

The TWIN-RELECT project has laid a solid foundation for strengthening collaboration and advancing research excellence in reliable electronics across all partner institutions. A key enabler of this progress is the comprehensive suite of tools that have been used, refined, or newly developed throughout the project. These tools, contributed by different partners and integrated into complete design and analysis flows, form a critical technical backbone supporting the project's objectives. Their varying levels of availability, whether publicly accessible or restricted to project partners, ensure both wide dissemination where appropriate and protected collaboration where necessary.

To facilitate long-term accessibility and collaborative use, all tools will be uploaded to the Virtual Knowledge Platform (VKP), the central repository developed specifically for TWIN-RELECT. UTH will maintain and update this platform, ensuring that partners always have access to the latest versions. For tools intended for public release, each contributing partner will publish and maintain them on platforms such as GitHub, enabling the broader scientific and industrial community to evaluate, adopt, and build upon the project's outputs.

Beyond these immediate outcomes, TWIN-RELECT has also fostered strong collaborative relationships that continue to expand. Through its workshops, meetings, and dissemination activities, the project has created multiple opportunities for partners to engage with new research groups and explore potential synergies. This has already resulted in the development of both short- and long-term plans for joint research activities. Several proposals for new national and European projects have been submitted, reflecting the consortium's commitment to deepening expertise in reliable electronics and branching into new, interdisciplinary domains. Additional research directions, some formalised as proposal ideas, will continue to evolve during and after the project.

Ultimately, TWIN-RELECT has achieved far more than its initial technical goals; it has created a sustainable and outward-looking ecosystem of collaboration. The consortium is now well positioned to maintain and expand the research excellence achieved during the project, guided by a shared vision of innovation, openness, and long-term scientific impact.