# Design and Validation of Chips for Space Applications

TWIN-Relect

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# Agenda

1. Motivation
2. Radiation Effects
3. Addressing SEEs in Digital Systems
4. Optimizing Overhead in Space Applications
5. Design Examples
6. Conclusions

# Motivation and goals

- Space applications are imposed with additional requirements, not so critical in traditional application domain
- Temperature: temperature range is extended -55° - +125°
- Reliability: depending on the mission requirements could be even 15 or 20 years
- Radiation hardness and tolerance: immunity against radiation effects
- As a consequence additional design steps are required to fulfil the requirements
- The design methods enhancing radiation hardness are known as radiation hardness by design (RHBD), and are usually based on fault tolerance
  - Fault tolerance is always achieved with some (significant!) cost
- How to limit the overhead imposed by fault tolerance?
  - Advanced static low-overhead techniques which provide certain level of fault tolerance with limited overhead
  - Adaptivity techniques which enable fault tolerance only when required

# Effects induced by Radiation

Radiation effects are present not just in space applications

Radiation effects can be split in two general categories:

**Cumulative Effects**

- Ionization
- Displacement (can also be caused by aging effects)
- Enhanced low-dose-Rate Sensitivity (ELDRS)

**Single Event Effects**

**Soft errors:**
- Neutron Single Event Upset (NSEU)
- *Single Event Transient (SET)*
- *Single Event Upset (SEU)*
- *Single Event Functional Interrupt (SEFI)*

**Hard errors:**
- Single Event Latchup (SEL)
- Single Event Gate Rupture (SEGR)
- Single Event Burnout (SEBR)

The effects need to be addressed by corresponding measures

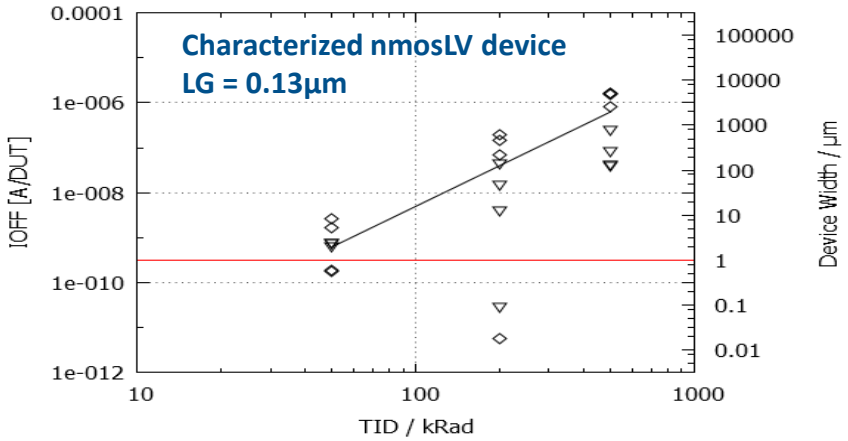
# Cumulative Effects and Ways against them

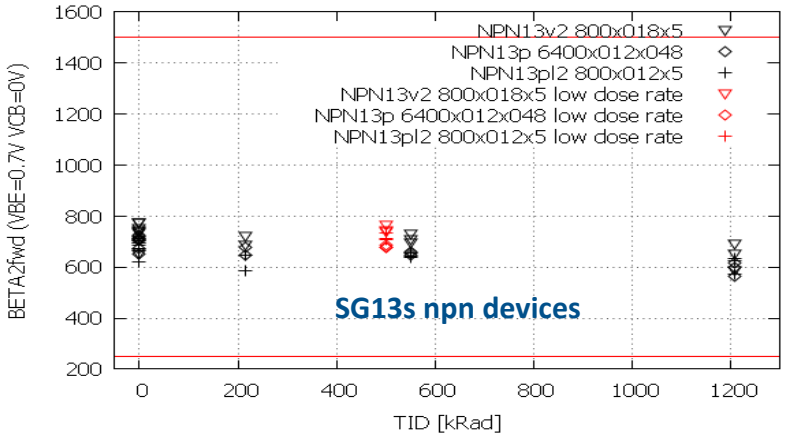
- Cumulative effects affect the parametric changes of the transistors (increase of leakage current, change of threshold voltage, reduction of transistor amplification etc.).
  - After total dose accumulation the system may reach the state outside of the specified functional range.
  - Due to the reduced performance of the transistors the respective faults may appear (timing faults for example)

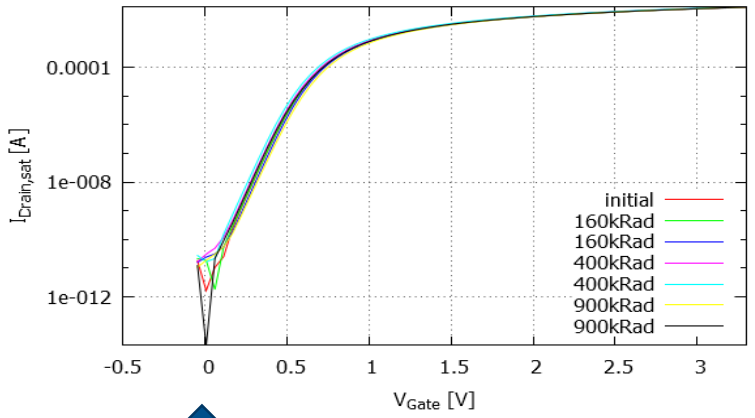
- Cumulative effects are usually addressed:
  - at the level of technology
  - by using specific hardened devices (ELT – enclosed layout transistor, JIC – junction isolated circuit)
  - by using the transistor sizing (bigger transistors are less prone to the parametric changes)

- Online methods could be used for the detection of the changes

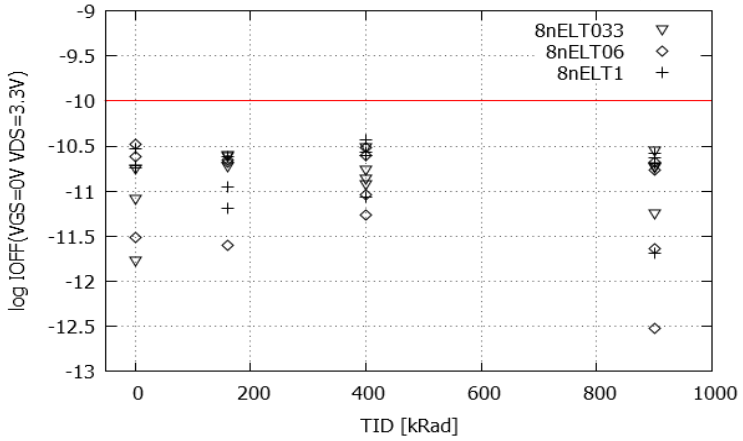
# TiD Example: Radiation Assessment of SG13RH



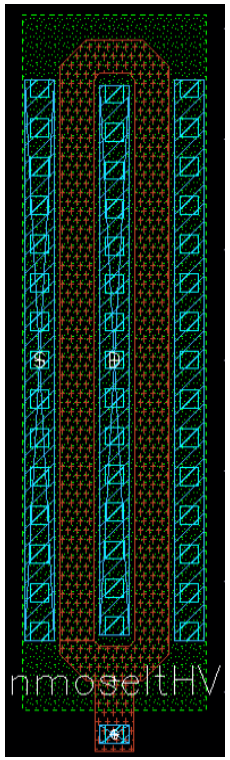




**nmoseltHV device**




**ELT-nmos**
**Edgeless transistor**
**RHBD**

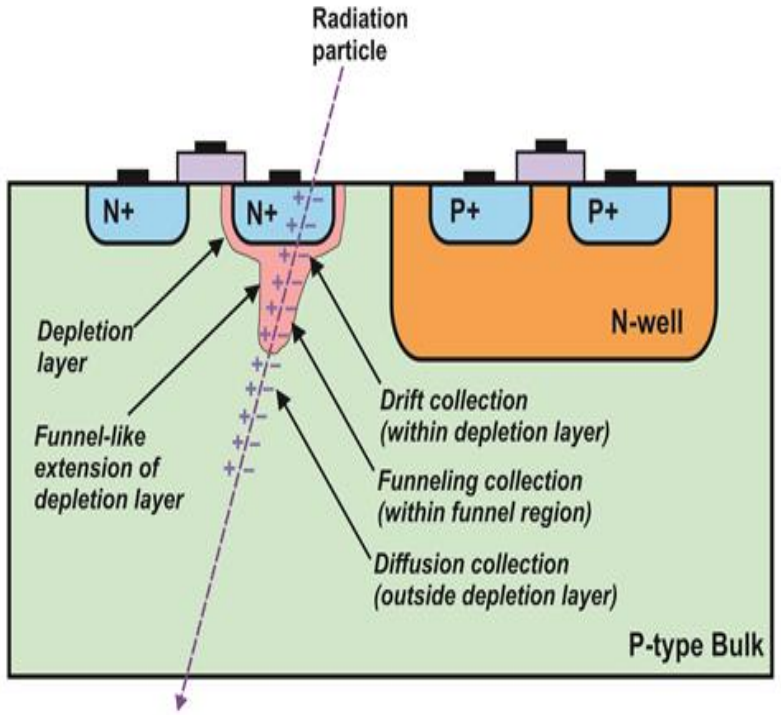


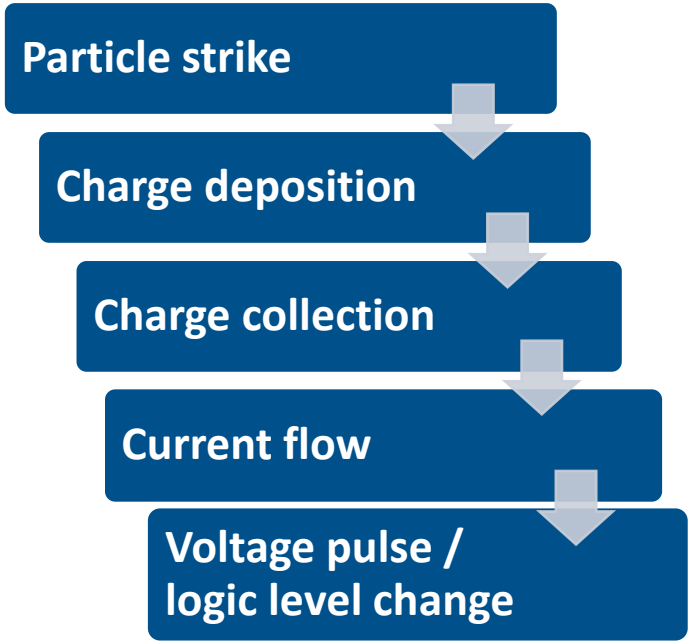

**Radiation Source :** Helmholtz-Zentrum Berlin für Materialien und Energie GmbH, Berlin. Gamma rays provided by $Co^{60}$ source. Dosimetry performed by Farmer Ionization Chamber, nominal photon energy range from 60kV to 50MV.

**Test Hardware :** Keithley SCS-4200 Semiconductor Parameter Analyzer with Keithley 707B Switch Matrix  Custom IHP  Test Fixtures for measurements.

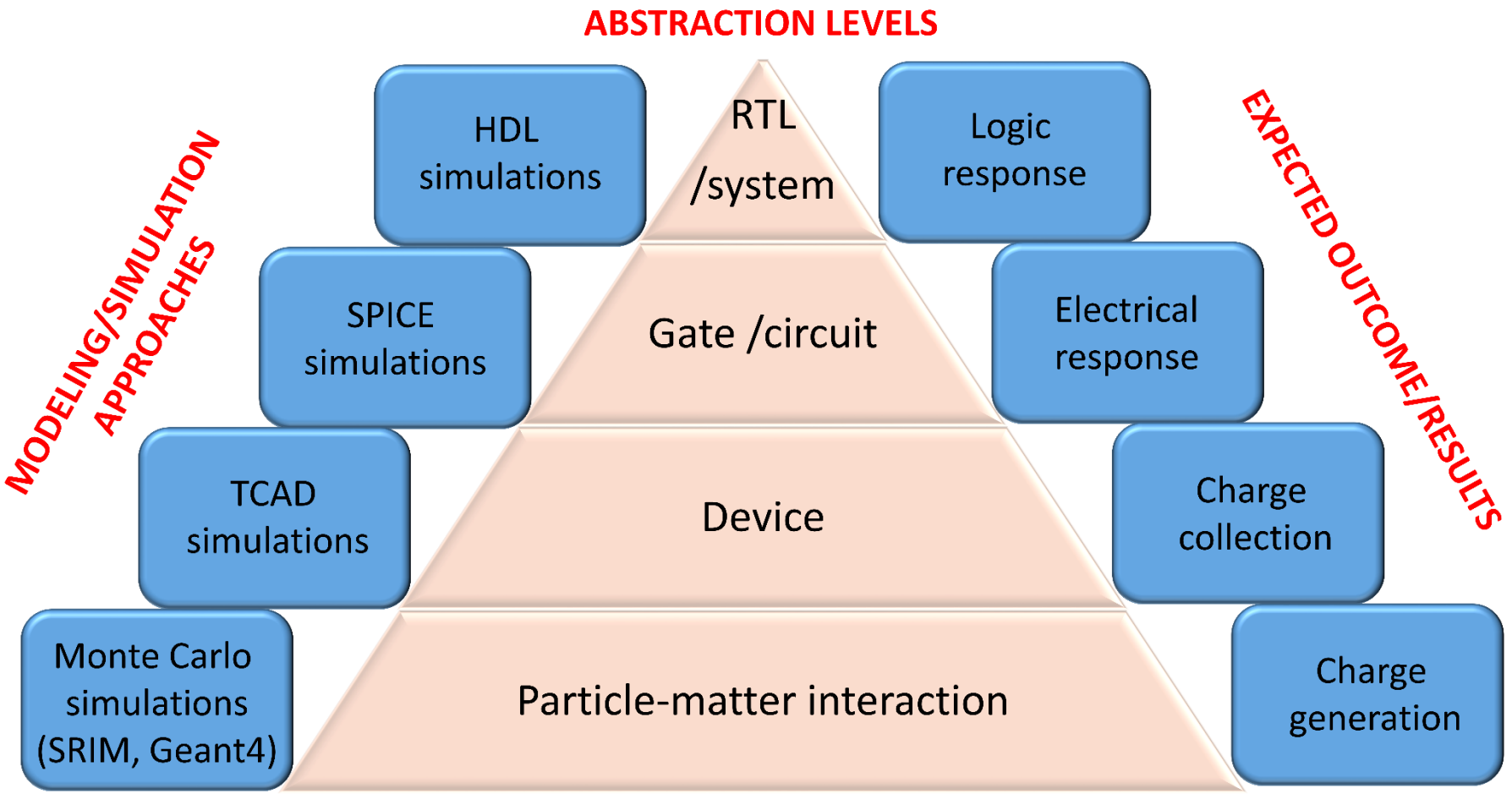
# SEE Mechanisms

- SEEs are induced by a single energetic particle (e.g. heavy ion)
- Manifested as current flow, leading to subsequent voltage disturbance
- Result in soft errors, i.e. change of logic value stored in memory
- SEE modeling and characterization is a key requirement in rad-hard design



# Multi-level SEE Modeling and Simulation

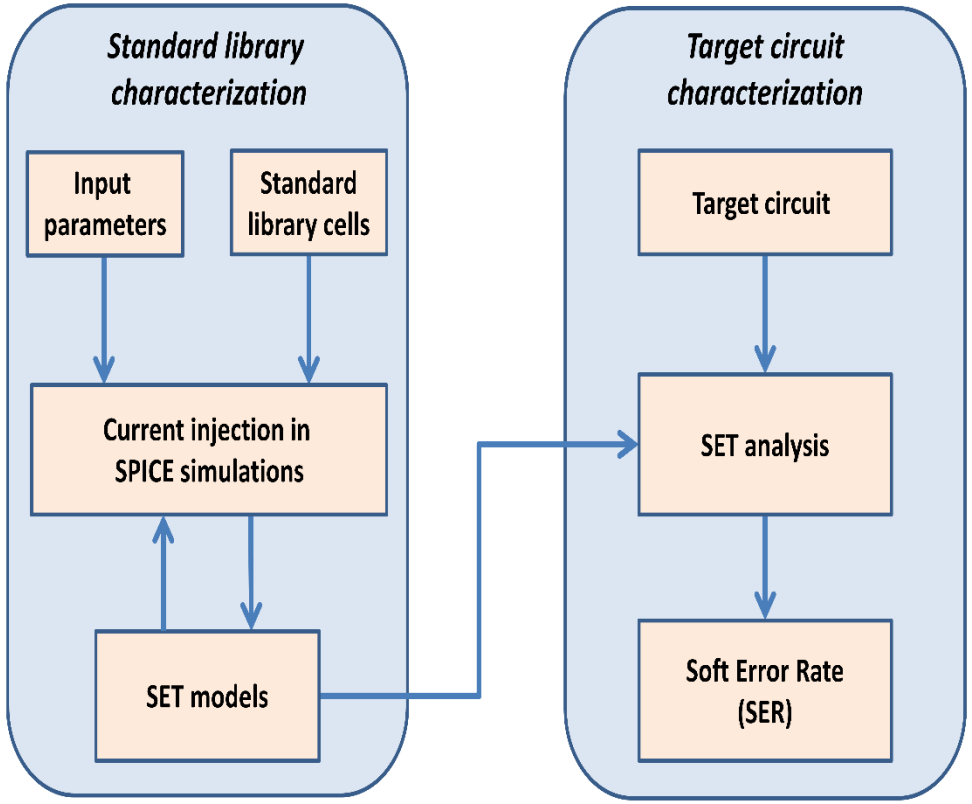


# Comparison of SEE Simulation Approaches

| Approach | Advantages | Disadvantages |
|---|---|---|
| *Particle-matter* | Very fast simulations (in the order of seconds) | Neglects technology parameters |
| *Device* | Accurate analysis of charge collection | Too slow even for simplest structure (can last several hours) |
| *Gate/circuit* | Provides insight into electrical effects<br>Fast for small circuits | Neglects some important physical aspects<br>Too slow for complex circuits |
| *RTL/system* | Fast analysis of SEE propagation in complex circuits | Neglects electrical and physical aspects |

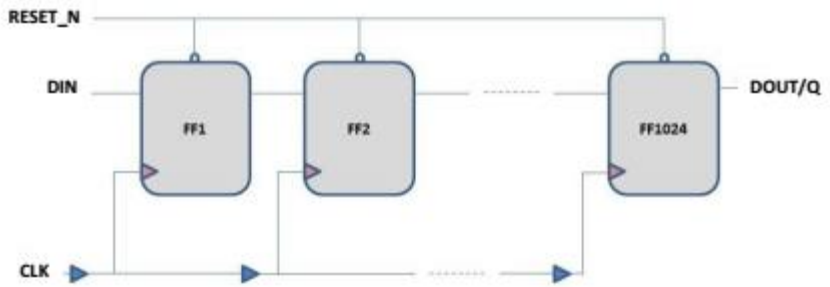
# Optimization of SEE Characterization

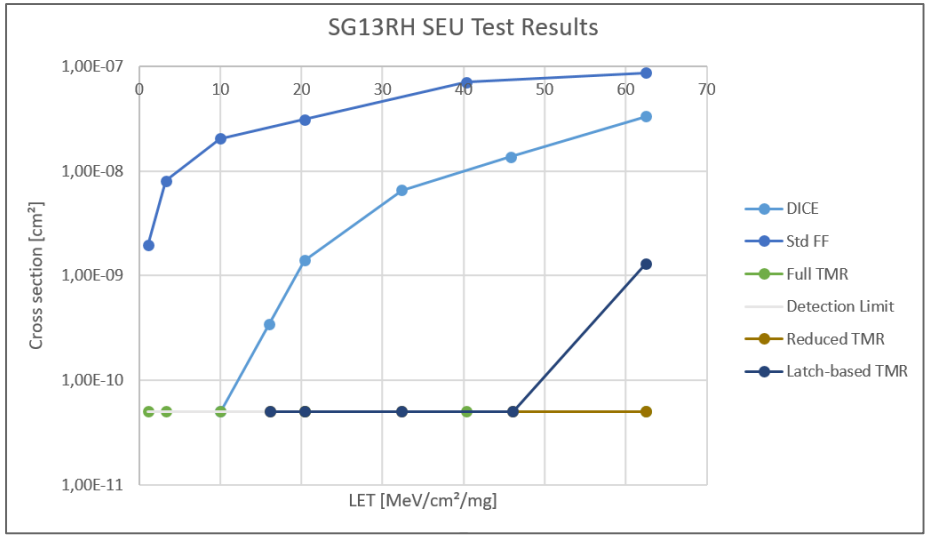
- Multi-level SEE simulation is time consuming for complex circuits
  - Simulations have to be done for every circuit node
- Optimization approach:
  - Characterization of SEEs in standard cells -> done only once
  - Use characterization data to establish analytical models for SER estimation
- Challenges:
  - Minimize the simulations
  - Establish accurate models
  - Apply the models effectively on a large design



# Radiation Testing

- Radiation testing is performed in the special labs equipped for TiD or SEE tests
- For TiD there are plenty of labs supporting Co-60 gamma radiation experiments
- SEE tests are possibile only in few labs (UCL, RADEFF etc.)
- For SEE tests special test setup is needed and the corresponding test vehicle
- Typical test vehicle – shift register
- TiD tests have also specific procedure



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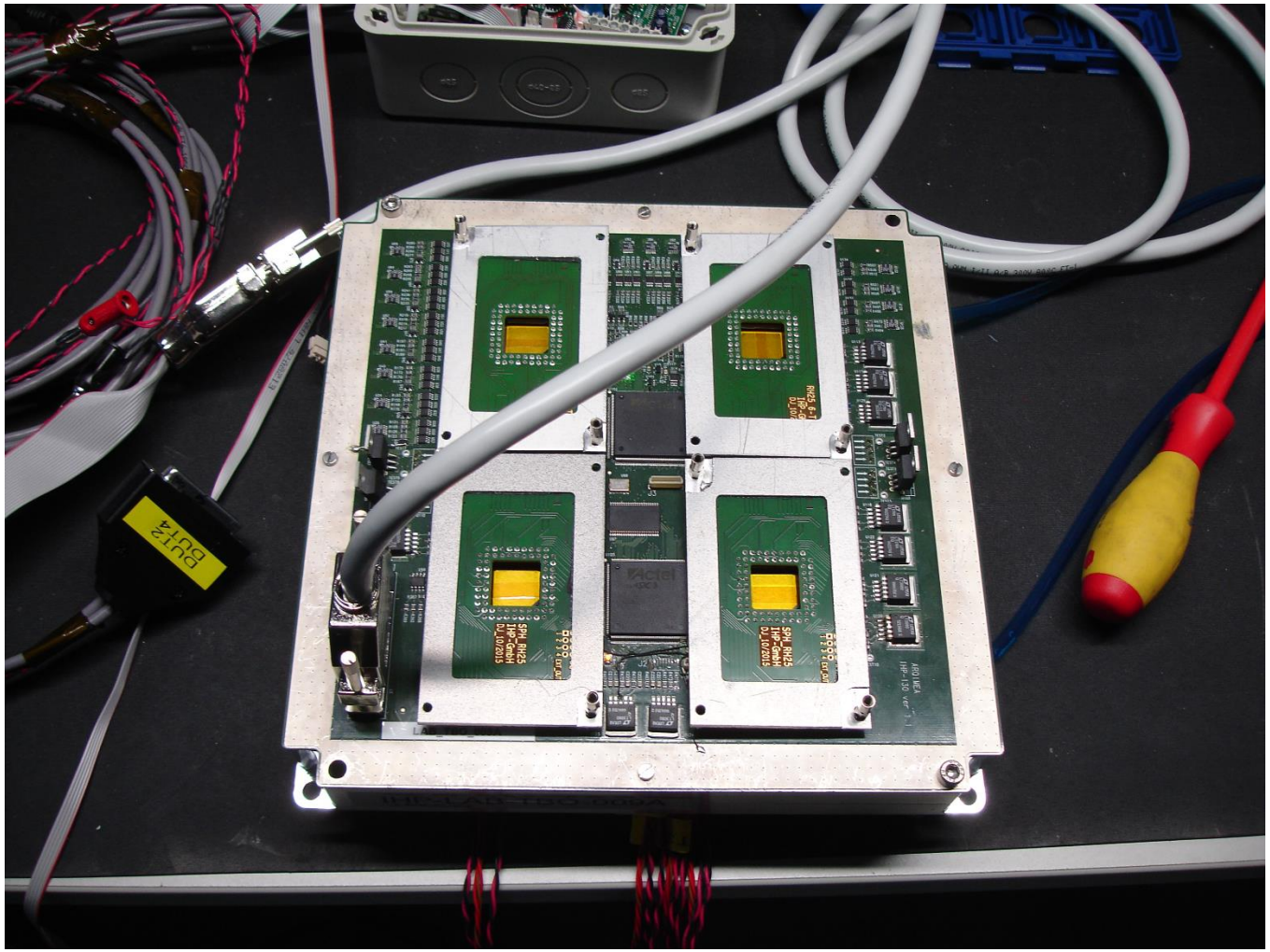

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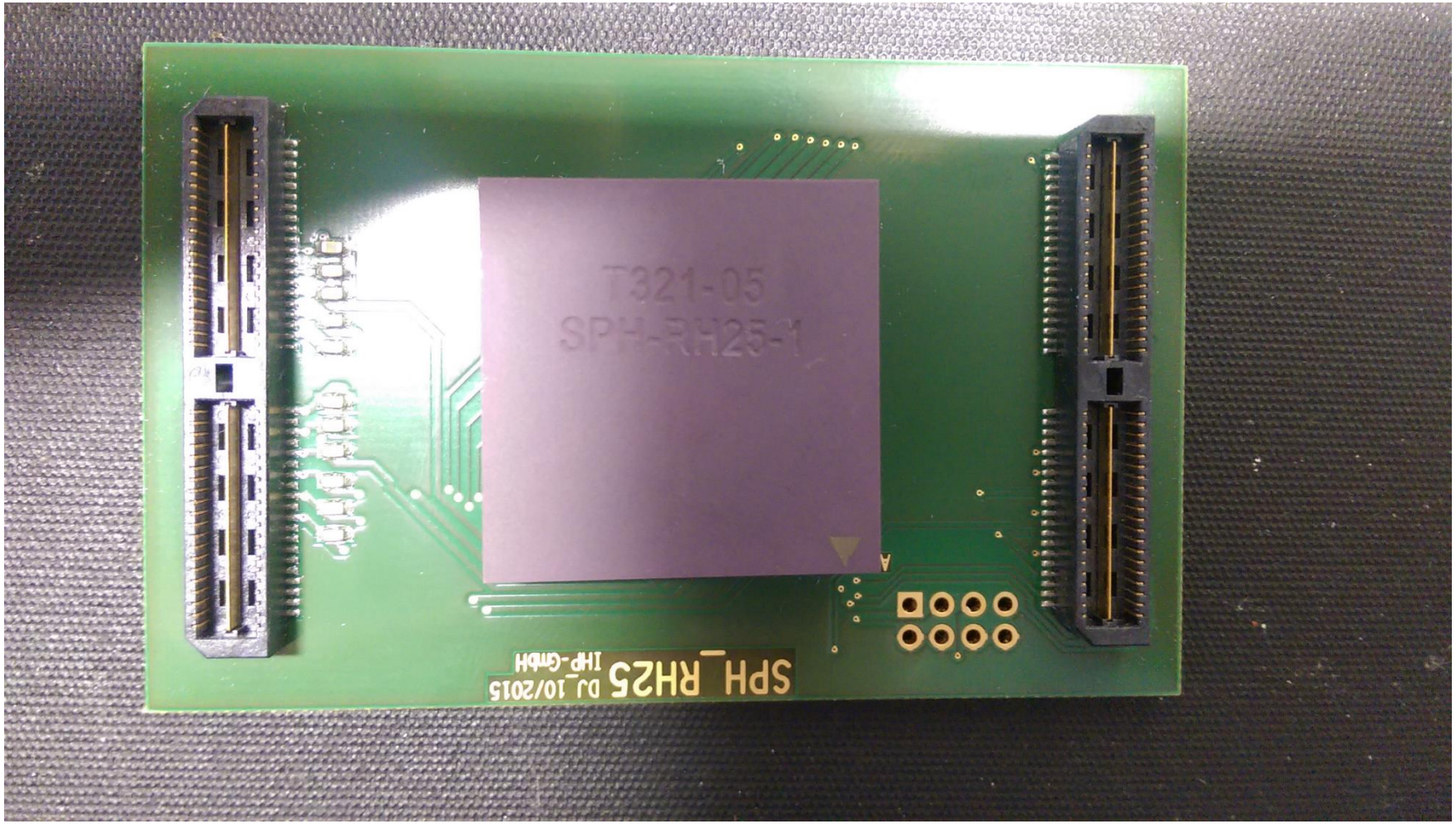

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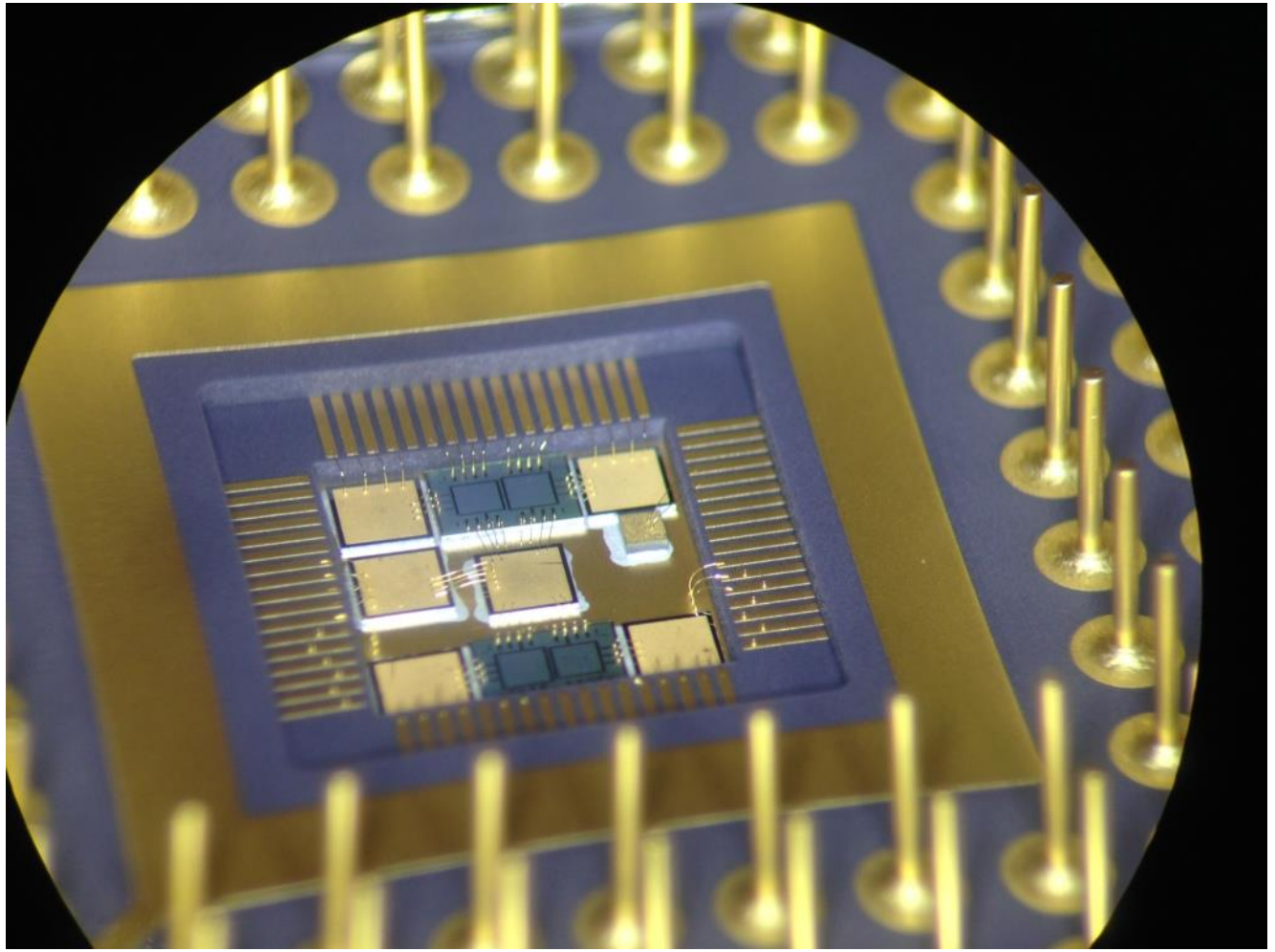

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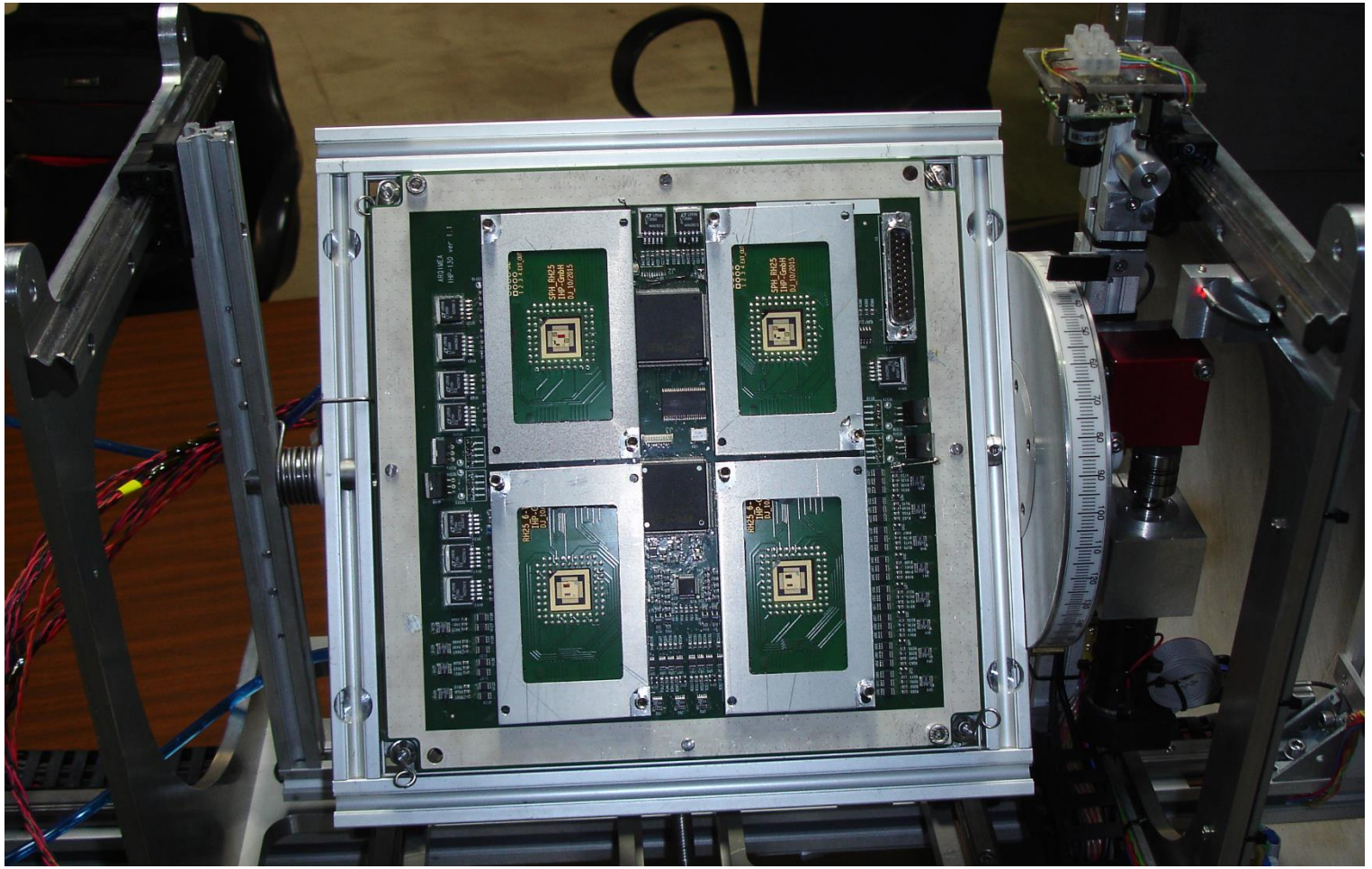

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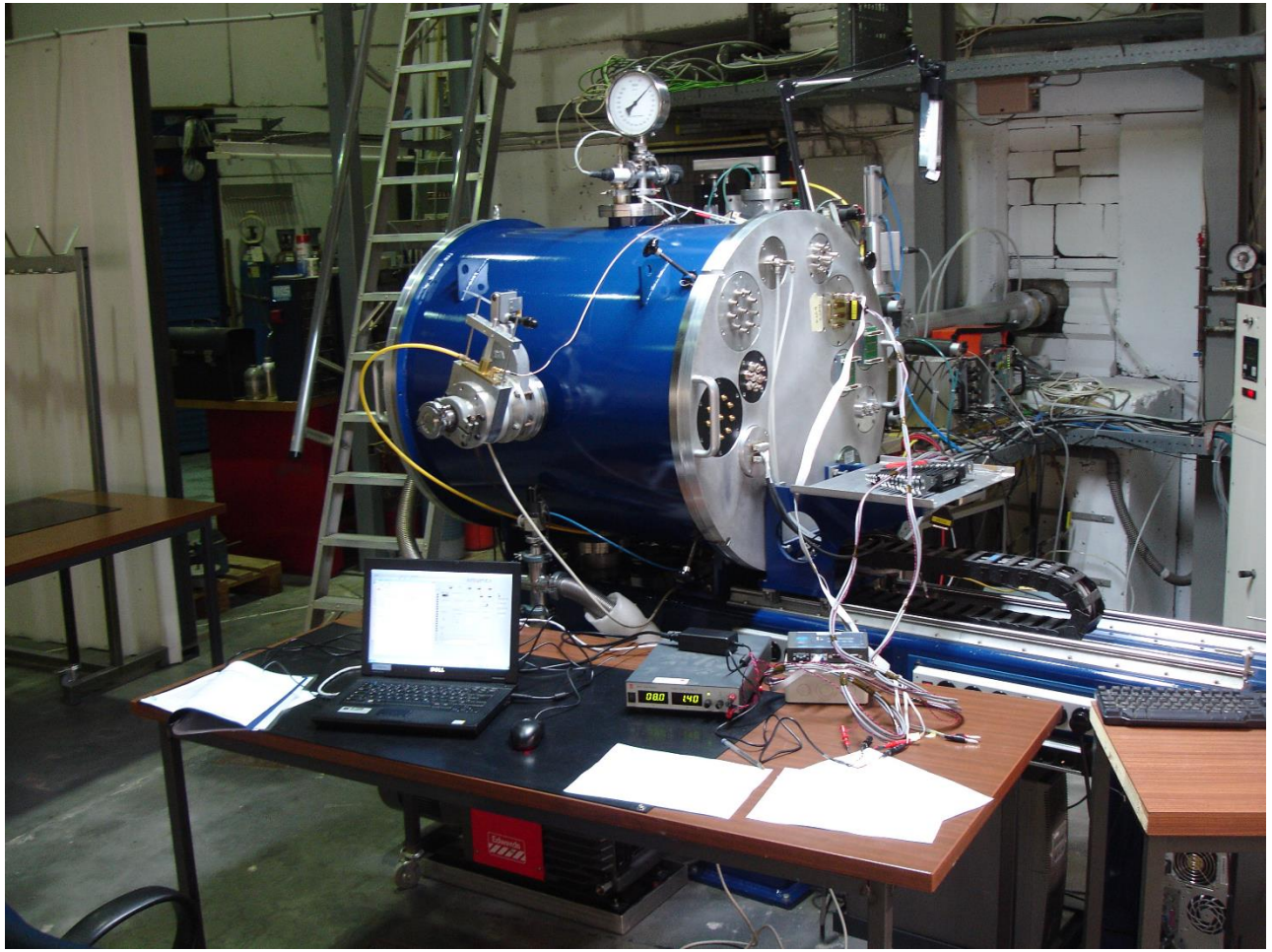

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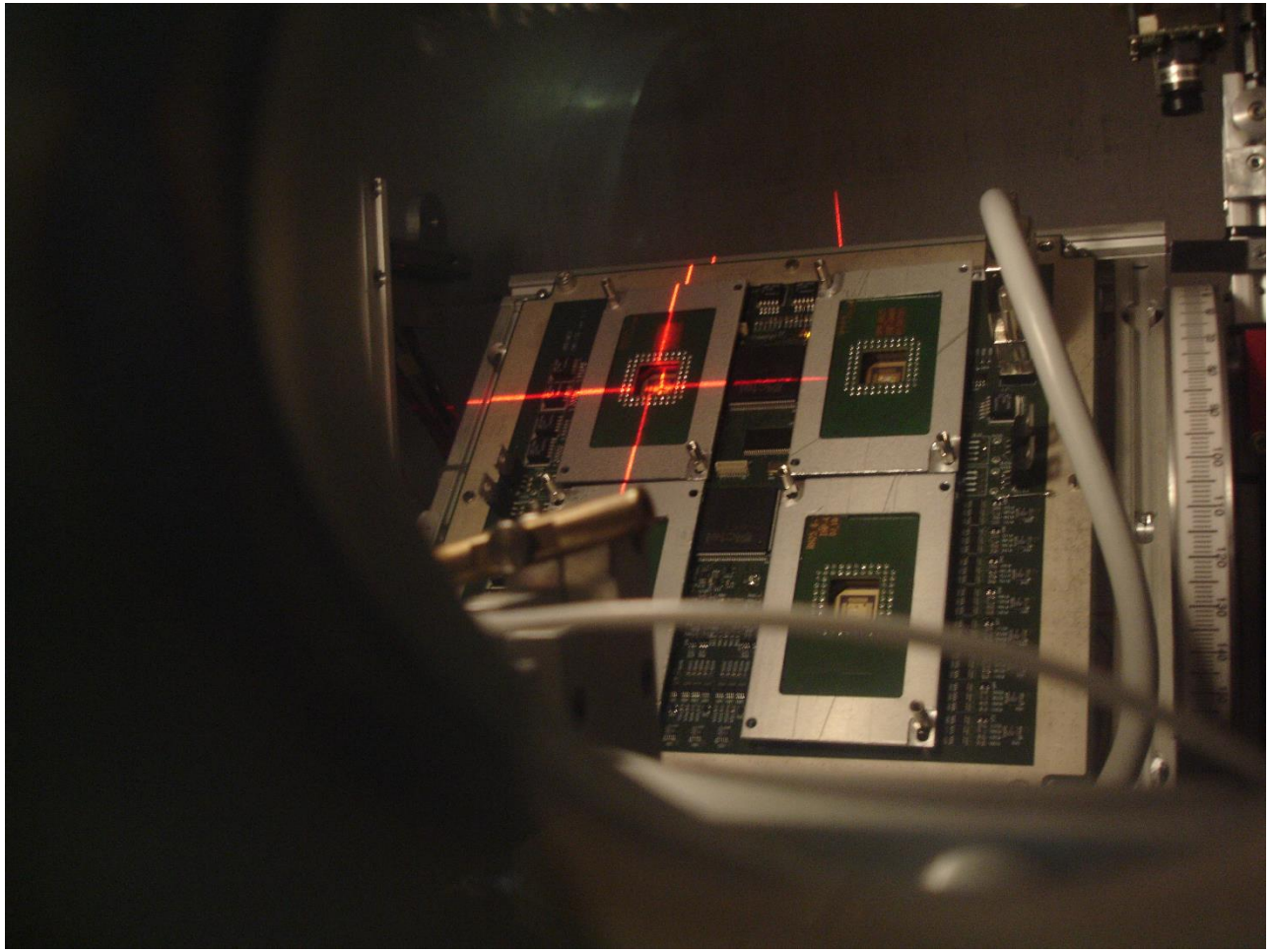
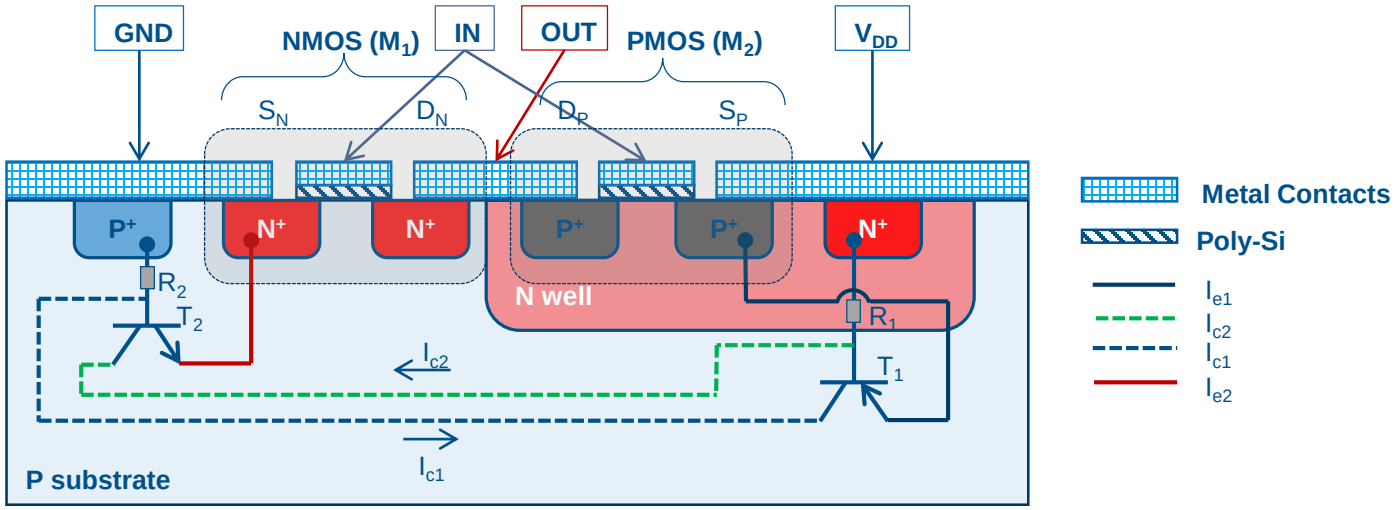


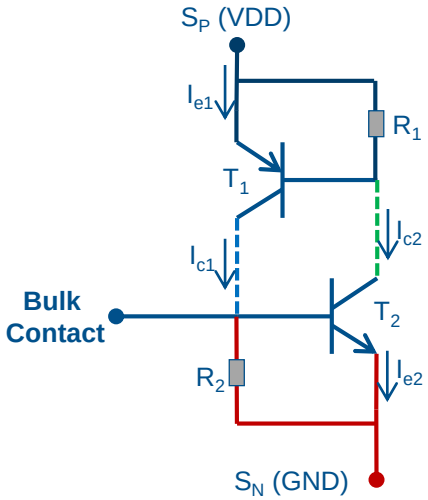
# Single Event Latchups (SELs)

- Single Event Latchups
- Abnormal high current caused for example by single energetic particle causing in CMOS creation of parasitic bipolar transistors



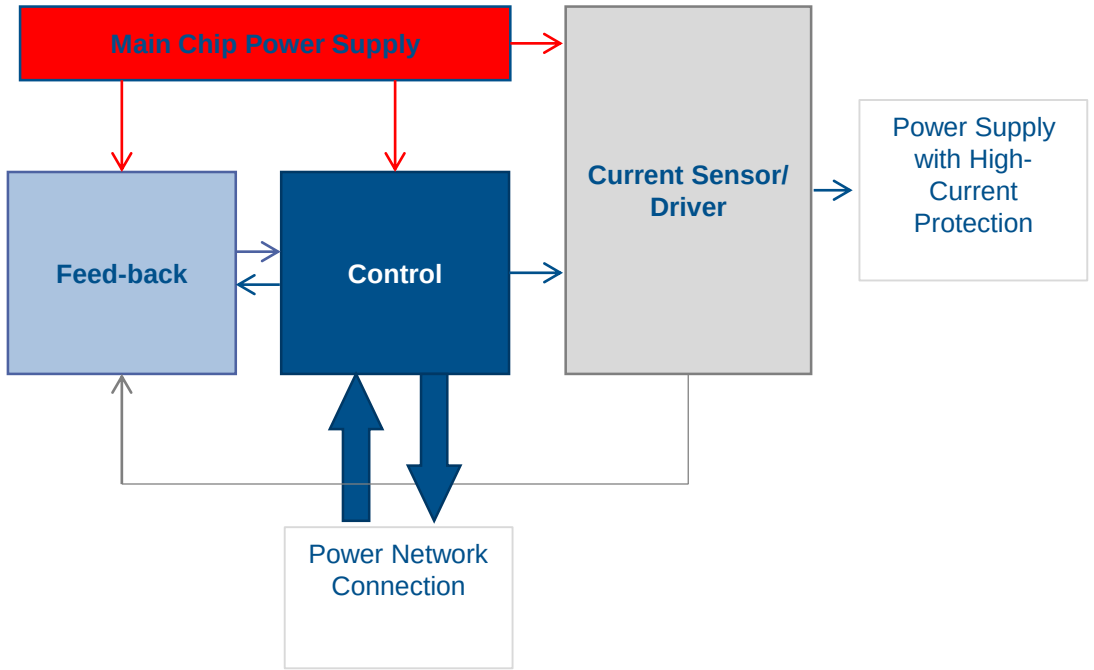






# Addressing SELs

- Some technologies are SEL hard (Silicon on Insulator, FDSOI)
- Strict design rules, substrate contacts, isolating MOS
- Protection circuits on the board (detecting SELs and switching off the power supply
- On-chip protection circuitry



# Addressing SEUs in Digital Systems

- In order to address SEUs the RHBD methods need to be applied
- The methodology could be applied at the different abstraction level of the design process
  - Cell level
  - RTL level
  - System level
- The methods could be static or dynamic
- Usual approach to deal with radiation induced errors are based on fault tolerance
  - The methods lead to overhead, and the goal is to reduce this overhead as much as possible without comprimising the application requirements

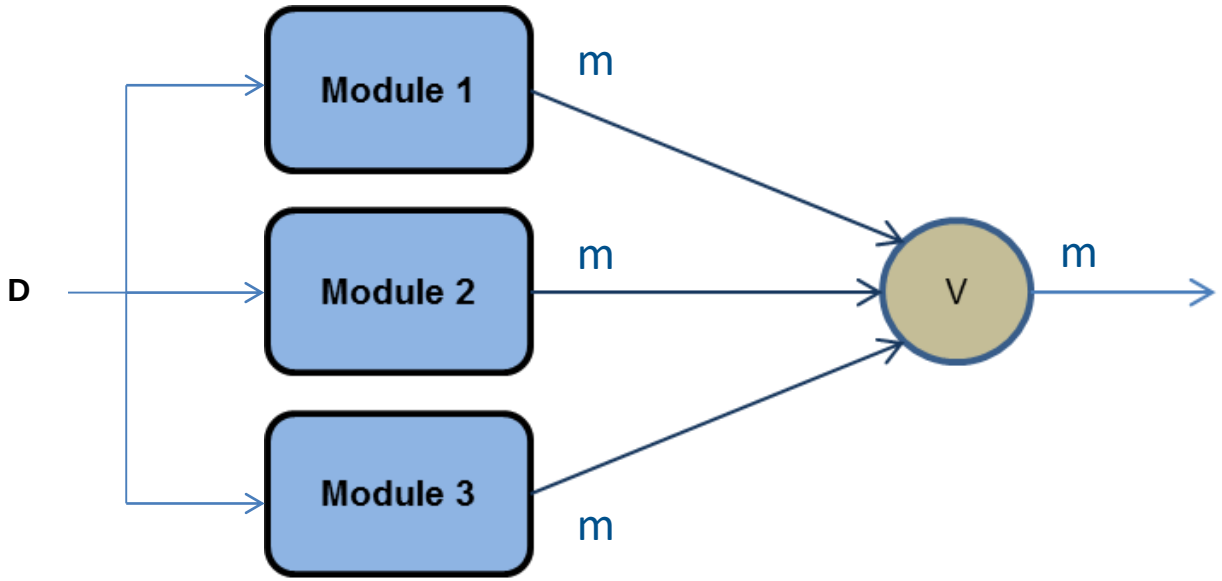
# Radiation Hardness on the Cell Level

- The usual approach of space design companies is to address the radiation hardness at the cell level
- As a result the special cell library is designed (usually known as radhard libary)
- Important elements of the radhard cell library:
  - Radiation tolerant flip-flops: in order to avoid SEUs and filter SETs
    - TMR, DICE, HIT flip-flops
  - Special buffers tolerant against SETs: for clock and reset tree
    - Sizing of transistors could influence radiation sensitivity
  - Guard Gates: for SET filtering
    - Special architecture
  - IO pads, including SET filtering
  - Radhard SRAM:
    - radiation tolerance of the control interfaces
    - increased critical charge of the cell
    - special cell placement to avoid multi-bit upsets (MBU)
    - ECC for SEU correction

# Hardware Redundancy with TMR

- The general approach is N-modular redundancy
  - Such systems are also known as M-of-N Systems
  - N=3, Triple Modular Redundancy (TMR)
  - N=2, Dual Modular Redundancy (DMR)

How TMR works?



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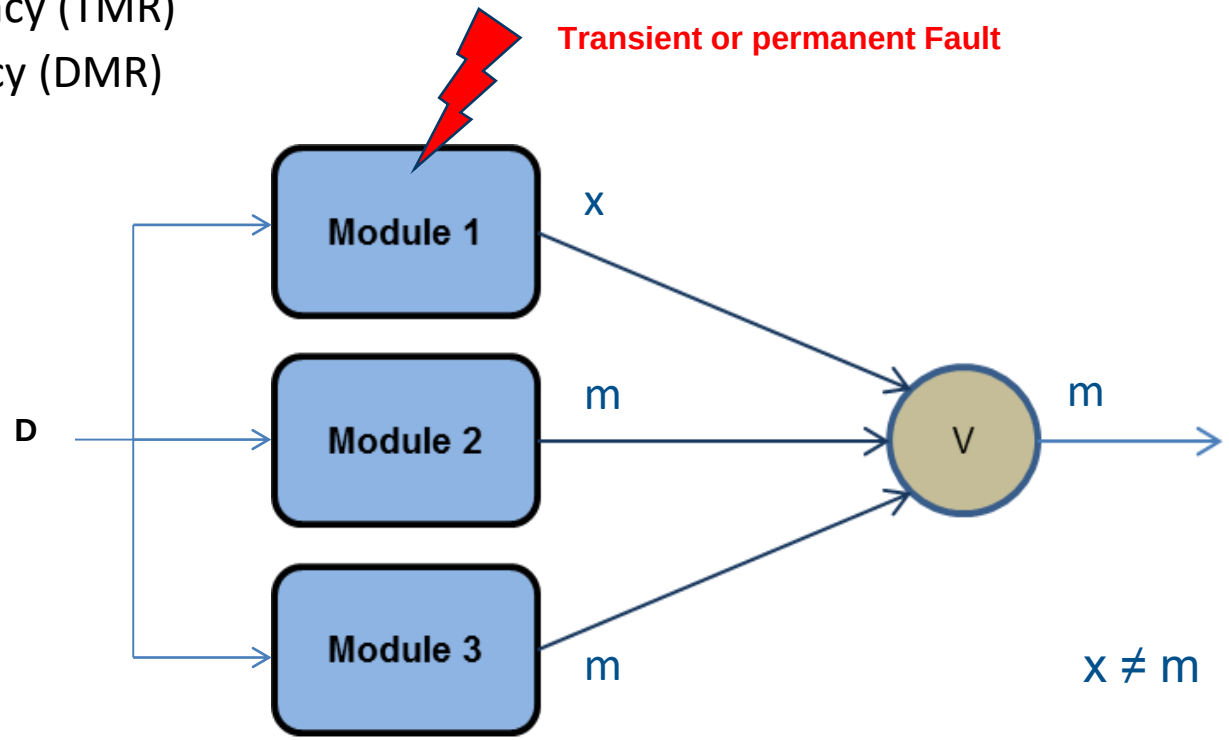

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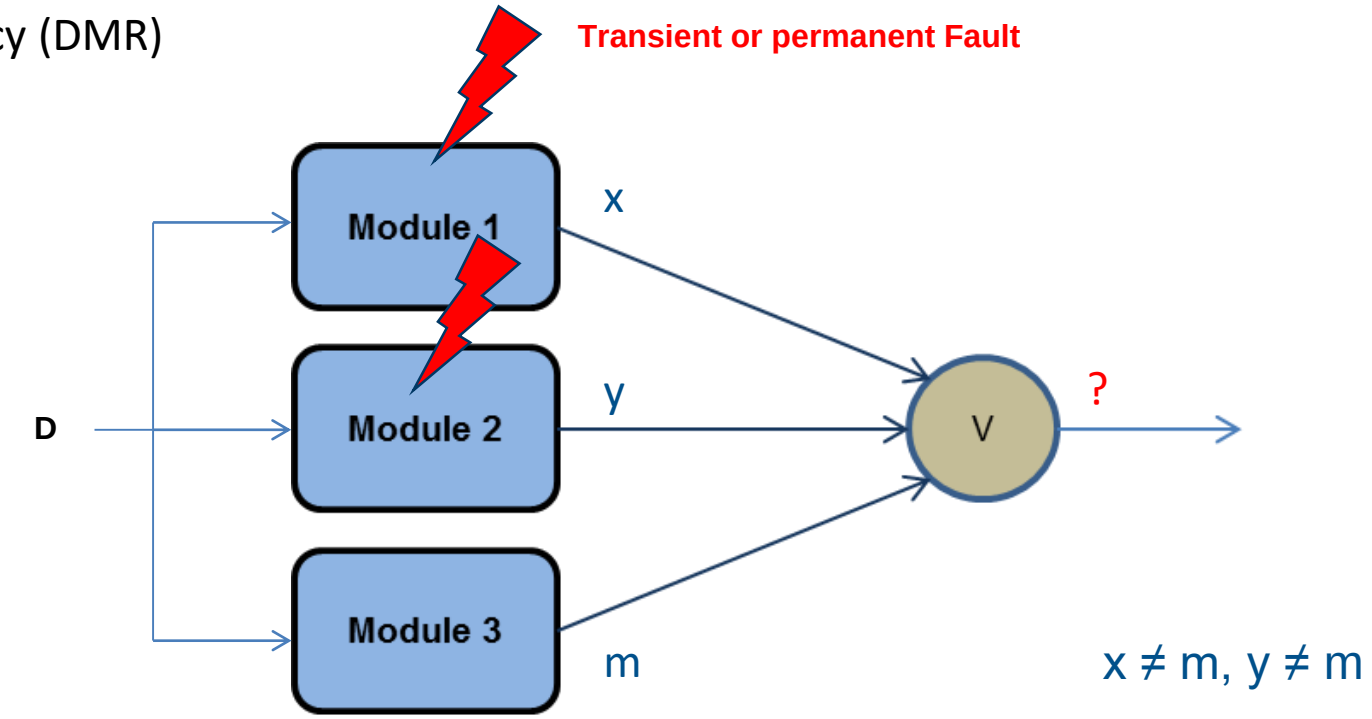
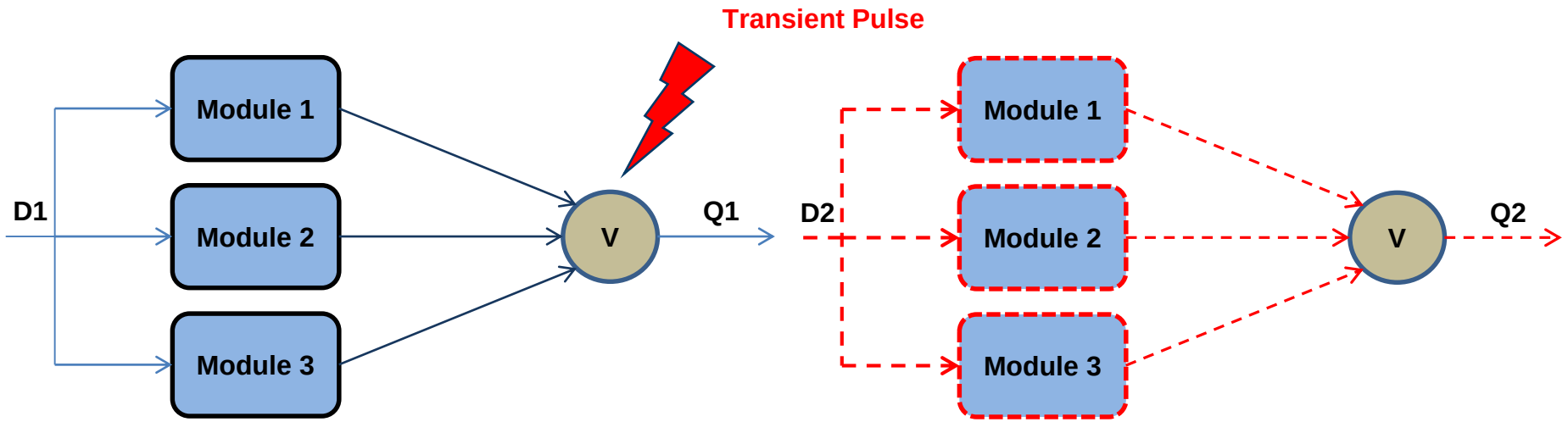



TMR is 2-of-3-System!

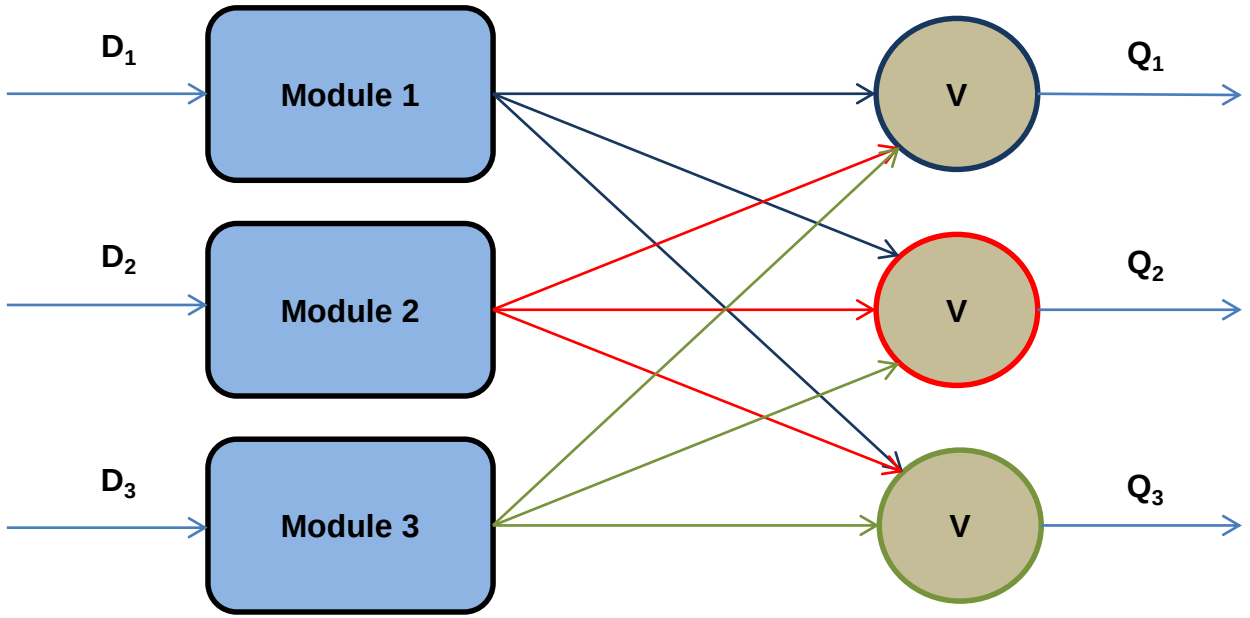
# Limits of the simple TMR-Circuit

- Voter (V) is the single point of failure!



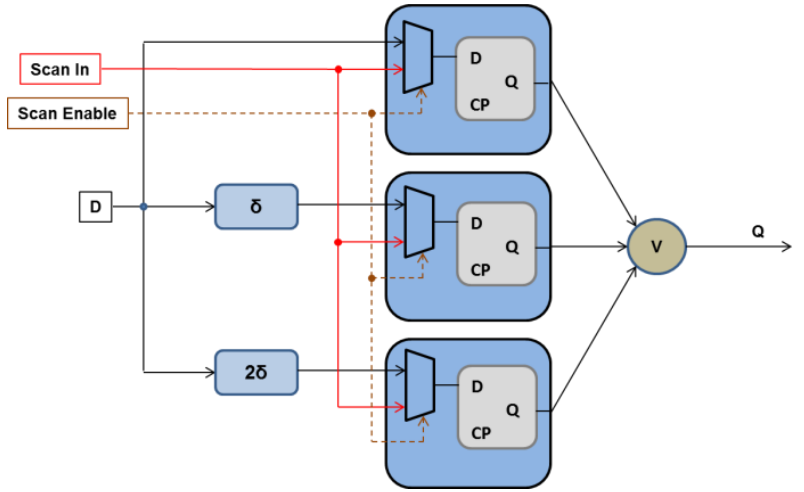
# Alternative TMR-Architecture

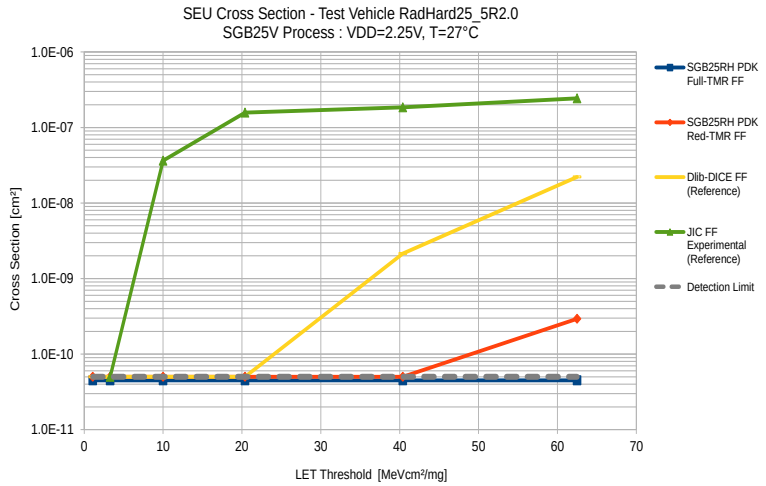
- Full TMR-architecture, including TMR-Voter



# TMR Flip-Flops

- TMR architecture could be effectively used against SEUs
- Single SEU in TMR scheme can be outvoted
- Cell placement is very critical to avoid MBUs (multiple bit upsets)
- Incoming SETs can be avoided with adding delay on input line
- The solution is very expensive in terms of additional hardware and power overhead




Schrape O, Andjelkovic M, Breitenreiter A, Zeidler S, Balashov A, Krstic M. Design and Evaluation of Radiation-Hardened Standard Cell Flip-Flops. Vol. 68. New York, IEEE Trans Circuits & Systems, Part I,; 2021.

# Consequences and Solutions

Redundancy = Power/Area Increase and performance drop!

The overhead could be more than N times baseline

The classical FT techniques could be performed in the more optimal way:

Static solutions:

- Limiting the level of fault tolerance but significantly reducing overhead (partial FT, ECC codes etc.)

Dynamic (adaptive) solutions:

- Enabling system adaptivity: using overhead only when it is needed
- Adaptivity is the key requirement for complex system implementation in advanced technologies

Example solutions:

- Static - partial and selective fault tolerance, FEDC
- Adaptive - adaptive MPSoCs

**Resilience**: Addressing with the same mechanisms different challenges

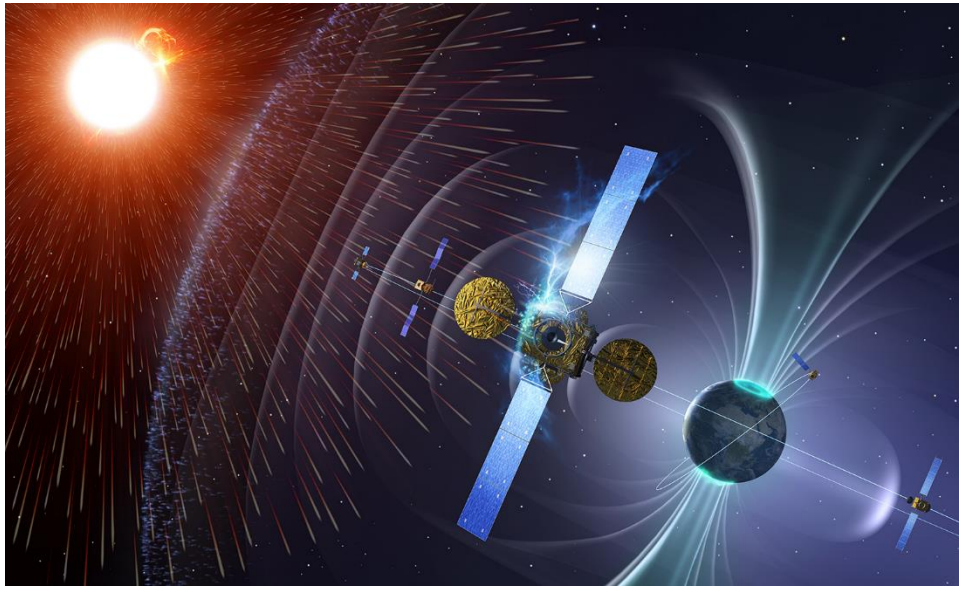
- Faults, PVT variations, security

# Static Solutions

# Selective Fault Tolerance

- Continuous reduction of transistor size increases sensitivity for upsets in sequential elements
  - Mainly radiation induced
- Especially important for space applications because of higher particle radiation
- Protection of flip-flops against soft errors in digital circuits incurs significant overheads
- Reduce protection costs by protecting only flip-flops in which faults have an intolerable impact
- Identify critical flip-flops in which faults can produce
  - an effect on system output
  - persistent error in system state

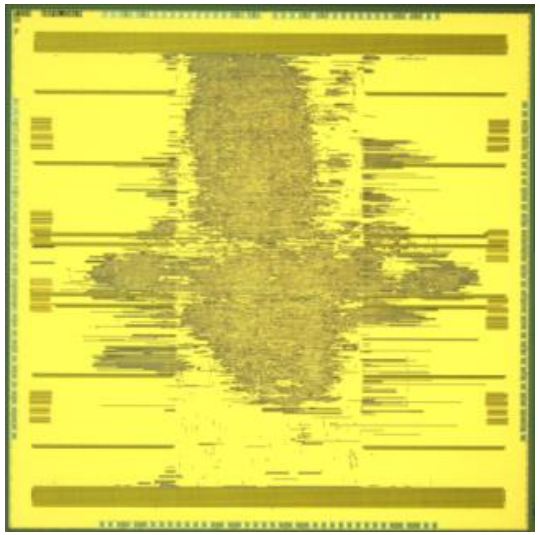
A. Breitenreiter, et al, "Selective Fault Tolerance by Counting Gates with Controlling Value" 2019 IEEE 25th International Symposium on On-Line Testing And Robust System Design (IOLTS), Rhodes Island, Greece, July 2019.



[https://www.esa.int]

# Partial Fault Tolerance

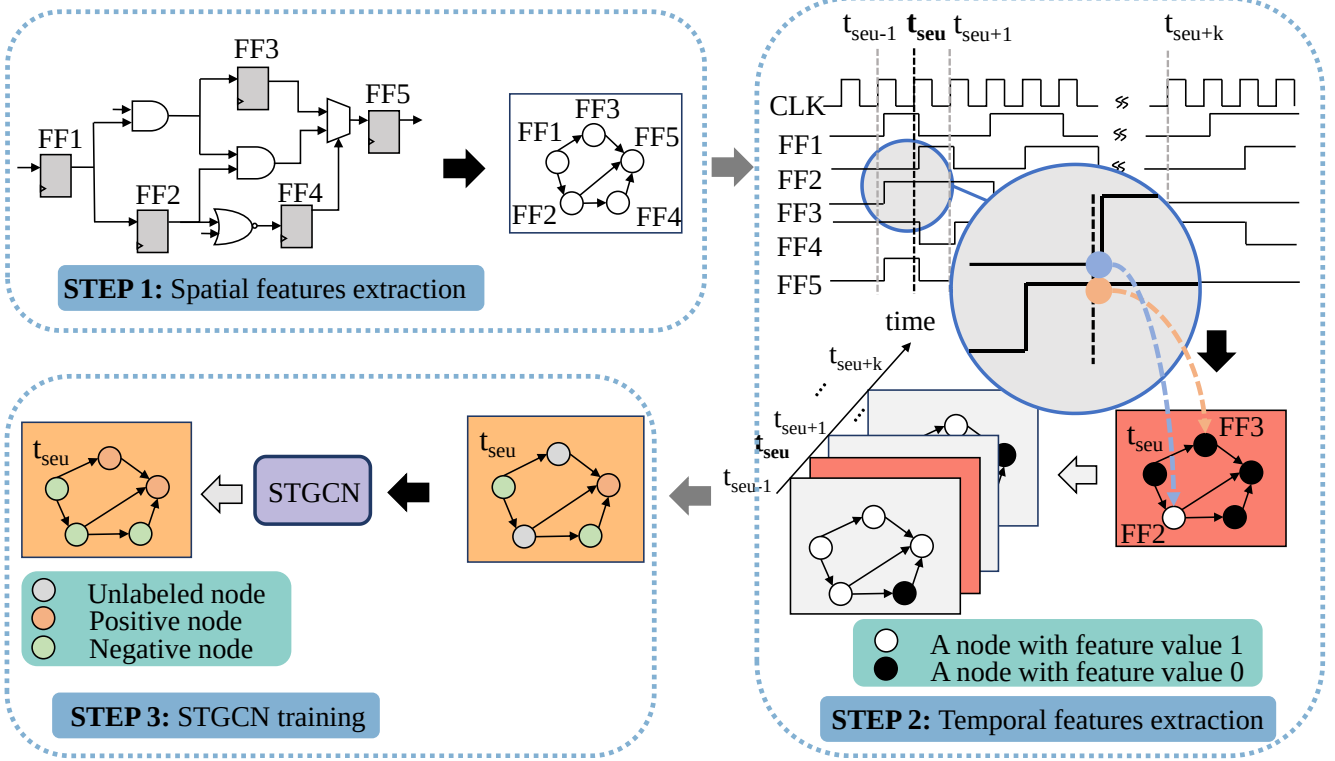
- We can reduce the overhead if we protect with redundancy only the parts of the systems which are most critical (control logic, command/status registers)
- This method is called partial fault tolerance
  - However, some part of the system remains fully unprotected
- Example: Design of Digital Beamforming Network processor for synthetic aperture radar (EU Project DIFFERENT)
- Digital baseband IC and in IHP technology
  - DFBN Chip tape-out Aug 2015 – 46 mm2 in SGB25V
  - Tested on wafer and operational up to 250 MHz!
  - Optimized overhead
    - saving 20% in area and 33% in power
    - radiation hardened TMR flip-flops in control logic
    - Standard flip-flops in datapath



DBFN Baseband Processor - 46mm$^2$ in SGB25V, Sep 2015

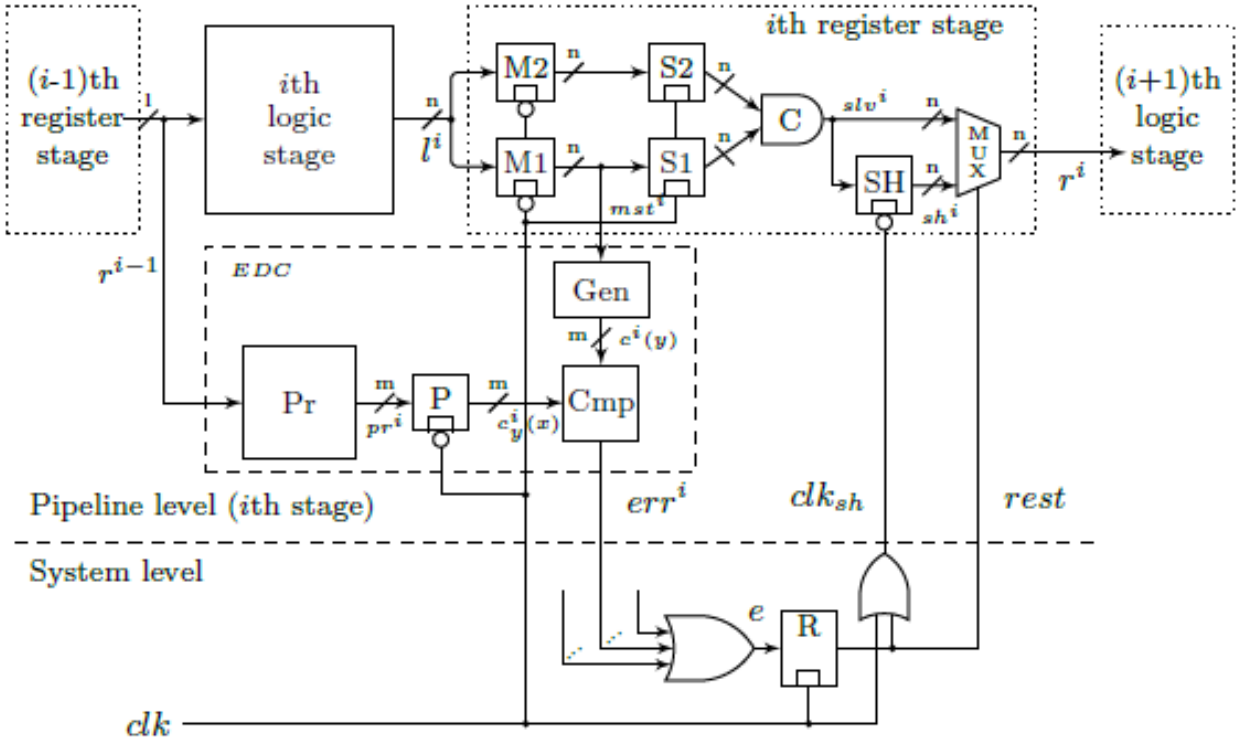
# Accelerate fault simulation with Machine Learning

- Simulation-based fault injection for reliability analysis is time-consuming.
  - Machine learning could be the alternative
- **GNNs** were able to identify critical flip-flops in terms of SEU tolerance.
  - The accuracy achieved with Ibex and RI5CY is up to 98%.
- **Spatio-temporal Graph Convolutional Network** (**STGCN**) could predict the results of SEU error simulation.
  - We validated the proposed method on four test circuits and achieved a prediction accuracy of 94-96 %.




| Circuit | Number of Samples | Percentage of Positive Samples (%) | Precision (%) | Recall (%) | Accuracy (%) |
|---|---|---|---|---|---|
| I2C | 7650 | 70.56 | 97.25 | 97.71 | 96.52 |
| SPI | 6550 | 62.60 | 96.19 | 97.63 | 96.23 |
| XGE-MAC | 48888 | 52.12 | 96.54 | 96.33 | 96.26 |
| Ibex | 63780 | 16.51 | 83.32 | 78.55 | 93.96 |

# Full Error Detection and Correction (FEDC)




Focused on full error correction

- All injected SETs could be corrected
- Suitable for long transients as well
- Effective against timing errors

Hardware/power overhead reduced compared with TMR

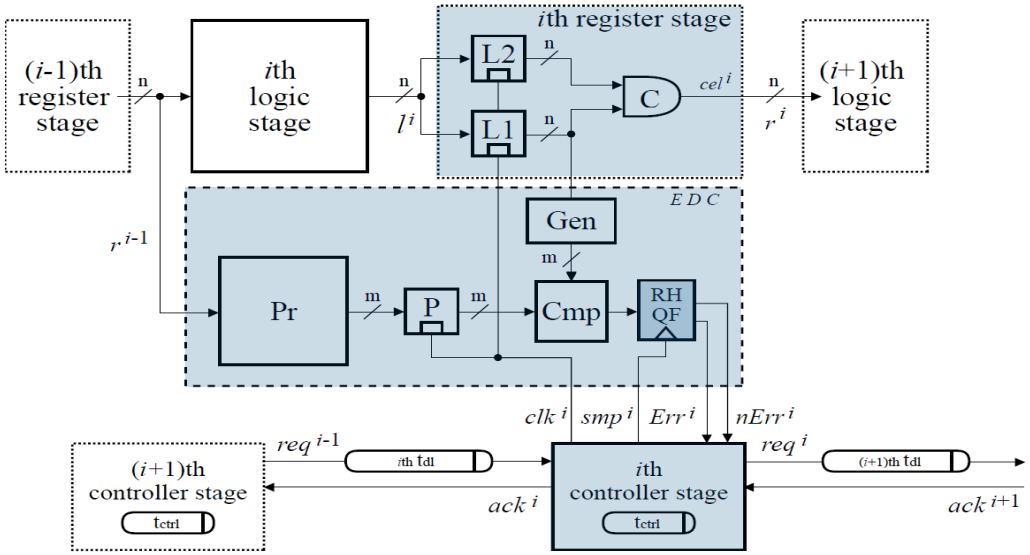
- Saves around 28% power

| Circuit | Dynamic Power [mW] | Area Comb [mm2] | Area Sequential [mm2] | Area Total [mm2] |
|---|---|---|---|---|
| TMR | 0,600 | 0,0421 | 0,0125 | 0,0470 |
| FEDC | 0,432 | 0,035 | 0,0126 | 0,0418 |

Milos Krstic, et al., Enhanced Architectures for Soft Error Detection and Correction in Combinational and Sequential Circuits, Microelectronics Reliability, 2016

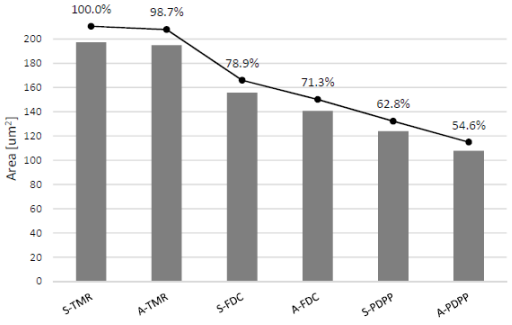
# Asynchronous Full Error Detection and Correction - AFEDC

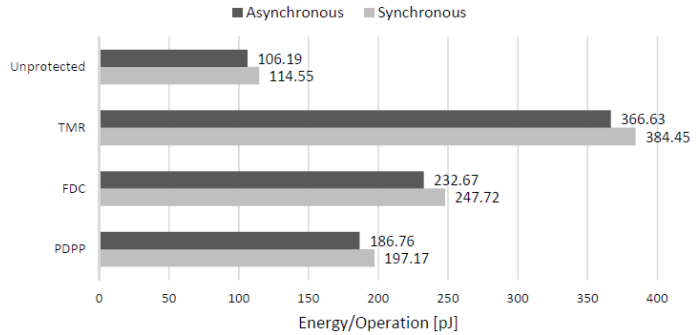
- Soft error resilient stage
  - Latch-based register
    - Dual Modular Redundant - DMR
    - C-element as voter
  - Bundled-data controller
    - 2-phase protocol
    - Click design
  - Error Detection Circuit - EDC
    - Partial Duplication with Parity Prediction - PDPP
    - Full Duplication and Correction - FDC
    - Q-Flop - QF




PNA-DIVIDER FAULT COMPARISON.

| Circuit | Injected faults | Flagged faults | Not corrected SETs | |
|---|---|---|---|---|
| | | | No. of not corrected SETs | % |
| S-Unprotected | 14885 | 350 | 350 | 100% |
| A-Unprotected | 15190 | 389 | 389 | 100% |
| S-TMR | 45128 | 24996 | 0 | 0% |
| A-TMR | 46088 | 25424 | 0 | 0% |
| FEDC-FDC | 29917 | 1047 | 0 | 0% |
| AFEDC-FDC | 30821 | 1140 | 0 | 0% |
| FEDC-PDPP | 22609 | 766 | 135 | 17.62% |
| AFEDC-PDPP | 23333 | 692 | 363 | 52.46% |




F. Kuentzer, M. Krstic, Soft Error Detection and Correction Architecture for Asynchronous Bundled Data Designs, IEEE Transactions on Circuits and Systems I: Regular Papers – TCAS-I, 2020

# Dynamic Methods

# Architectural Framework for Adaptable Multiprocessors

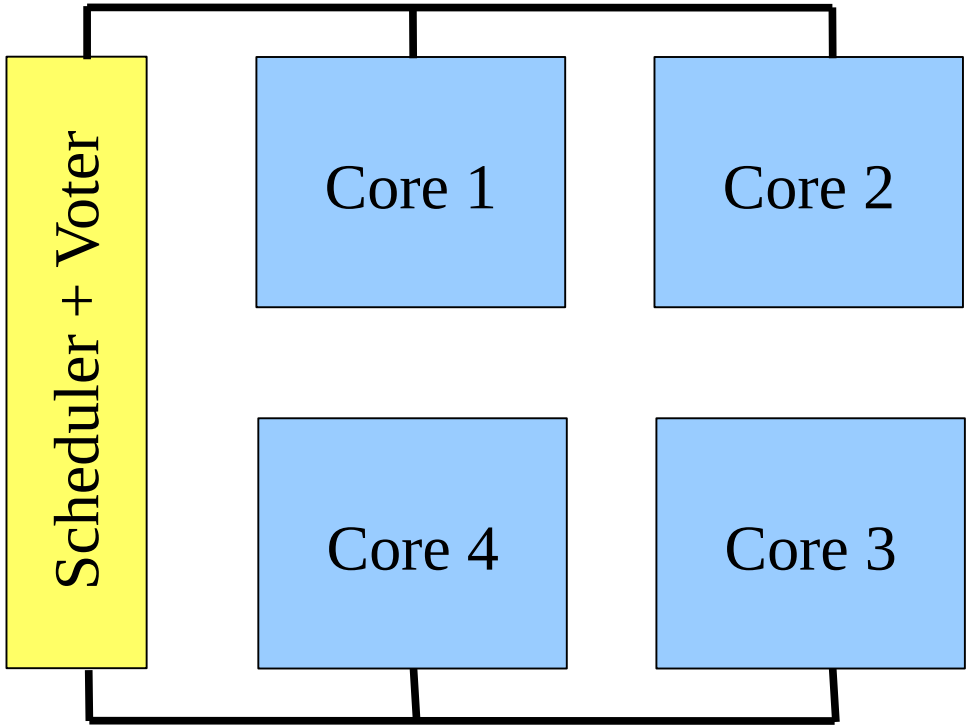
Framework addressing fault-tolerance and aging effects for space and automotive applications

- Aging monitors
- Automated HW/SW verification, design & test
- Programmable NMR voters

Modes of operation

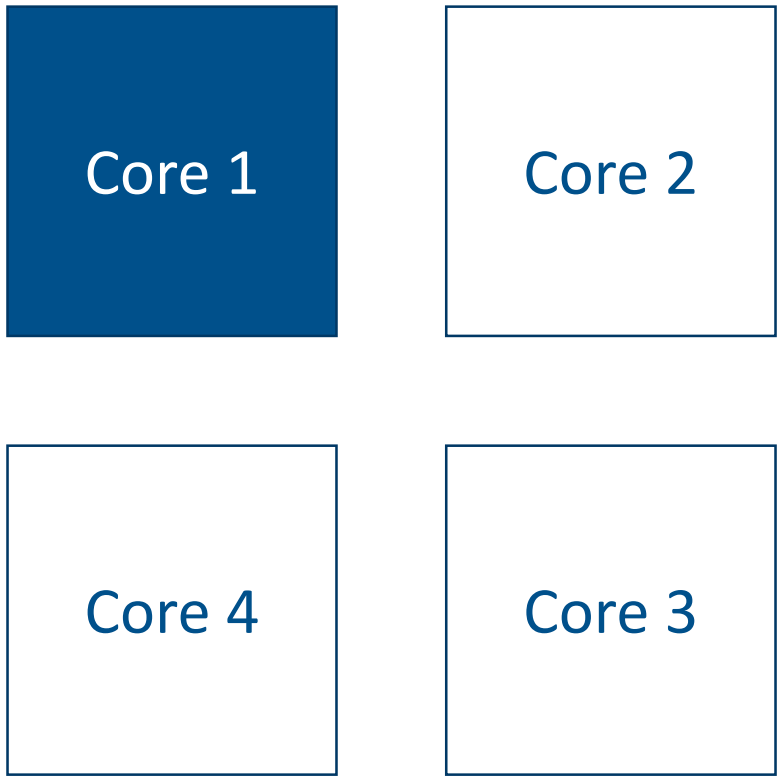
- De-stress
- Fault-tolerant
- High-performance

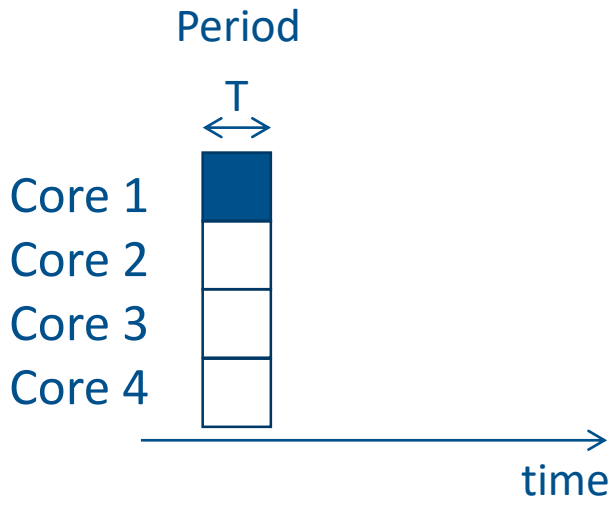
Dynamic mode change depending on the application requirements




A. Simevski, R. Kraemer, M. Krstic, Investigating Core-Level N-Modular Redundancy in Multiprocessors, IEEE MCSoC-14

# De-stress mode



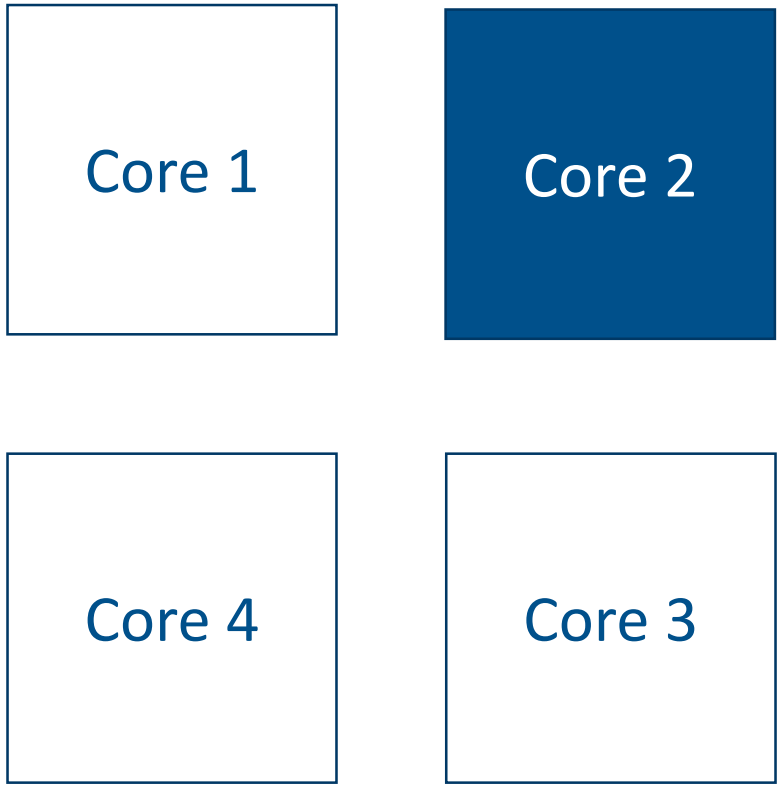



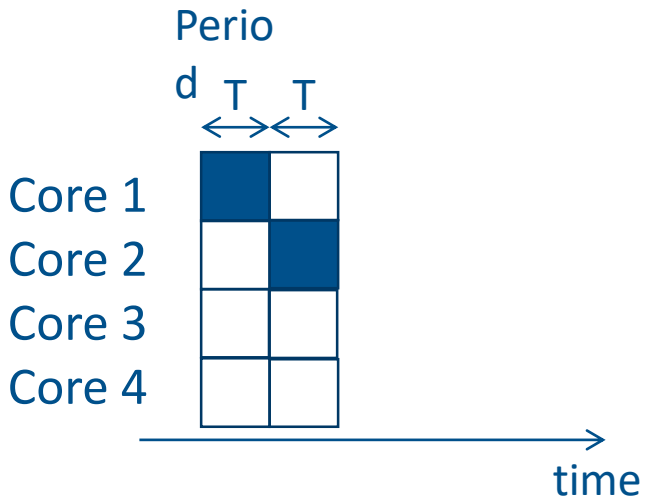

Legend:

= active core

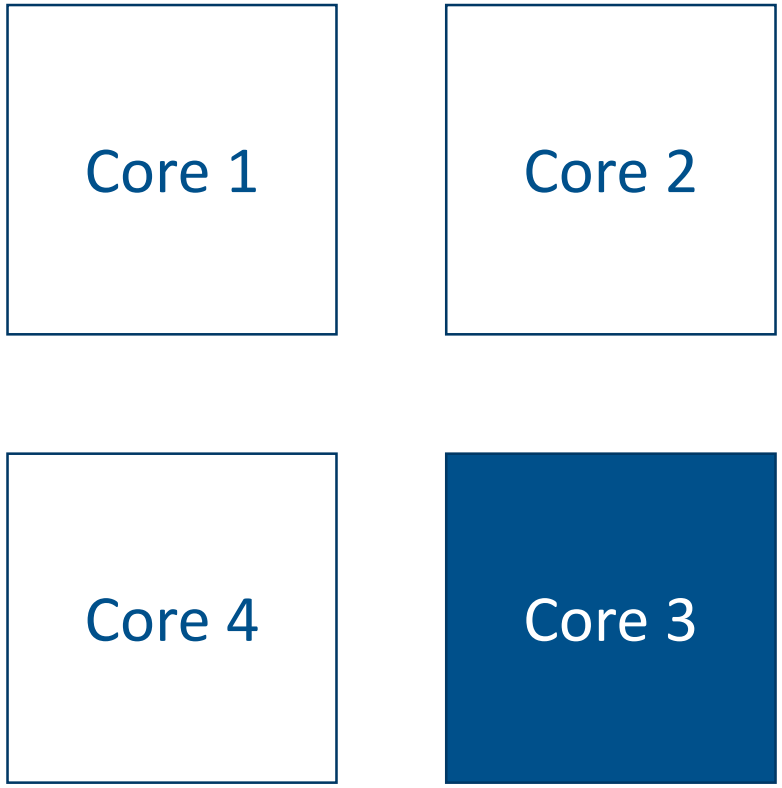
= inactive core

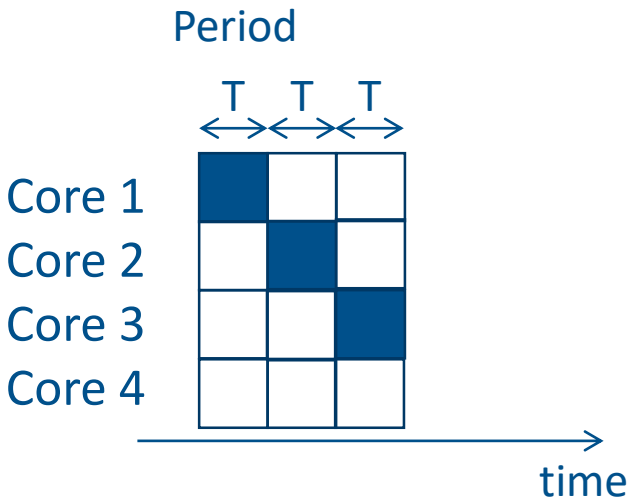
# De-stress mode



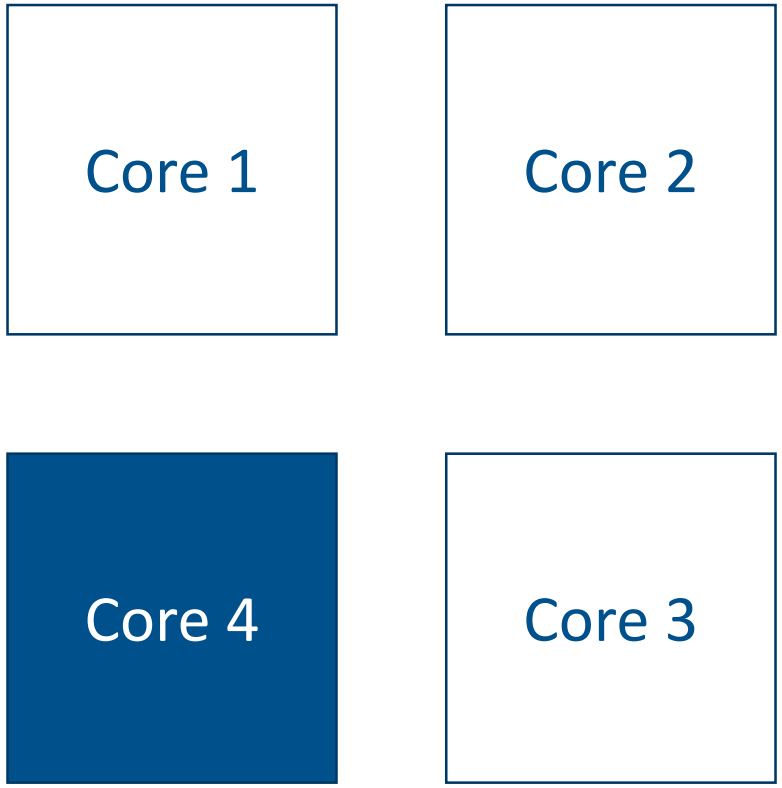



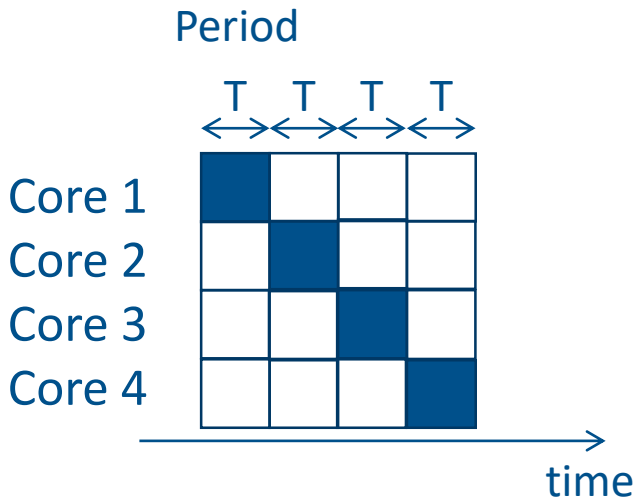
# De-stress mode



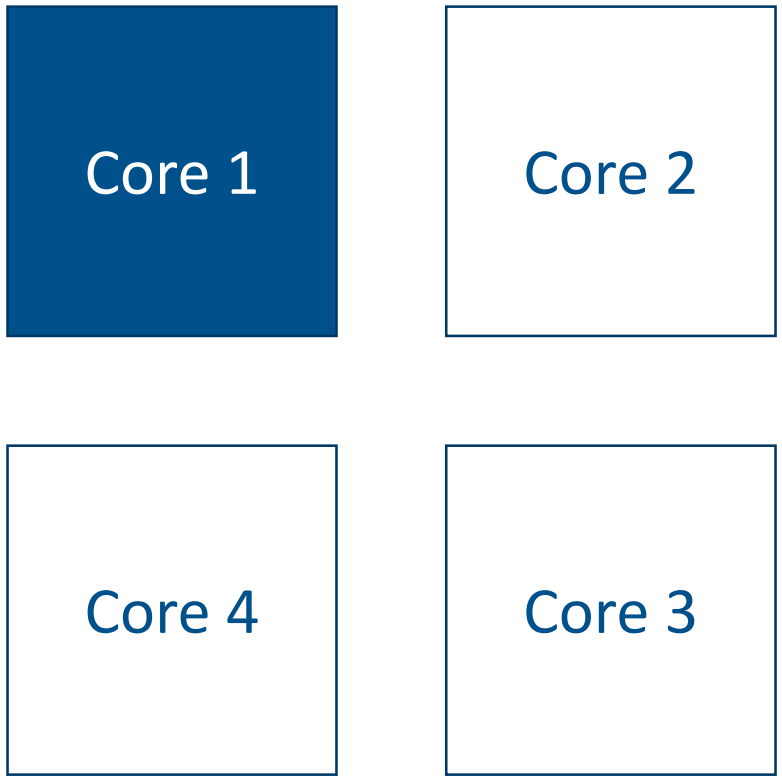



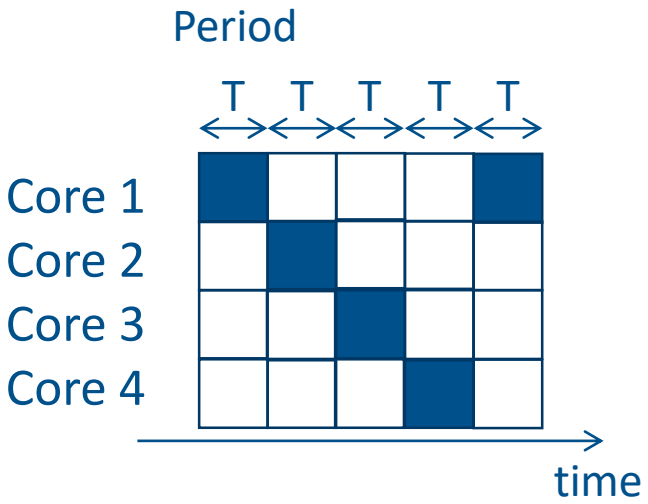
# De-stress mode



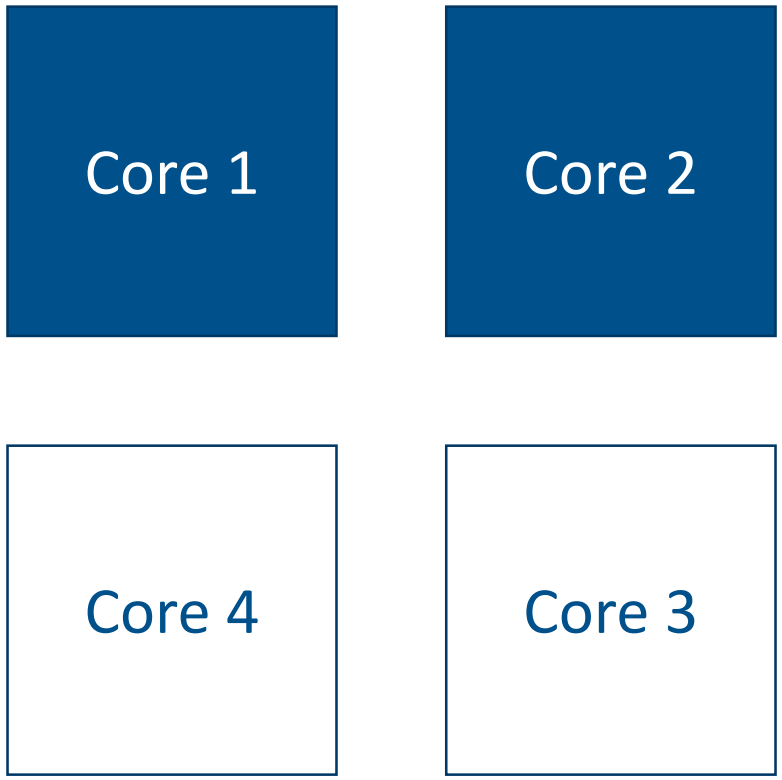



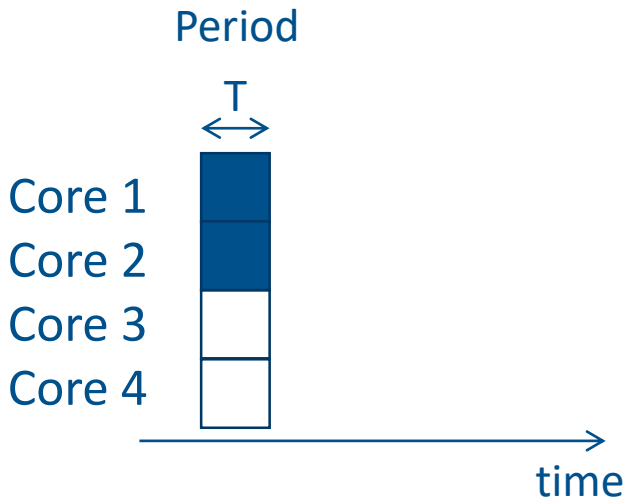
# De-stress mode



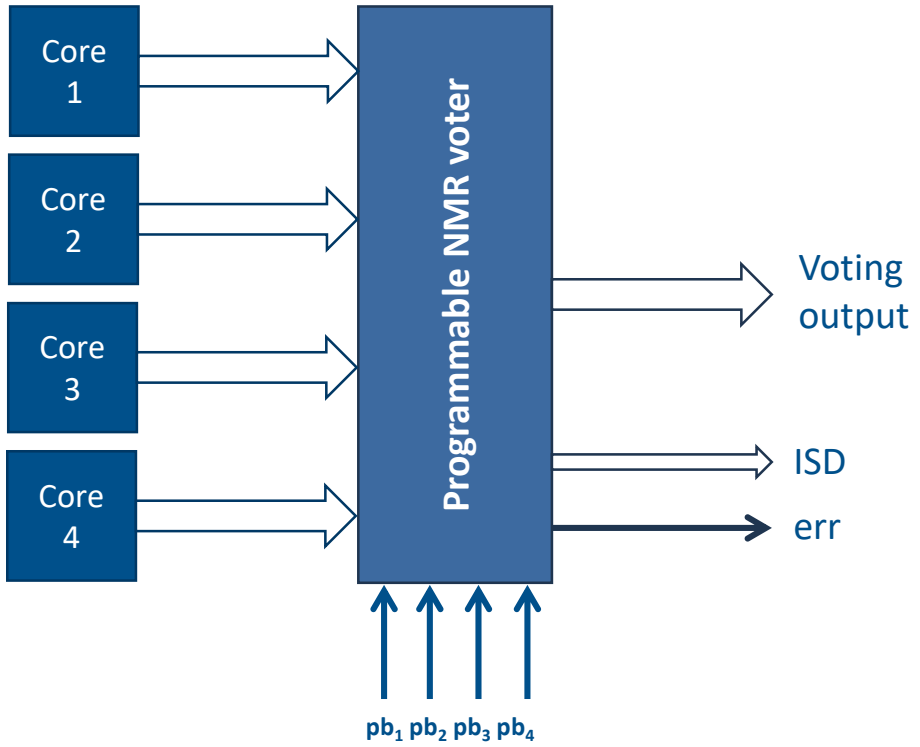
# De-stress mode (2 active cores)



# Fault-tolerant mode

- Core-level NMR – voting in each clock cycle !
- Masking faults, no need for instant recoveries for N>2
- Dynamic reconfiguration – NMR on-demand

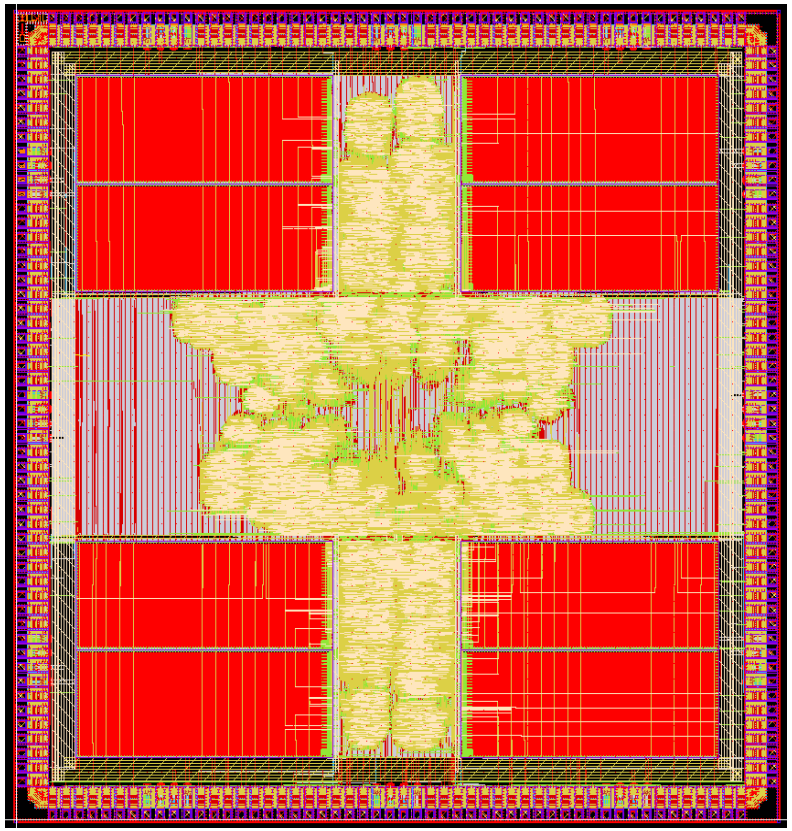


# Implementation and Results

Test ASIC named FMP implemented and tested

- 8-core system based on 32-bit internal processor
- Fully functional in IHP 130 nm technology

- Youngest-First Scheduling Methodology (YFSM) could increase the system lifetime up to 31%



A. Simevski, R. Kraemer, M. Krstic, Investigating Core-Level N-Modular Redundancy in Multiprocessors, IEEE MCSoC-14

# Resilience methods

# What is Resilience?

Resilience - „an ability to recover from or adjust easily to change” (Merriam-Webster)

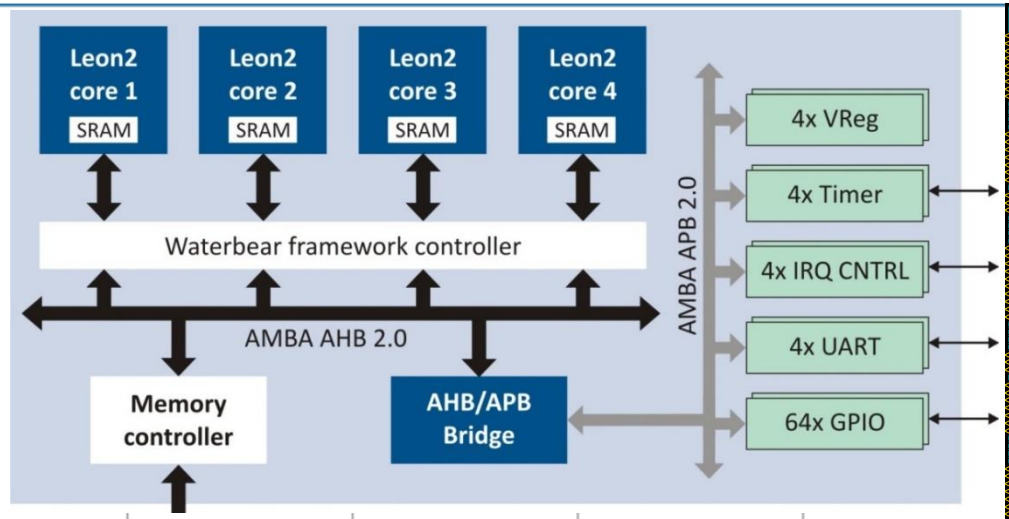
What can be this change in our digital systems?

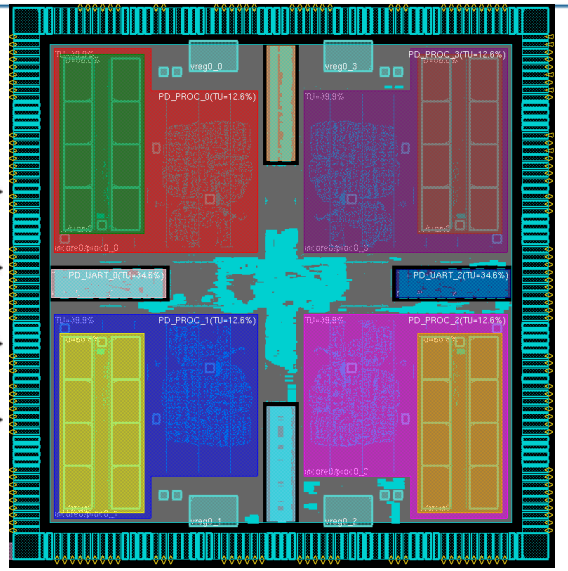
Environmental changes:

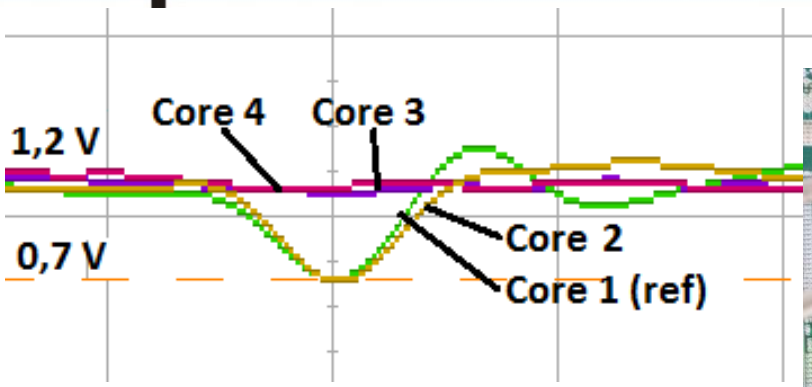
- Voltage/Temperature variations
- External effects (Radiation (SEEs))
- Ageing and manufacturing issues
- Security threats (side channel attacks)
- We need some measures to address those changes
- We already know that addressing faults will cause some overhead
  - However, addressing the other aspects also leads to overhead
  - Example: Supply management unit and its overhead
- Synergy needed in addressing those challenges!
  - In this way the **optimization of the overhead** need to be performed

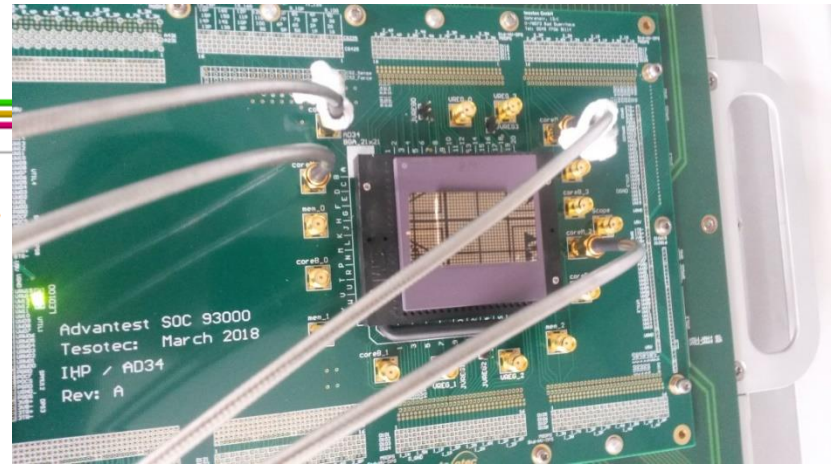
# PISA IC – Error Resilient Multi-Processor Chip

- 4-core Leon2 multiprocessor in 130 nm IHP process
- Exploring CAD tool for obtaining robust power grid
- AVS (Adaptive Voltage Scaling) capability
- Radhard library, Power Management Flow
- ~50 mm2, 300mW @ 50 MHz (tape-out: Aug. 2017)
- Fully functionally validated in Apr./Mai 2018



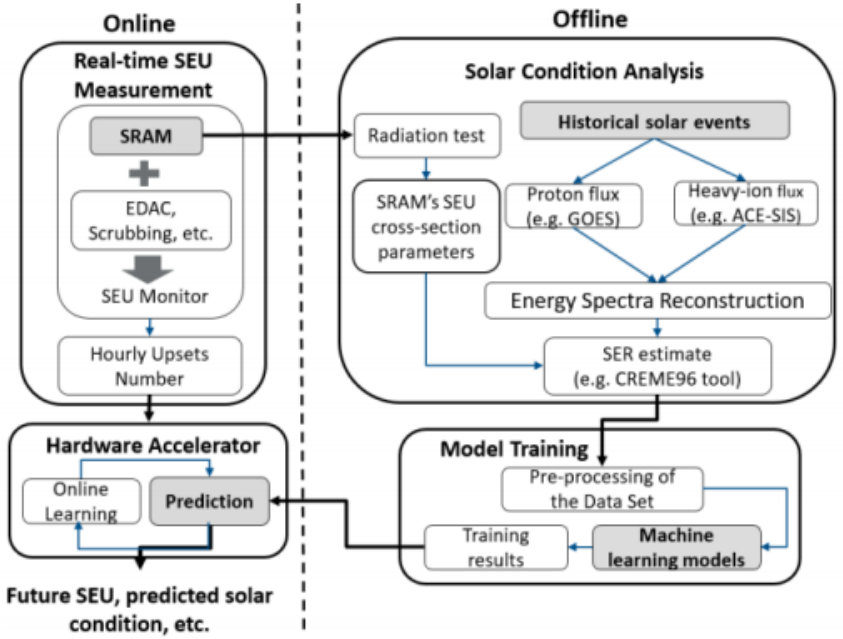



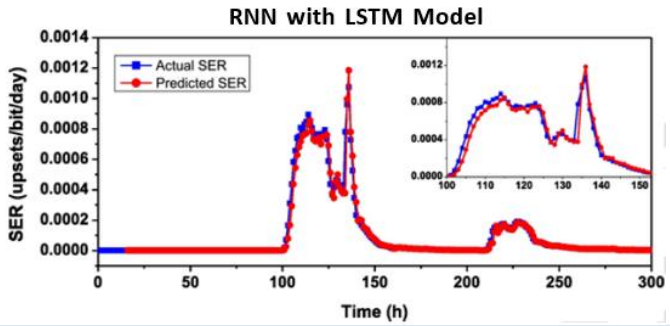


# Solar Particle Events Prediction with Machine Learning

- Solar Particle Events (SPEs) dominate the space radiation environment increasing Soft Error Upset (SEU) rate several orders of magnitude for certain time
- How to predict SPEs?
  - Analyze a data from large number of historical SPEs and Supervised-machine learning for data and model training
  - Collect the suitable SPE&SEU prediction model
- Novel SRAM-based SEU monitor for in-flight real-time hourly SEU number detection
- Customized low-cost hardware accelerator for SPE & SEU prediction
- Achieved: Prediction of SPEs 1 hour in advance




J. Chen, T. Lange, M. Andjelkovic, A. Simevski, L. Lu and M. Krstic, "Solar Particle Event and Single Event Upset Prediction from SRAM-based Monitor and Supervised Machine Learning," in IEEE Transactions on Emerging Topics in Computing, 2022

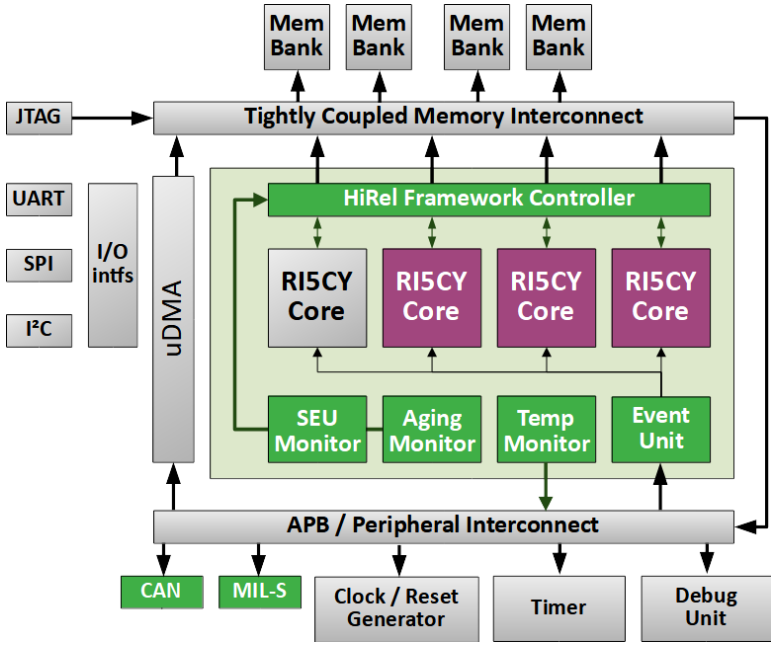
# Open Hardware Approach: TETRISC SoC

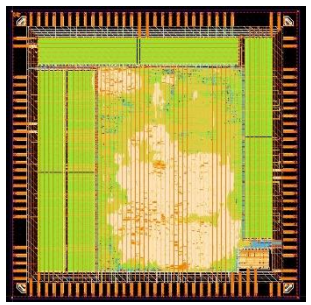
**The TETRISC SoC** - a **smart highly reliable RISC-V based multiprocessor platform**, suitable for harsh environments (such as aviation, space, etc.)

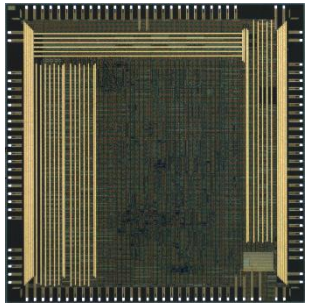
- RISC-V based adaptive quad-core SoC
- Based on the open-source single-core microcontroller architecture PULPissimo
- Multiple on-chip monitors (SEU, Temperature, Aging)
- Smart framework controller for on-line system adaption
- Dynamic trade-off between reliability, performance and power consumption

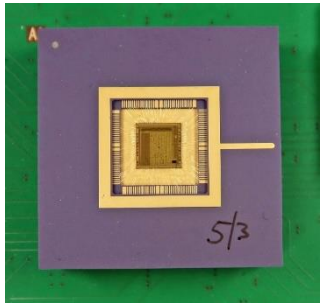
**Chip Specs**

- **Area** - 43,56 mm2 (6.6*6.6mm), **Nominal clock frequency** - 30MHz, **Power consumption** - <1W (estimated), **Memory** - 4*8192*40 Bit SRAM, **Pads** - 81 Signal pads, 35 others



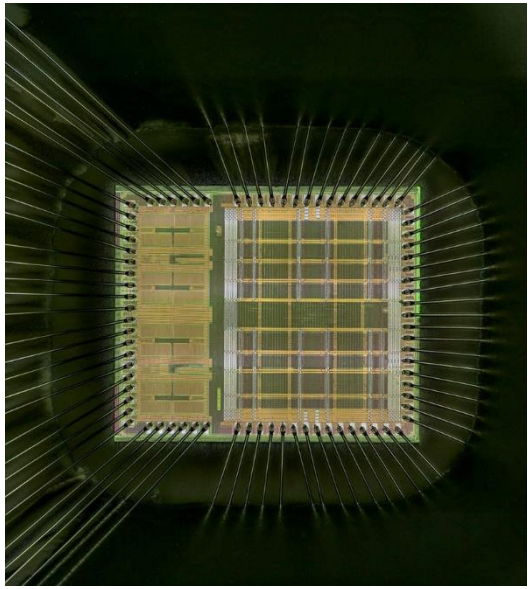







# Chirp-IC

- Chirp Transform Spectrometer
  - 2-Chip solution
  - can determine the composition of Jupiter's stratosphere, for example, by analysing spectra



**IHP chips fly to Jupiter**

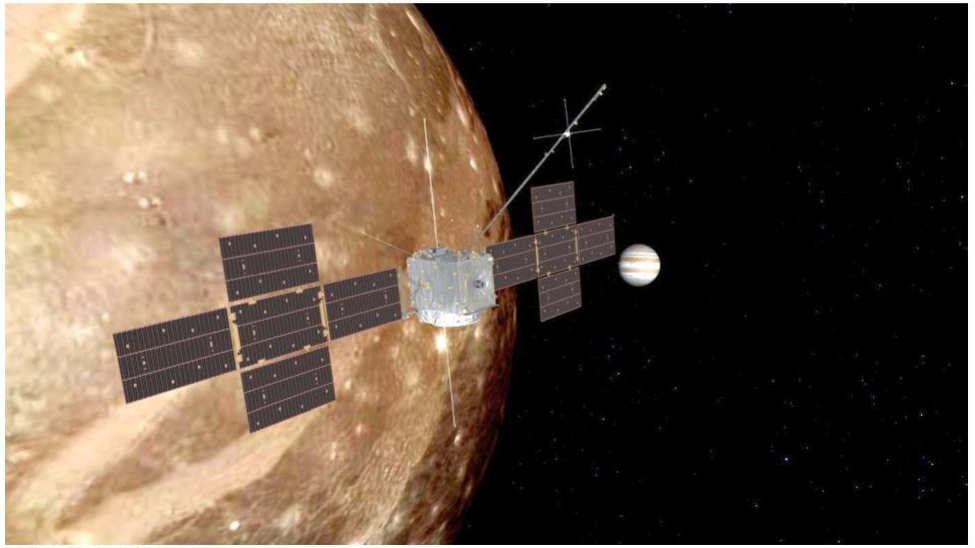
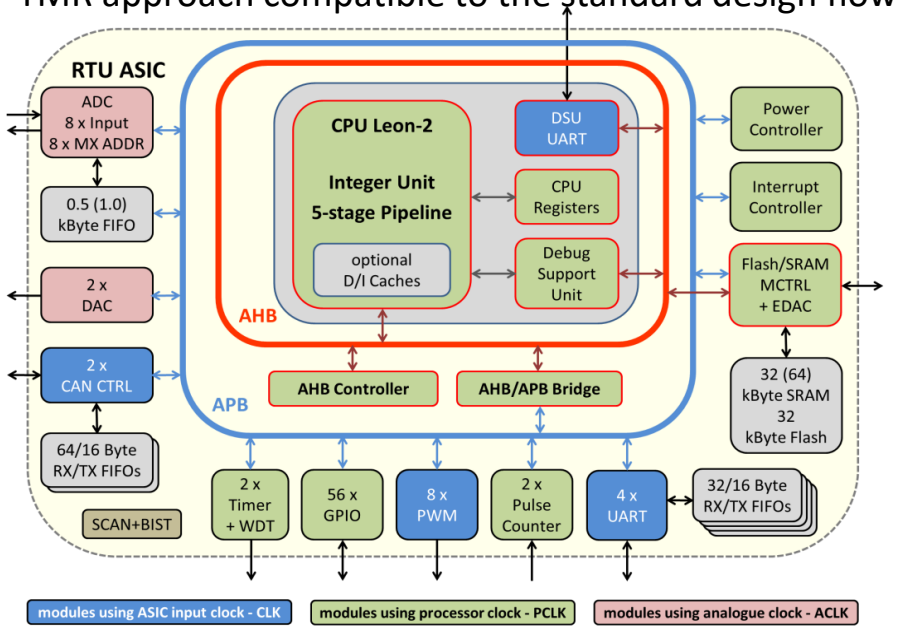
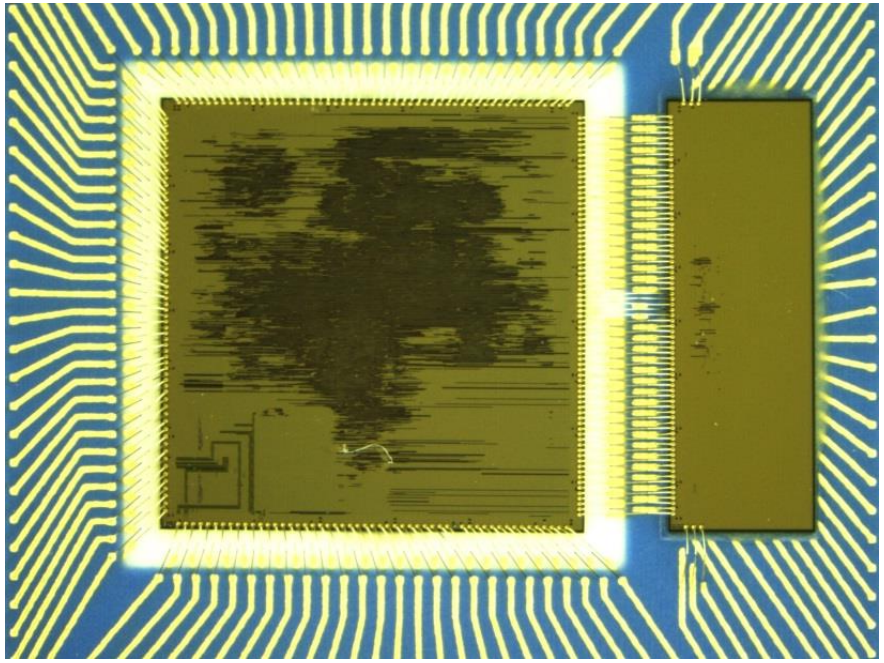


Photo ESA (ATG MEDIALAB)

# Example Space ASICs: Development of the RTU ASIC Chip

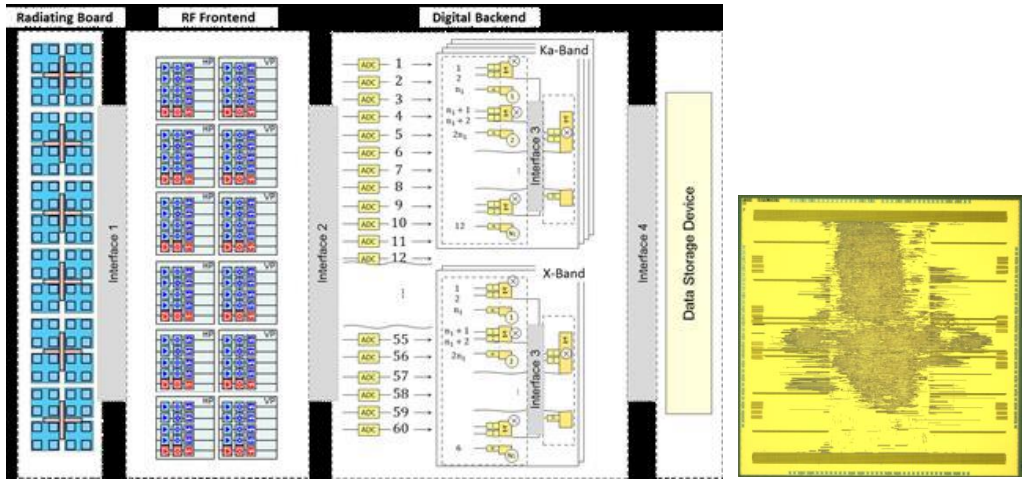
- Remote Terminal Unit ASIC under development for small satellite applications
- Complex mixed-signal dual-chip in package solution
- Target technology – internal 0.25 um CMOS
- Tape out Feb 2015 – fully functional confirmed measurements!
- Radiation hardness  based on radhard TMR library of flip-flops
  - TMR approach compatible to the standard design flow



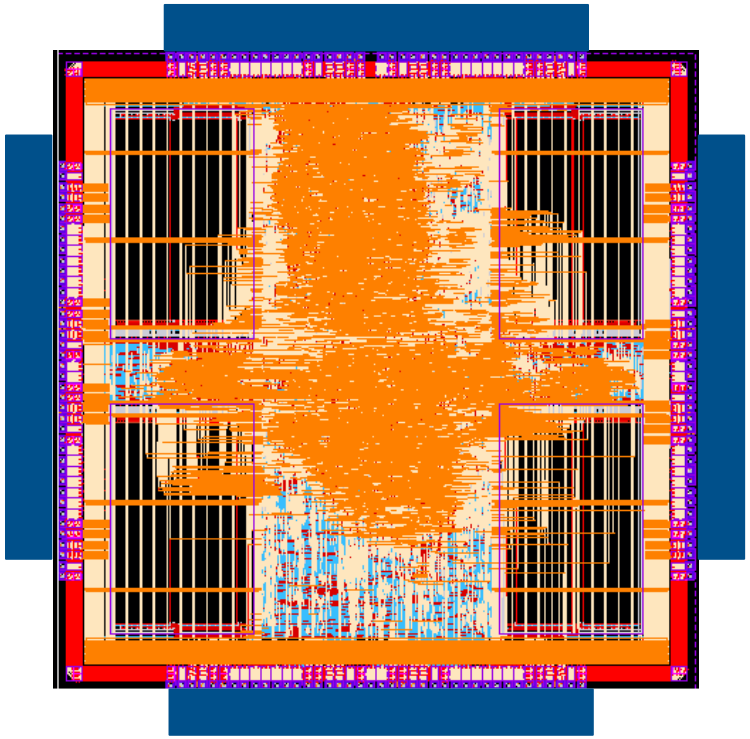



# Example Space ASICs:
# DBFN Baseband Processor for Synthetic Aperture Radar

- The DIFFERENT project tackles the development of low-cost highly-integrated compact radar for formation flying multistatic SAR applications.
- IHP is designing DFBN baseband chip in SGB25V technology
  - This chip includes high-speed processing and IO interfaces
- Fabrication of digital baseband IC and RF MMICs in IHP technologies
  - DFBN Chip tape-out Aug 2015 – 46 mm2 in SGB25V
  - Tested on wafer and operational up to 250 MHz!
  - Optimized overhead (reduced by 20% in area and 33% in power)
    - radiation hardened flip-flops in control logic
    - Standard flip-flops in datapath



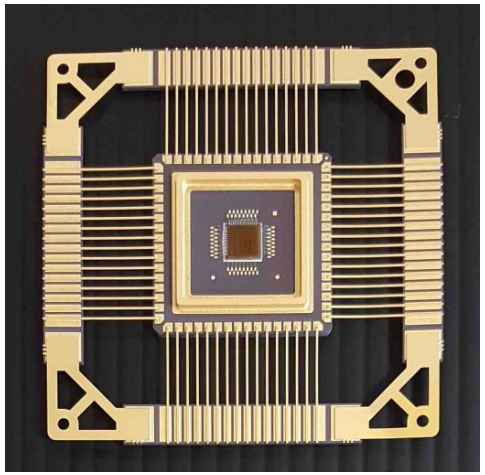

Architecture of RadarModule in DIFFERENT

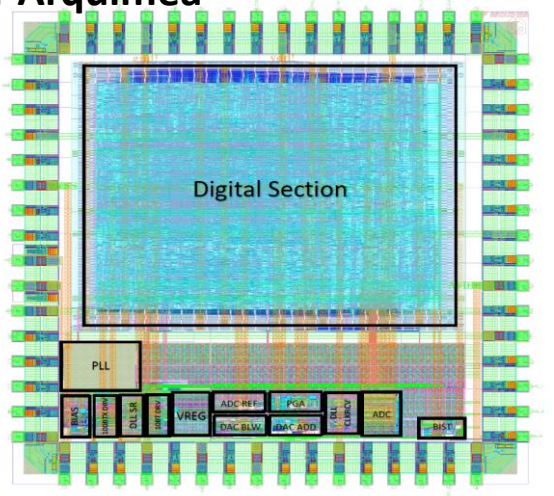


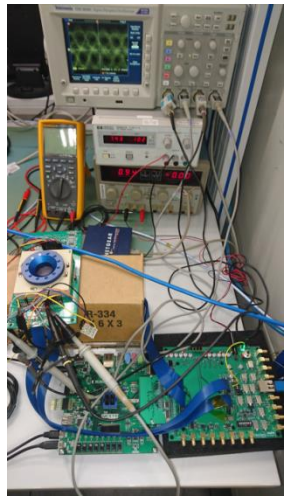
DBFN Baseband Processor - 46mm² in SGB25V, Sep 2015

# Example Space ASICs:
# EU Project SEPHY – Space Ethernet Physical Layer Transceiver

- Radiation hardened 10/100 Ethernet physical layer transceiver for the space market
- SEPHY Chip
  - 150 nm CMOS process, ATMEL radhard PDK
  - IHP responsible for digital IP design and verification
  - **10 BaseT/100BaseTx PHYs fully functional**
  - **Radiation hardness confirmed at the end of 2018**
    - 100 Krad TiD – no effects on BER
    - SEE Tests has shown Mean Time Between Failure (MTBFs) of 940 years
  - **Commercialization steps currently planned with coordinator Arquimea**

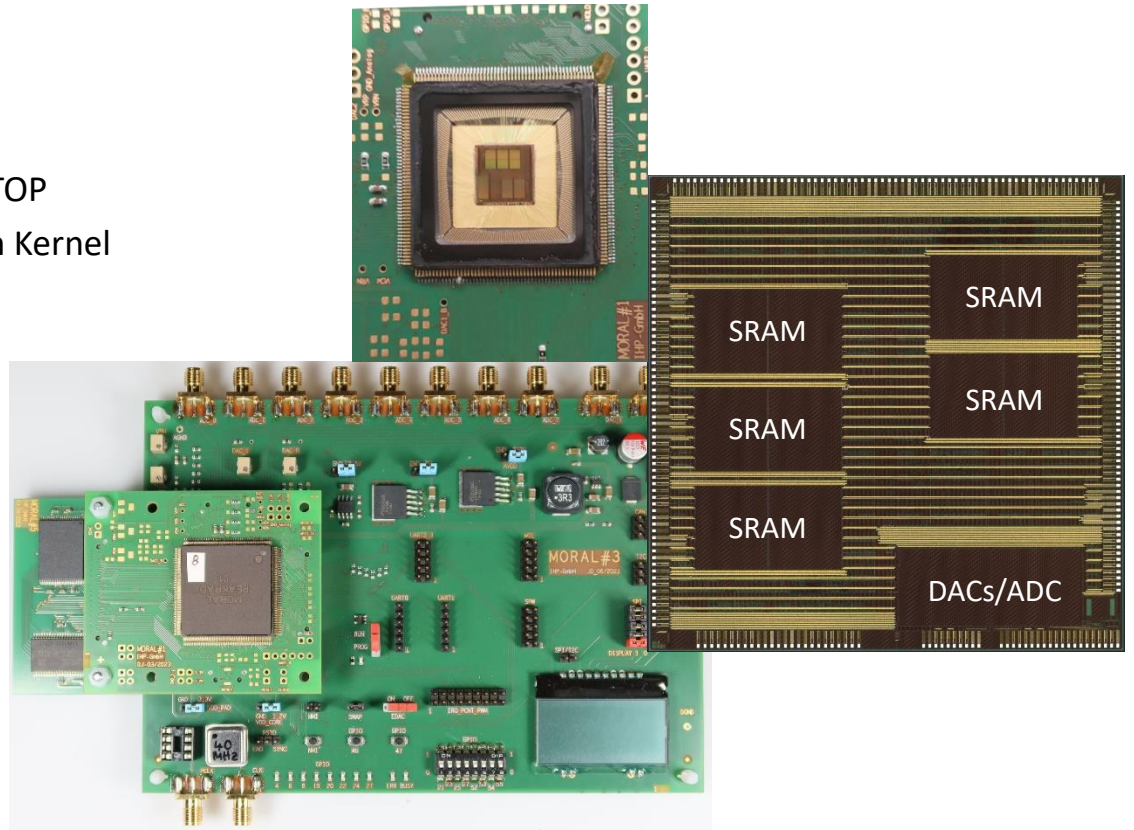




# MORAL - Export-free Rad-hard Microcontroller for Space Applications

- Microcontroller – **Peakrad SG13RH (S)**
  - IHP's PEAKTOP architecture
  - Rad-Hard ADC, DAC, and SRAM
  - **Achieved TRL-6!**
- Software Toolchain
  - C Compiler for PEAKTOP
  - Real-Time Separation Kernel

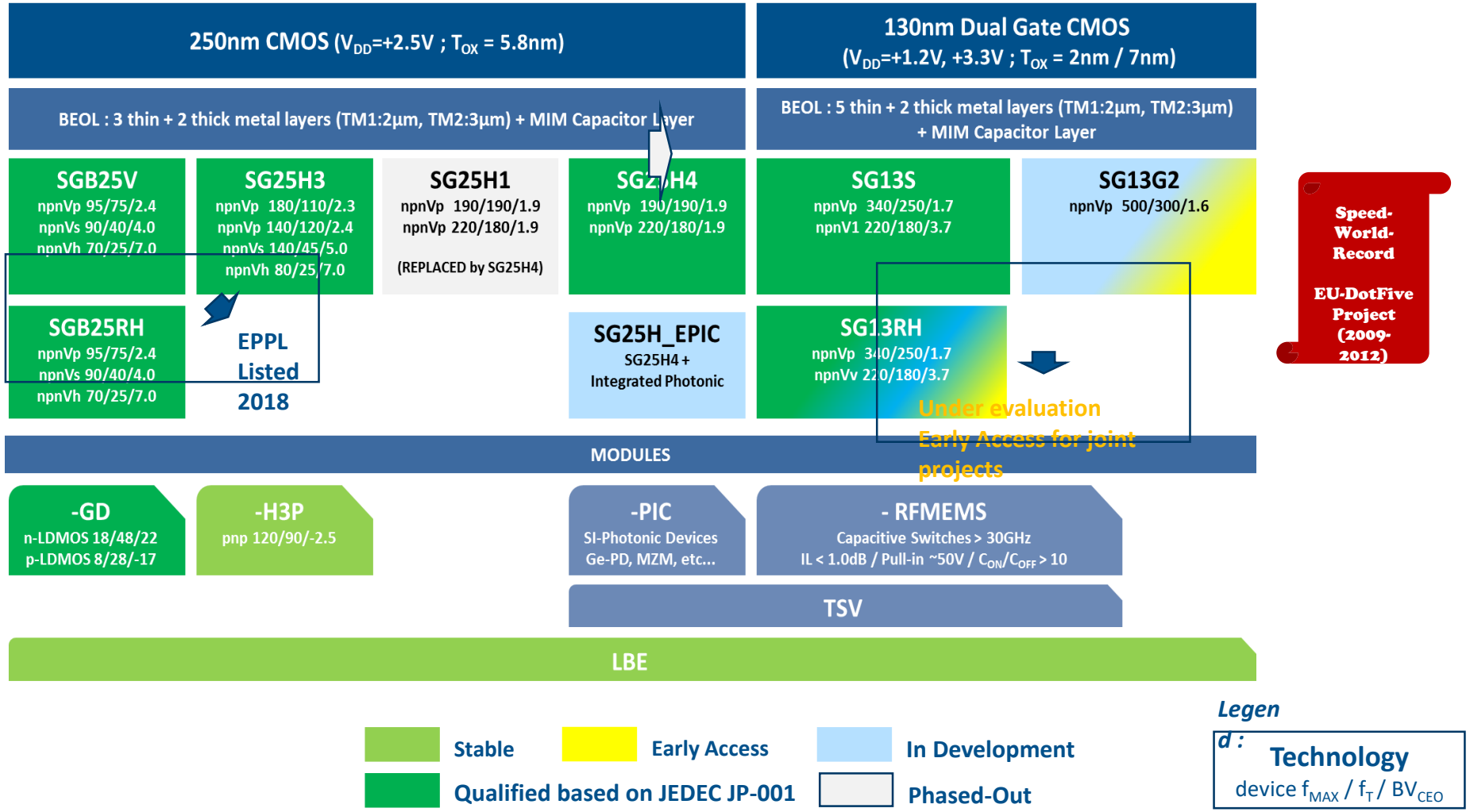



- Outstanding achievements
  - Highly complex ASIC– **70.56 mm²**
  - Demonstrator board
  - Embedded ADC/DACs with superior performance (12b)
  - All devices passed successfully 1000h life testing
  - Irradiation tests
    - Total ionizing dose (TID) **106 krad (Si)**
    - Single event latch-up (SEL) **62,5 MeVcm²/mg**
    - Very low single event upset (SEU) rate and T>**15 MeVcm²/mg**

MORAL microcontroller is suitable for **any space mission orbit and duration!**

Confirmation of our radhard designflow and cornerstone for future activities

# IHP SiGe BiCMOS Technologies for Space Applications



# IHP Processes and PDKs for Space Applications

## Summary I of III

## Status: 2024

| | SGB25V/RH | SG13S/RH |
|---|---|---|
| ■ **Process Description** | SiGe HBTs npn Peak $f_T$ /$f_{MAX}$ 75/95GHz<br>250nm CMOS<br>($V_{DD}$=+2.5V;$T_{OX}$ = 5.8nm) | SiGe HBTs npn Peak $f_T$ /$f_{MAX}$ 220/340GHz<br>130nm Dual Gate –Oxide CMOS<br>($V_{DD}$=+1.2V, +3.3V ; $T_{OX}$ = 2nm / 7nm) |
| ■ **Applications** | **Mixed-Signal MMIC/ASICs<br>up to Ku Band** | **Mixed-Signal MMIC/ASICs<br>up to W-Band** |
| ■ **Commercial Qualification**<br>– Based on JEDEC Standard JP001.01<br>– EPPL/QML/QPL (ESCC QPL, ESCC QML, MIL QPL, JAXA QPL) | **Re-Qualified 2010<br>active & stable > 10 years (2005)**<br><br>**EPPL Listed 2018** | **completed 2014**<br><br>EPPL under preparation |
| ■ **Radiation Assessment (Analog)**<br>■ HBT npn (all devices)<br>■ PMOS<br>■ NMOS (WG=1µm)<br>■ ELT-NMOS (RHBD Device) | **completed**<br>PASS TID 800krad(Si) no ELDRS<br>TID > 550krad(Si)<br>PASS TID 100krad(Si)<br>Characterized up to 500krad(Si)<br>TID > 550krad(Si) | **completed**<br>PASS TID >1210krad(Si) no ELDRS<br>TID > 200 (HV) / 500 (LV) krad(Si)<br>PASS TID 50krad(Si) (LV)<br>Characterized up to 500krad(Si)<br>TID > 900krad(Si) |

# IHP Processes and PDKs for Space Applications

## Summary II of III

## Status: 2024

| | SGB25V/RH | SG13S/RH |
|---|---|---|
| ■ PDK Availability<br>■ Access Status | completed<br>NDA/EXPORT License | In development -Early Access<br>NDA/EXPORT License |
| ■ CMOS Std Cell Core and IO Libraries | Dolphin SESAME2-LP core cells + special RHBD cells (IHP)<br>(80 cells)<br><br>Saphyrion SAGL (25 cells)<br>(Tested for SEU/SEL only) | IHP IXC013RH (~ 90 cells) |
| ■ Radiation Assessment (Digital)<br>■ TID<br>■ CMOS Libraries | 100krad(Si) – 300krad(Si)<br>SEU/SEL completed<br><br>SEL Threshold > 65MeV/cm²/mg<br>(RHBD IHP cells)<br><br>SEU Threshold > 30MeV/cm²/mg<br>(IHP RTMR FF) | 100krad(Si) – 300krad(Si)<br>SEU/SEL completed<br><br>SEL Threshold > 65MeV/cm²/mg<br>(RHBD IHP cells)<br><br>SEU Threshold > 30MeV/cm²/mg<br>(IHP RTMR FF) |

# IHP Processes and PDKs for Space Applications

## Summary III of III

## Status: 2024

| | SGB25V/RH | SG13S/RH |
|---|---|---|
| ■ **Evaluation Testing**<br>■ **in acc. ESCC No. 2269010** | **completed** | **ongoing** |
| ■ **Operation Temperature (max rated $T_J$)** | **-55°C to +125°C** | **-55°C to +125°C (TBC)** |
| ■ **Test Vehicles**<br>■ in acc. ESCC No. 2269010 | **TCV, DEC-I/-II, RIC** | **TCV,**<br>**DEC –I DEC-II(CMOS, Bipolar)**<br>**RIC** |
| ■ **Radiation Tests**<br>■ TCV (Devices, analog)<br>■ DECs (Digital, Analog BiCMOS)<br>■ RIC (Mixed-Signal IC) | **completed**<br>„<br>DEC-I (SEU/SEL), Early structures<br>TID + SEE LO RIC | **completed**<br>„<br>DEC-I (SEU/SEL), Early structures |
| ■ **Endurance Testing HT & RT**<br>■ HBT npn- devices<br>■ HBT lifetime determination<br>■ CMOS devices<br>■ CMOS Core & IO Std Cell Library | **passed**<br>very stable : no or low drifts<br>characterization available<br>drifts are mesured and defined<br>lifetime determination ~ 20 years | **ongoing** |
| ■ **Additional Tests (Reliability)** | **SiGe HBT HCI & Lifetime Estimation** | **SiGe HBT HCI & Lifetime Estimation** |

# Conclusion

- Designing digital systems for space requires additional design steps
- Changes of the design flow are present from modeling, over library design to the general design flow and used architectures
- Most of the solutions are based on fault tolerance that always causes significant hardware & power overhead
- Different methods how to limit this overhead exist
  - Static techniques for reducing power overhead, but also reducing fault protection
  - Adaptive techniques enabling dynamic trade-off power-reliability
- Design examples have been provided
  - IHP technology is evaluated for the space applications

Special thanks to current and former members of my team that contributed to slides: Vladimir Petrovic, Aleksandar Simevski, Markus Ulbricht, Anselm Breitenreiter, Rizwan Syed, Felipe Kuentzer, Steffen Weidling, Patryk Skoncej, Yuanqing Li, Oliver Schrape, Junchao Chen, Li Lu

# Thank you for your attention!

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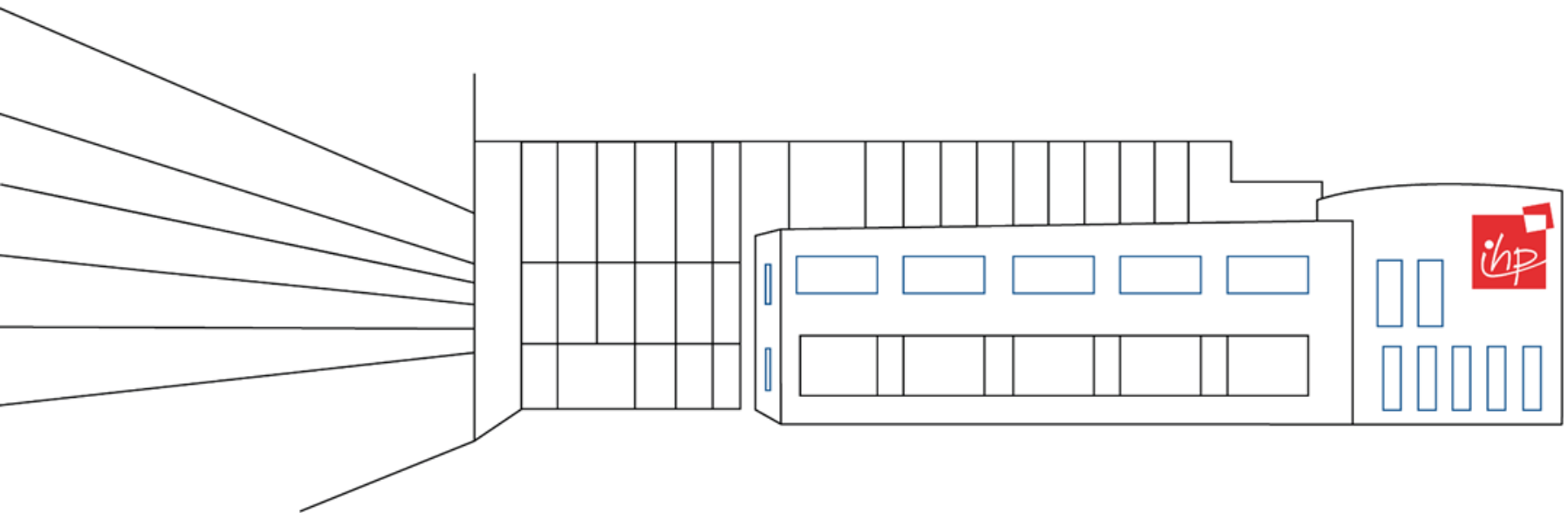

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