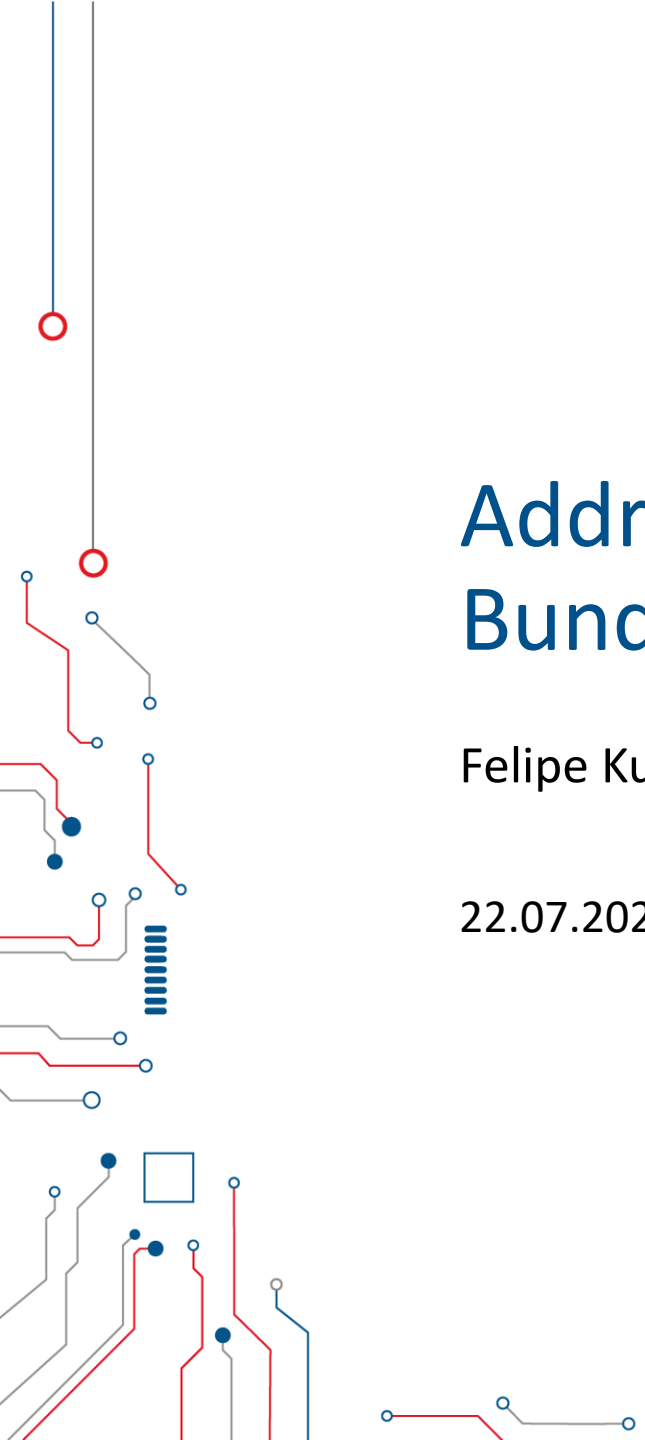

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Addressing Soft Errors in Asynchronous Bundled Data Design

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22.07.2025

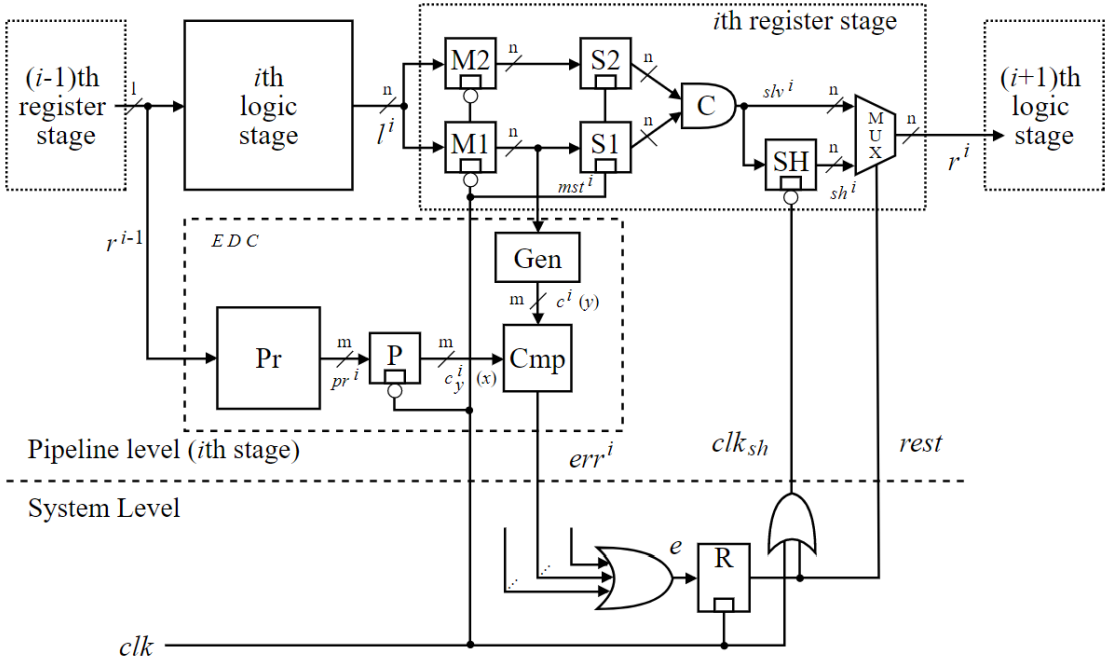
Context: Fault Tolerant Solutions

- Space redundancy
  - Triple modular redundancy (TMR)
- Time redundancy
  - Speculative operation
- Gate sizing, glitch filtering, and radiation-hardened cell libraries

- Limitations
  - Partial protection against soft errors
    - Sequential logic (SEU - Single Event Upsets) or combinational logic (SET - Single Event Transient)
  - Limited detection window
    - Unable to tolerate long pulse widths – **4.5ns**
  - TMR is effective but not very efficient (area, power and time overheads)
  - High recovery penalties
  - Metastability problems

Context: Baseline Work

- Full Error Detection and Correction – FEDC [Krstic et al., 2016]
  - Fault tolerant master-slave flip-flops for sequential logic
  - Error Detection Circuit - EDC
  - Soft errors of arbitrarily long duration



M. Krstic et al., "Enhanced Architectures for Soft Error Detection and Correction in Combinational and Sequential Circuits", Microelectronics Reliability, vol. 56, pp. 212-220, Jan 2016.

Context: Why Asynchronous?

- Self-adapting properties associated with data transferring
- Data sampling controlled locally
  - Error recovery can also be handled locally
- Data can be re-sampled and re-checked for an indefinite period
  - Longer SETs are easily handled
- Metastability issues are better handled in asynchronous designs
  - The circuit naturally waits for the metastability to resolve

An asynchronous design is a more natural and practical approach for soft error resilient architectures, which could be a go-to application for asynchronous designs

- Main Goals

(1) Prevent metastability problems

(2) Better handle SETs of unbounded duration locally

(3) Reduce error correction time penalties

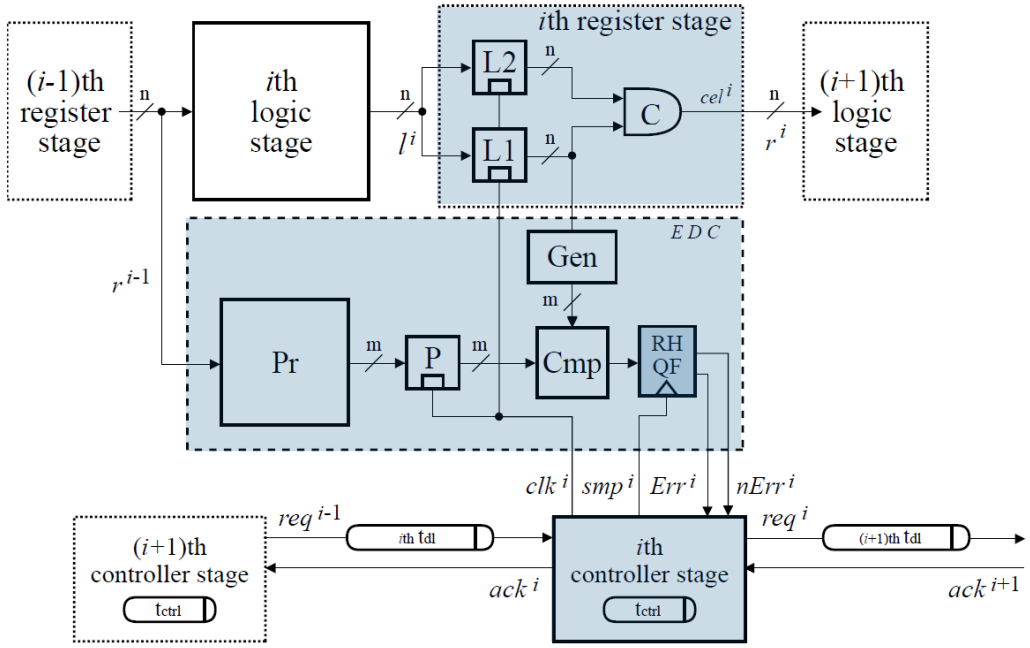
(4) Reduce power and area

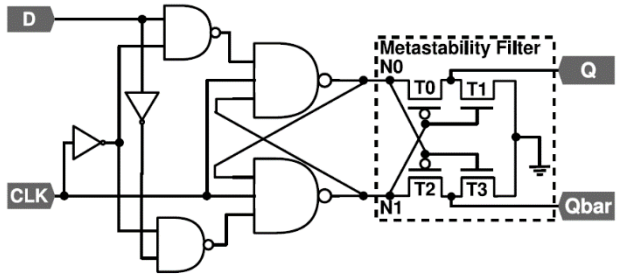
Outline

- Asynchronous Full Error Detection and Correction - AFEDC
  - AFEDC Click Controller
  - Radiation-hardened Click Controller
  - Performance Metrics and Timing Constraints
  - Design Flow – Desynchronization
  - Experiments and Results
- Addressing SEMT in RH-Click Controllers
  - Proposed Approach
  - Approach Evaluation
    - SEMT Fault Experiments
    - Layout Impact
- Conclusions and Future Works

Asynchronous Full Error Detection and Correction - AFEDC

- Soft error resilient stage
  - Latch-based register
    - Dual Modular Redundant - DMR
    - C-element as voter
  - Bundled-data controller
    - 2-phase protocol
    - Click design
  - Error Detection Circuit - EDC
    - Partial Duplication with Parity Prediction - PDPP
    - Full Duplication and Correction - FDC
    - Q-Flop - QF



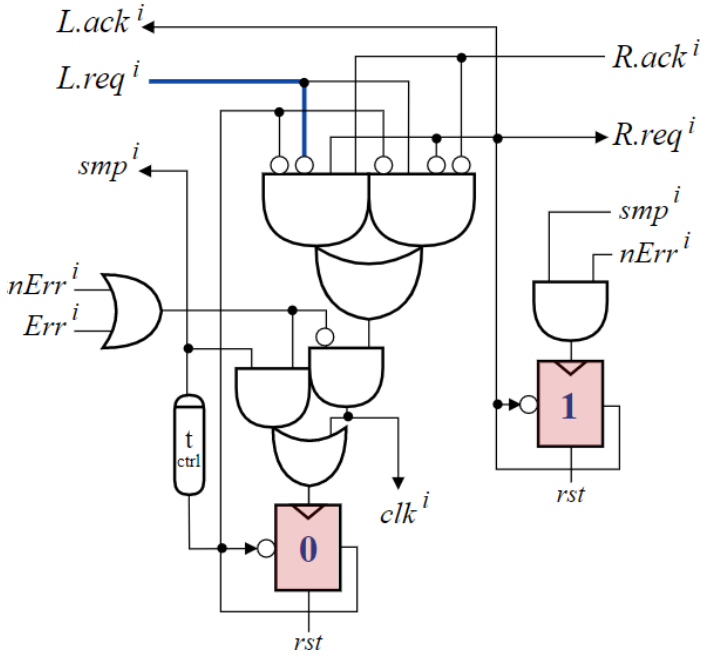


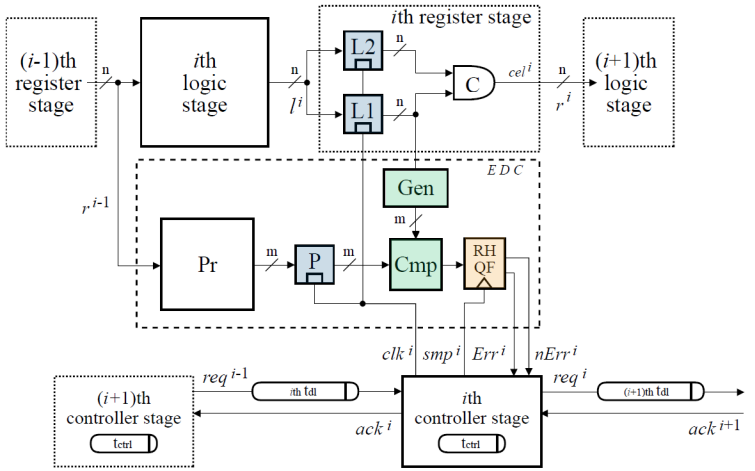
CLK	D	Q	Qbar
0	0	0	0
0	1	0	0
↑	0	0	1
↑	1	1	0

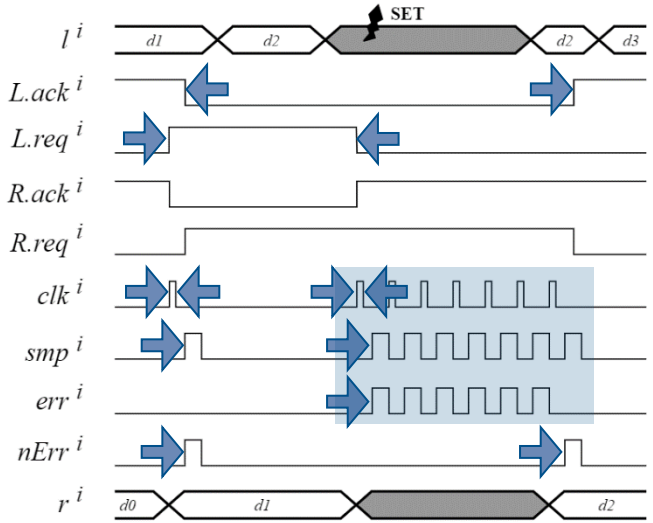
F. A. Kuentzer and M. Krstic, "Soft error detection and correction architecture for asynchronous bundled data designs", TCAS-I, vol. 67(12), pp. 4883-4894, 2020.

AFEDC Click Controller

- Why Click?
  - Relies on flip-flops to build the state machine
    - Natural valid start and endpoints for its logic paths
  - Better compatibility with commercial EDA
    - Static timing analysis

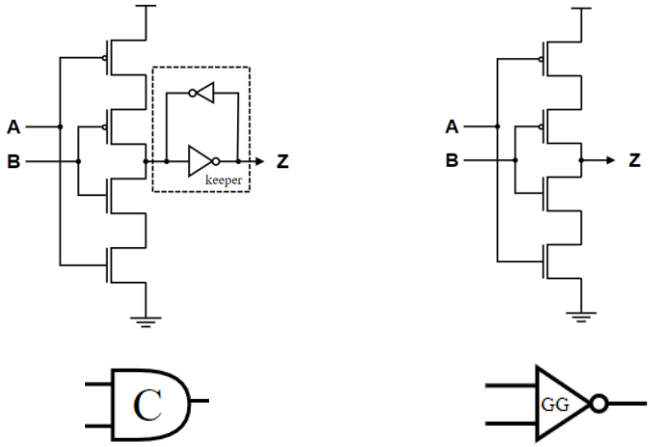


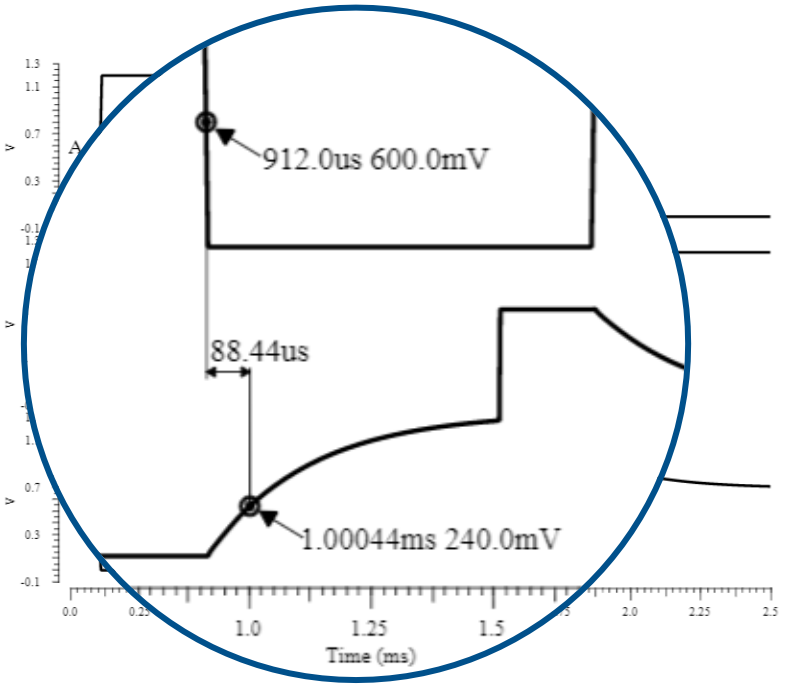




RH-Click Controller

- Guard Gates - GG
  - Protect the controller against SET and SEU faults
  - Similar to a C-element, but without the keeper
    - Output only changes when the inputs have the same value
    - Holds previous state if inputs differ
  - Output degrades due to leakage current
  - Degradation is in the micro-seconds range (IHP 130nm)

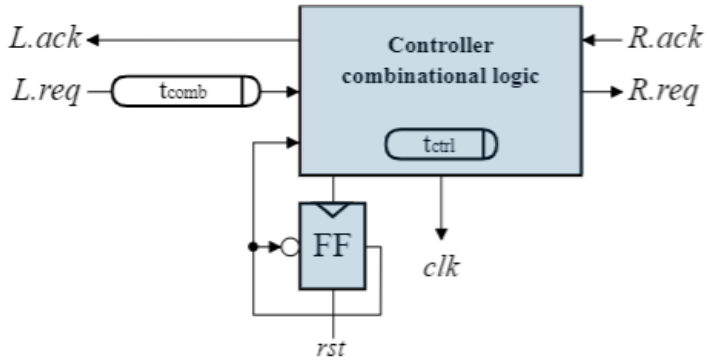


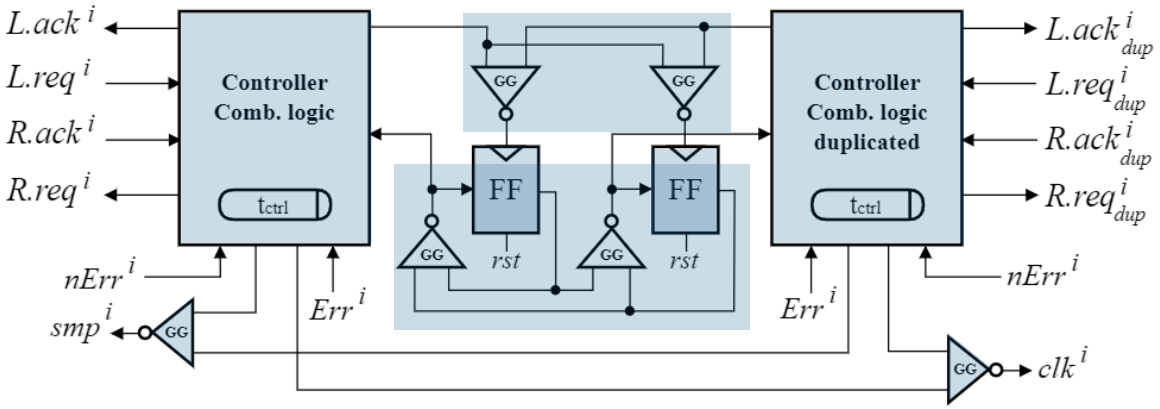


F. A. Kuentzer, M. Herrera, P. A. Beerel, O. Schrape, and M. Krstic, "Radiation hardened click controllers for soft error resilient asynchronous architectures", ASYNC, Mar. 2020, pp. 1–8.

RH-Click Controller

- Generalized approach for Click controller
  - (1) Duplicate the combinational logic and delay lines
  - (2) Duplicate FFs
  - (3) Cross-couple equivalent FFs outputs with GGs
  - (4) Cross-couple equivalent FFs clock inputs with GGs
  - (5) Add GGs for “voting” equivalent control outputs



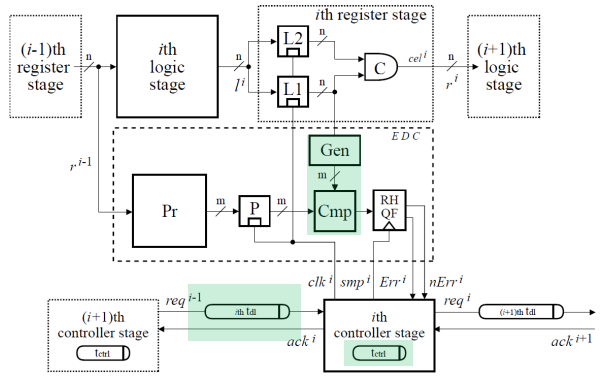


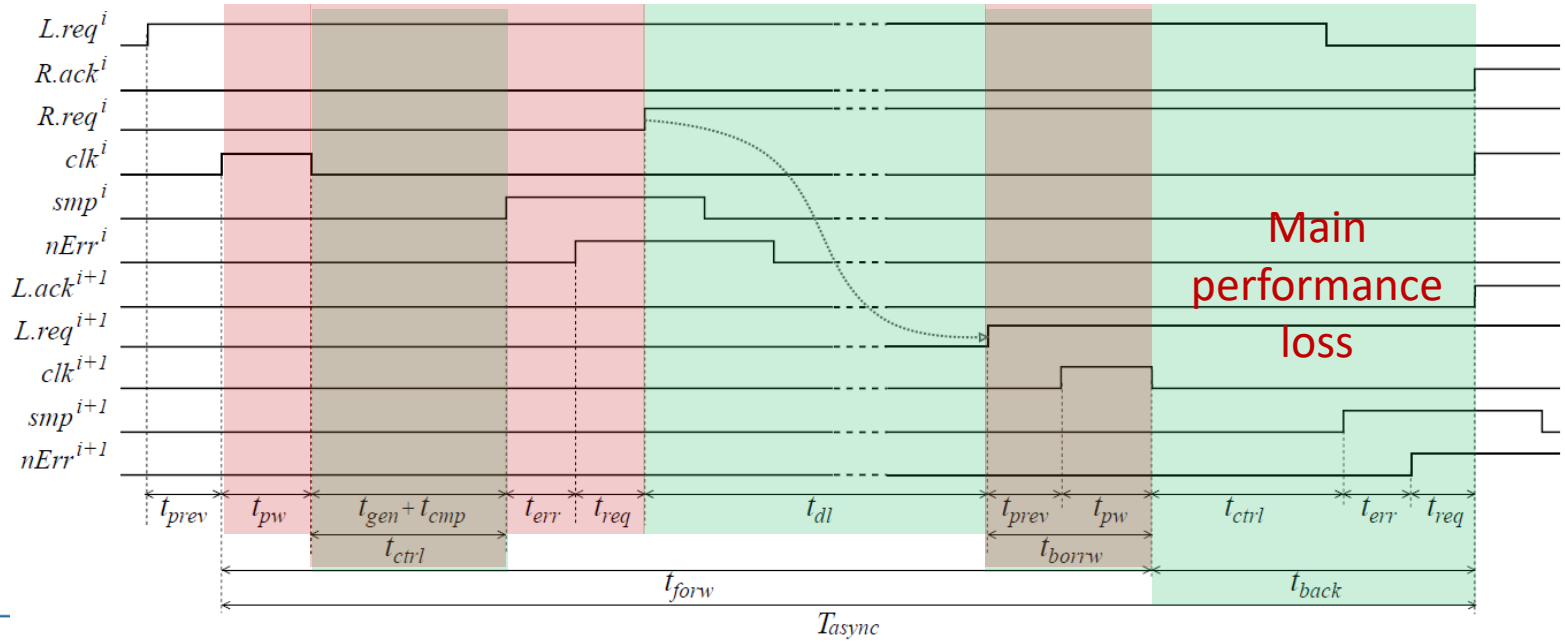
F. A. Kuentzer, M. Herrera, P. A. Beerel, O. Schrape, and M. Krstic, "Radiation hardened click controllers for soft error resilient asynchronous architectures", ASYNC, Mar. 2020, pp. 1–8.

Performance Metrics and Timing Constraints

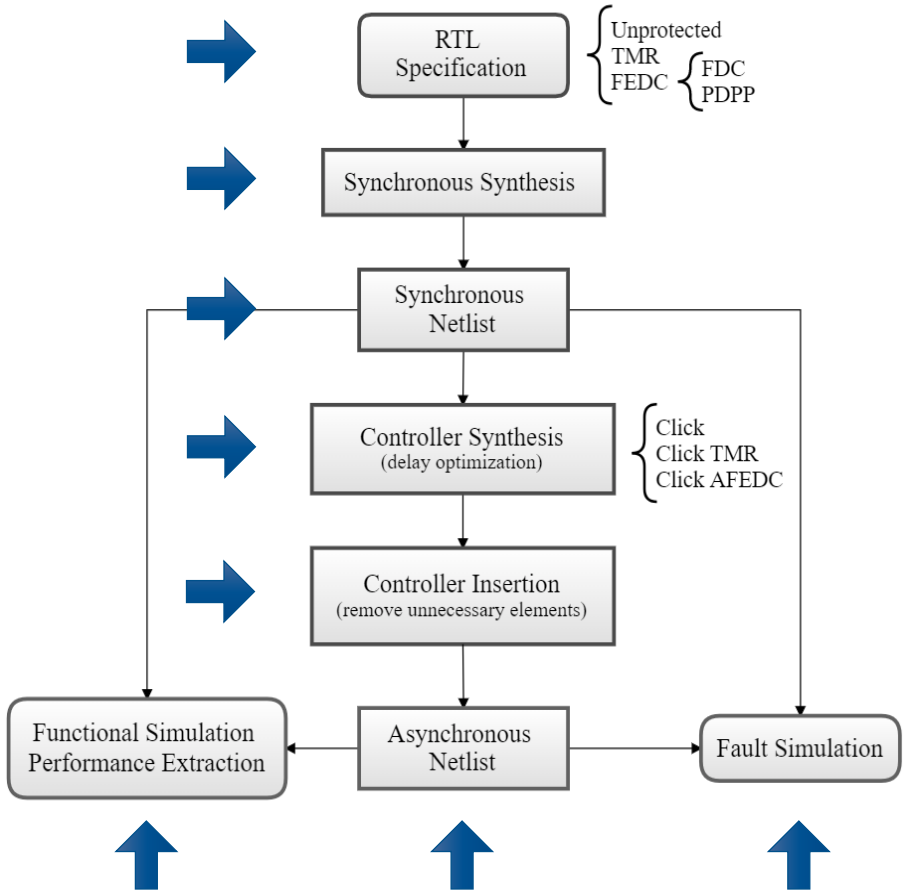
- There are three main metrics for performance evaluation
  - Forward latency $t_{forw} = t_{ctrl} + t_{comb}$
  - Backward latency $t_{back} = t_{ctrl} + t_{err} + t_{req}$
  - Cycle time $T_{async} = t_{forw} + t_{back}$

$t_{ctrl} \geq t_{gen} + t_{cmp}$ $t_{dl} = t_{comb} - (t_{pw} + t_{ctrl} + t_{err} + t_{req} + t_{borrw})$ $t_{borrw} = t_{prev} + t_{pw}$





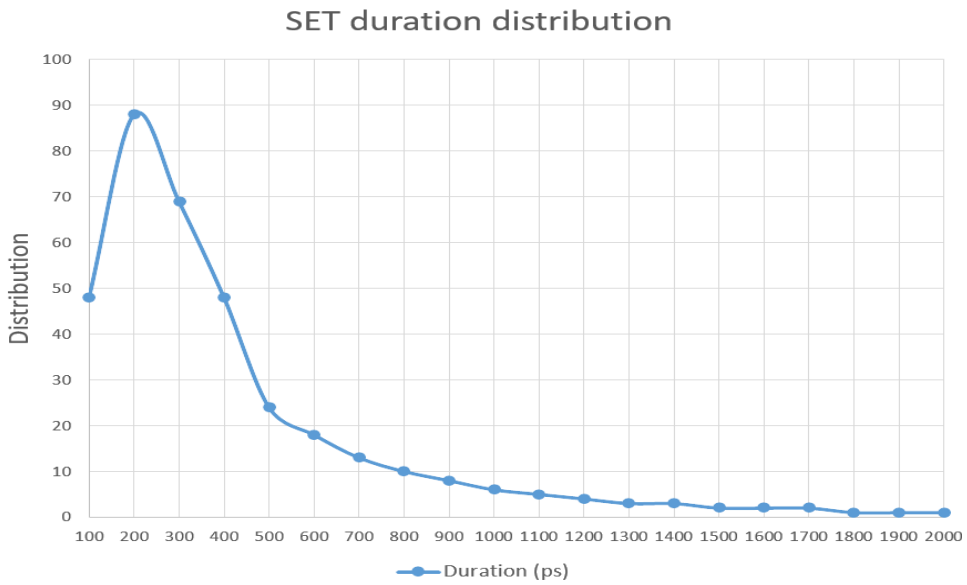
Design Flow – Desynchronization



- Synopsys and Cadence Tools
- Start with an RTL description
  - Unprotected
  - Full Duplication and Correction – FDC
  - Partial Duplication with Parity Prediction – PDPP
  - Triple Modular Redundancy – TMR
- Asynchronous controller synthesis
  - Unprotected - original Click
  - TMR - triplicate original Click
  - AFEDC used the RH-Click
- Asynchronous conversion
  - Clock tree is replaced by controllers
  - Remove FEDC unnecessary elements
  - Insert Q-Flop
- Fault and performance simulations

Fault Simulation

- Cadence Incisive Functional Safety Simulation – IFSS
- IFSS Elaborate
  - Fault list – specify target modules and exclude faults
  - Support for SEUs and multiple SETs (single duration)
- IFSS Good simulation
  - Strobe list – specify observation points (functional and checkers)
  - Random generates fault injection time for all paths
- Script to generate random SET duration (custom distribution)
  - Script to modify SET duration
- IFSS Fault simulation
  - Inject all instrumented faults
- Fault reports
  - IFSS + Testbench



Fault Simulation

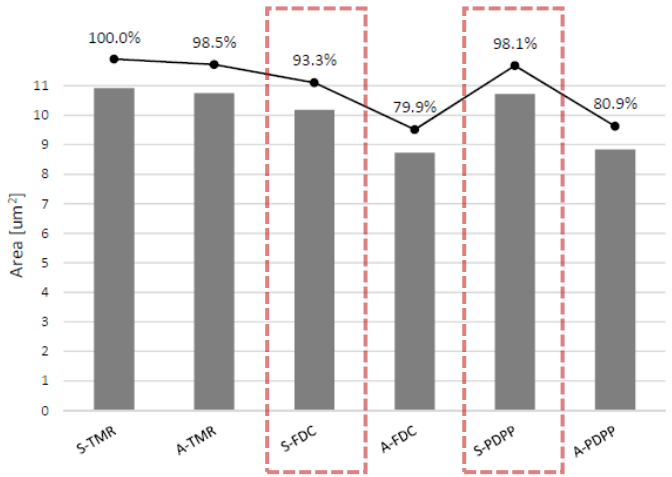
- Test cases
  - Two linear pipelines
  - 1-stage 32-bit adder **SDAdder**
    - Same circuit used to evaluate the synchronous FEDC
  - 5-stage 32-bit non-restoring array divider **PNA-Divider**
    - Larger circuit to evaluate how the different designs scale
- IHP 130nm technology process
- Q-Flop cell not available
  - Implemented with a standard FF and additional circuit to mimic its behavior
  - No metastability filter
- Evaluated circuits for each test case
  - S-Unprotected, A-Unprotected
  - S-TMR, A-TMR
  - FEDC-FDC, AFEDC-FDC
  - FEDC-PDPP, AFEDC-PDPP

Experiments and Results

Area evaluation

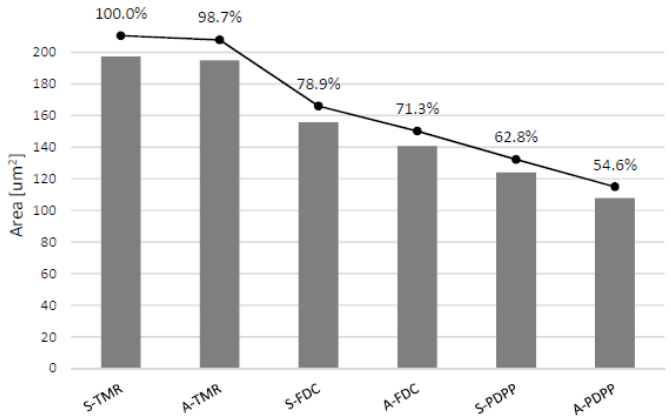
SDADDER COMPARISON OF SYNCHRONOUS AND ASYNCHRONOUS SOLUTIONS IN TERMS OF AREA.

Circuits	Area [μm^2]			Area normalised (A / A_{TMR})
	Comb.	Reg.	Total	
S-TMR	6.24	3.63	10.91	1
A-TMR	7.06	2.09	10.75	0.985
FEDC-FDC	4.28	3.77	10.18	0.933
AFEDC-FDC	4.08	2.27	8.73	0.799
FEDC-PDPP	4.54	3.81	10.71	0.981
AFEDC-PDPP	4.13	2.31	8.83	0.809



PNA-DIVIDER COMPARISON OF SYNCHRONOUS AND ASYNCHRONOUS SOLUTIONS IN TERMS OF AREA.

Circuits	Area [μm^2]			Area normalised (A / A_{TMR})
	Comb.	Reg.	Total	
S-TMR	119.11	28.35	197.33	1
A-TMR	124.77	16.07	194.83	0.987
FEDC-FDC	81.02	29.32	155.60	0.789
AFEDC-FDC	77.82	16.89	140.68	0.713
FEDC-PDPP	60.33	27.51	123.95	0.628
AFEDC-PDPP	56.57	14.81	107.71	0.546



Experiments and Results

- Power and performance evaluation
  - Extracted post-logic synthesis - clock tree power estimation is not available
  - Clock tree is usually 30-40% of the total dynamic power of the chip
  - In asynchronous bundled-data design, only the highest nodes of the clock tree are replaced
  - Leaf-levels drive the highest capacitance in the tree (around 80%), thus we added only 5%

SDADDER COMPARISON IN TERMS OF POWER AND PERFORMANCE.

Circuit	Throughput [MHz]	(A- / S-)	Dynamic Power [mW]	Energy/Operation [pJ]	(A- / S-)
S-Unprotected	80.00	1	0.184	2.30	1
A-Unprotected	79.59	0.995	0.179	2.24	1.027
S-TMR	80.00	1	0.683	8.54	1
A-TMR	79.51	0.994	0.683	8.59	0.994
FEDC-FDC	80.00	1	0.506	6.33	1
AFEDC-FDC	70.29	0.879	0.458	6.52	0.971
FEDC-PDPP	80.00	1	0.619	7.74	1
AFEDC-PDPP	70.00	0.875	0.539	7.71	1.004

12.5%

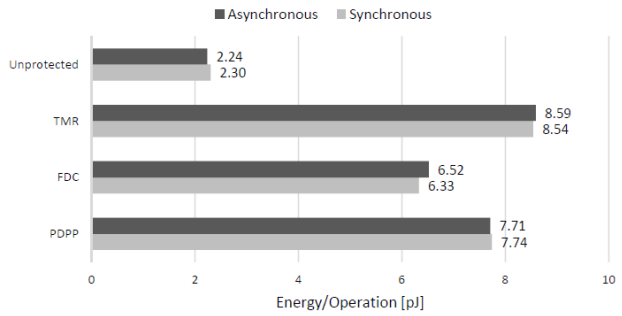
PNA-DIVIDER POWER AND PERFORMANCE COMPARISON.

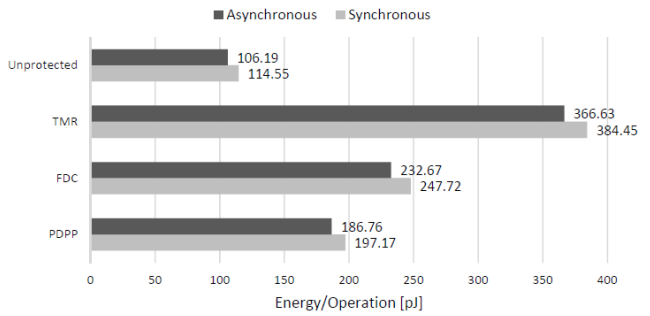
Circuit	Throughput [MHz]	(A- / S-)	Dynamic Power [mW]	Energy/Operation [pJ]	(A- / S-)
S-Unprotected	46.00	1	5.269	114.55	1
A-Unprotected	45.17	0.982	4.797	106.19	1.079
S-TMR	46.00	1	17.685	384.45	1
A-TMR	45.01	0.978	16.502	366.63	1.049
FEDC-FDC	46.00	1	11.395	247.72	1
AFEDC-FDC	41.47	0.902	9.648	232.67	1.065
FEDC-PDPP	46.00	1	9.070	197.17	1
AFEDC-PDPP	41.02	0.892	7.660	186.76	1.056

10.8%

6.5%

5.6%





Experiments and Results

- Fault simulation
  - Faults are injected in the datapath and control path

SDADDER FAULT COMPARISON.

Circuit	Injected faults	Flagged faults	Not corrected SETs	
			No. of not corrected SETs	%
S-Unprotected	631	21	21	100%
A-Unprotected	686	46	46	100%
S-TMR	1893	1593	0	0%
A-TMR	2004	1621	0	0%
FEDC-FDC	1262	48	0	0%
AFEDC-FDC	1398	127	0	0%
FEDC-PDPP	1169	47	1	2.13%
AFEDC-PDPP	1311	151	3	1.99%

PNA-DIVIDER FAULT COMPARISON.

Circuit	Injected faults	Flagged faults	Not corrected SETs	
			No. of not corrected SETs	%
S-Unprotected	14885	350	350	100%
A-Unprotected	15190	389	389	100%
S-TMR	45128	24996	0	0%
A-TMR	46088	25424	0	0%
FEDC-FDC	29917	1047	0	0%
AFEDC-FDC	30821	1140	0	0%
FEDC-PDPP	22609	766	135	17.62%
AFEDC-PDPP	23333	692	363	52.46%

Addressing SEMT in RH-Click Controllers

- Multiple transient (MT) faults resulting from a single event - due to charge sharing
  - **The simplified and unrealistic limits of SETs is no longer sufficient**
- The proposed approach aims to reduce the probability of MT faults affecting the controller's behavior
  - Gates close to each other have a higher probability to be affected by the same particle strike
- Post placement strategy for the RH-Click controller
  - Strategy aimed to minimize performance/area/timing overheads
  - R-Abax – Legalisation algorithm is an alternative
    - Automatically satisfy the spacing constraints among the specified groups of gates

F. A. Kuentzer, C. Georgakidis, C. P. Sotiriou, and M. Krstic, "Addressing Single-Event-Multiple-Transient Faults in Asynchronous RH-Click Controllers", SBCCI, Sept. 2023, pp. 1–6.

Proposed Approach

Grouping strategy

1. **Grouping gates based on the controller's state transitions**

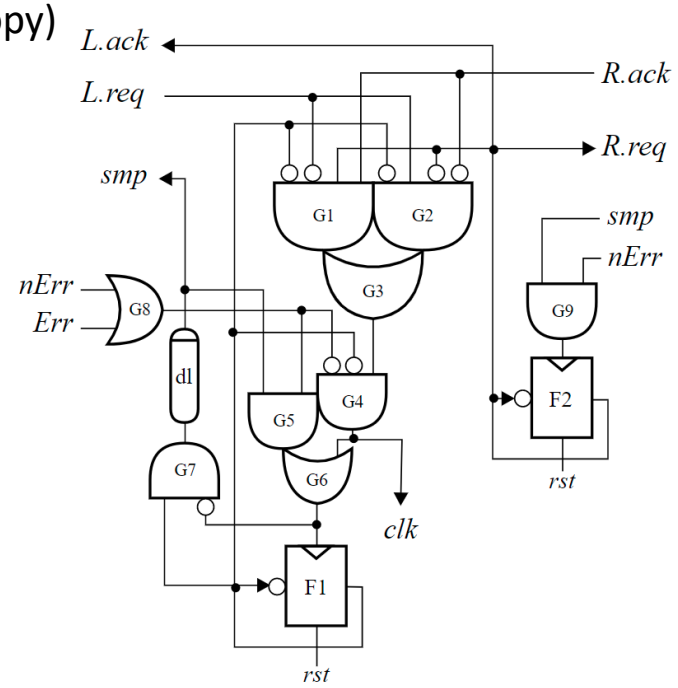
   Allow gates within a group to be placed close to each other to minimize the area overhead

   Space equivalent groups spaced from each other (RH-Click combinational logic copy)

2. **Tracing critical gates based on MT fault simulations**

   Identify special cases where the previous step cannot address

   The controller timing behavior is taken into account

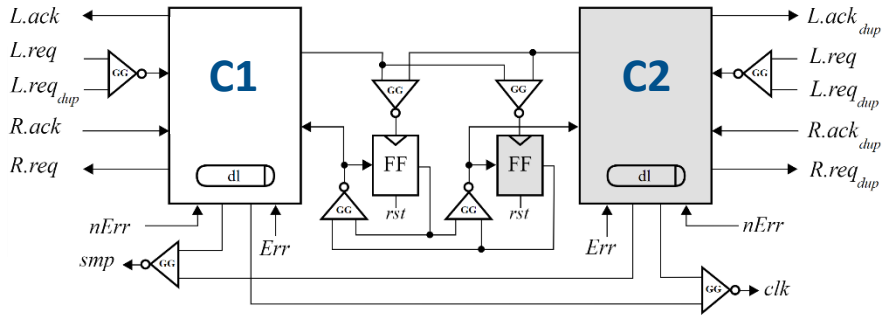


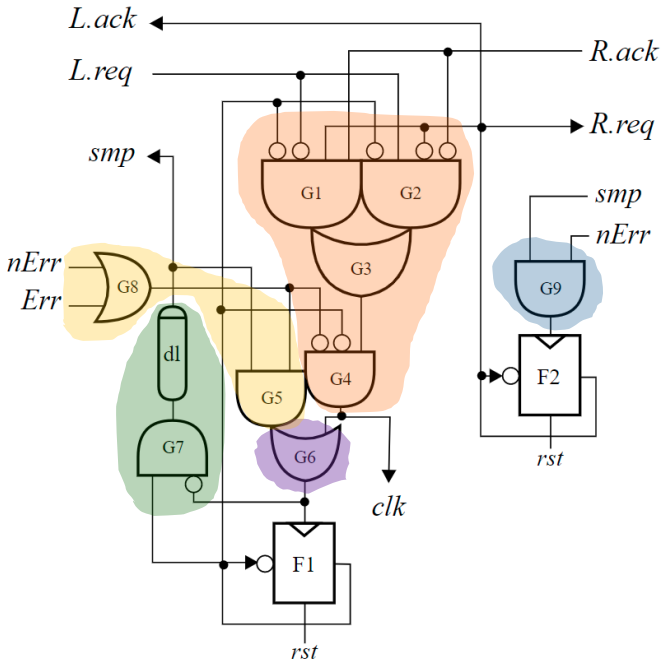
F. A. Kuentzer, C. Georgakidis, C. P. Sotiriou, and M. Krstic, "Addressing Single-Event-Multiple-Transient Faults in Asynchronous RH-Click Controllers", SBCCI, Sept. 2023, pp. 1–6.

Asynchronous Full Error Detection and Correction - AFEDC

1. Grouping gates based on state transition
   - State transition of flip-flops **(F1,F2)**
   - **{G1,G2,G3,G4,G6}** control **(0,0) → (1,0)**
   - **{G5,G6,G8}** control **(1,0) → (0,0)**
   - **{G6}** intersect both groups

- Equivalent groups in **C1** and **C2** should not be affected by TFs simultaneously
  - Assuming the spaced groups, faults are only present in valid gate combinations
  - Ex. of valid combination (considering 2 MT)
    - **G1** in **C1** and **G5** in **C2**
    - **G5** in **C1** with **G6** in **C1**
  - Ex. of invalid combination
    - **G1** in **C1** and **G2** in **C2**
    - **G6** in **C1** and **G6** in **C2**



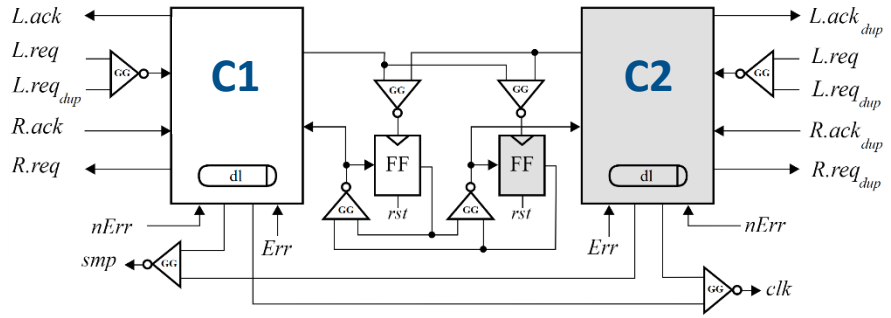


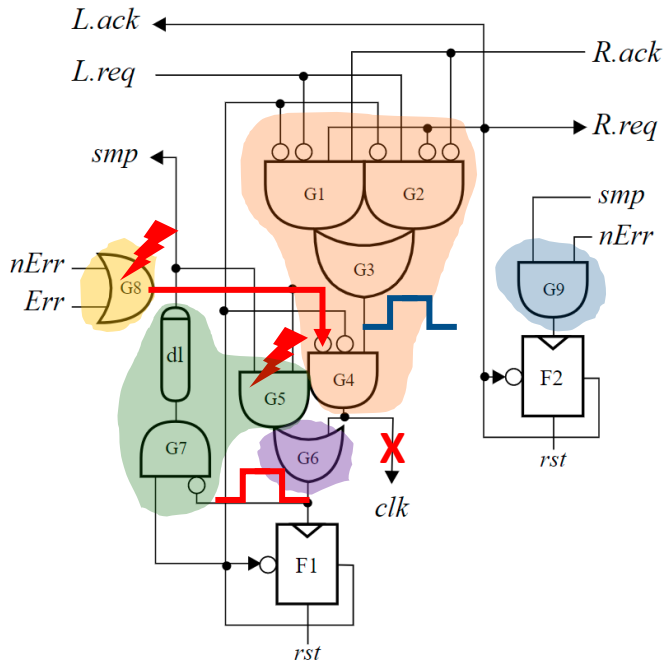
Why not simply space C1 from C2?

Asynchronous Full Error Detection and Correction - AFEDC

- MTs within the same combinational copy
  - **G5** and **G8** in **C1** generate a transient and **G3** is propagation a valid transition in **C1** and **C2**
  - **G8** mask the path from **G3** and **G5** transient propagates through **G6** in **C1**
  - **C2** propagates a valid transition through from **G3** to **G6**
  - The ***clk*** is not generated in **C1** (GG voted) but **F1** is triggered anyway
    - Invalid state transition
    - **G5** in **C1** and **G8** in **C1** is a critical combination

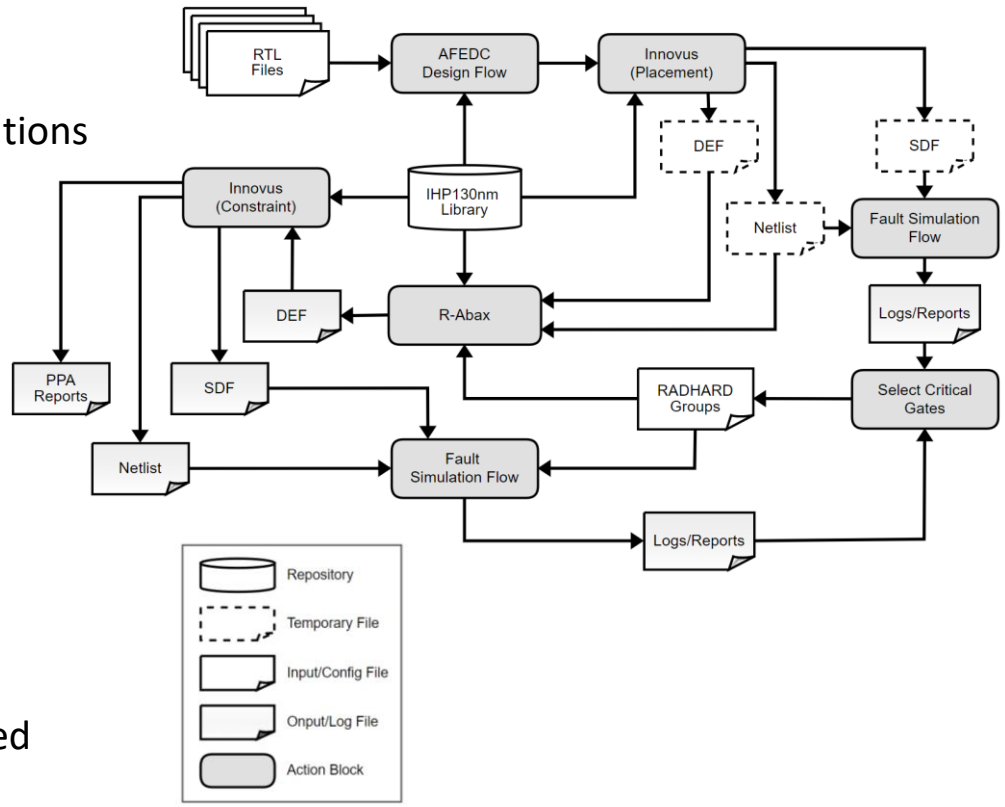
2. Tracing critical gates
   - Multiple transient fault simulations
     - Randomly injected in all possible gate combinations
       - No restrictions
     - Critical gate combinations automatically reported
       - Gates most involved in faulty simulations
   - **G6** and **G8** are the critical gates
     - Spacing them only from their copies is not enough
     - **G6** and **G8** became separate “groups”
       - Must be spaced from all other gates including both combinational copies





Proposed Approach Evaluation

- AFEDC Design Flow
  - Design Compiler from Synopsys for logic synthesis
  - Innovus from Cadence for P&R
  - Cadence Incisive Functional Safety Simulator (IFSS) for the fault simulations
    - Part of Xcelium
- 5-stage 32-bit array multiplayer
  - One RH-Click controller for each stage
  - IHP 130nm technology process
- The fault simulations target only the controller in the center stage
  - 2 MT and 3 MT faults simulations
  - Gate combinations are marked as forbidden and automatically removed
    - Reflects the spacing strategy



SEMT Fault Experiments

- Three separate experiments
  - **T1** is the baseline where no spacing is assumed
    - All gate combinations are allowed
  - **T2** includes only the first grouping step
  - **T3** combines both grouping steps
  - MTs duration follow a log-normal distribution ranging from 100ps to 2000ps

MT	Experiment	Simulations	Errors	%
2	T1	1891	29	1.53%
	T2	1376	3	0.22%
	T3	1032	0	0.00%
3	T1	37820	1726	4.56%
	T2	15388	135	0.88%
	T3	8644	0	0.00%

Layout Impact

- The minimum spacing between cells depends on the area affected by the particle strike
  - Not deterministic and depends on several parameters
    - Particle diameter, strike angle, energy deposited in silicon
  - 5 µm and 10 µm are suggested in the literature and evaluated along with 7 µm as an intermediate
- The spacings were applied in all five RH-Click controllers
- Power, Performance, and Area (PPA) parameters are extracted with Cadence Innovus

Spacing [µm]	Area [µm^2]	Density [%]	Throughput [MHz]	Total power [mW]		Wire length [µm]		Average wire length/net [µm]	
0	73.01	59.94	80.96	8.4028	1.00000	96677.245	1.0000	19.121	1.0000
5	73.01	59.94	80.96	8.4416	1.00463	103416.240	1.0697	20.454	1.0697
7	73.01	59.94	80.96	8.4418	1.00464	104013.385	1.0759	20.572	1.0759
10	73.01	59.94	80.96	8.4412	1.00458	104958.110	1.0857	20.759	1.0857

Conclusions and Future Works

- Asynchronous Full Error Detection and Correction - AFEDC
  - Latch-based asynchronous bundle-data design
  - Covers soft errors in combinational and sequential logic
    - Datapath and Control path
  - Error handled locally
  - Tolerance to unbounded SET durations
  - Addresses the metastability problem
  - Future Works
    - Explore different detection mechanisms
    - More complex test cases
    - Chip TO

- SEMT in RH-Click Controllers
  - Post-placement spacing approach
  - Grouping strategies to minimize PPA and detect critical gates
  - Effective to prevent MTs from affecting the RH-Click behavior
  - Future Works
    - Demonstrate the proposed solution is generic

Thank you for your attention!

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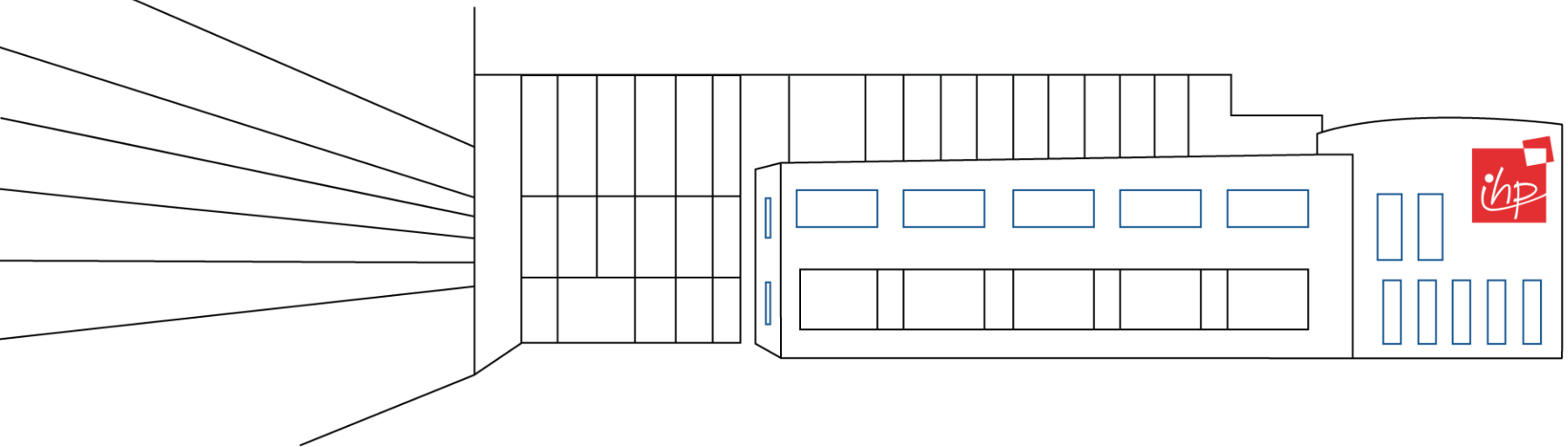

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