Experimental Analysis of Single Event Transients in Digital Circuits

Marko Andjelkovic

IHP – Institute for High Performance Microelectronics, Frankfurt (Oder), Germany

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Outline

1. **Introduction**
2. **Fundamentals of Single Event Transients**
3. **Design of a SET pulse width measurement system**
4. **Conclusion**

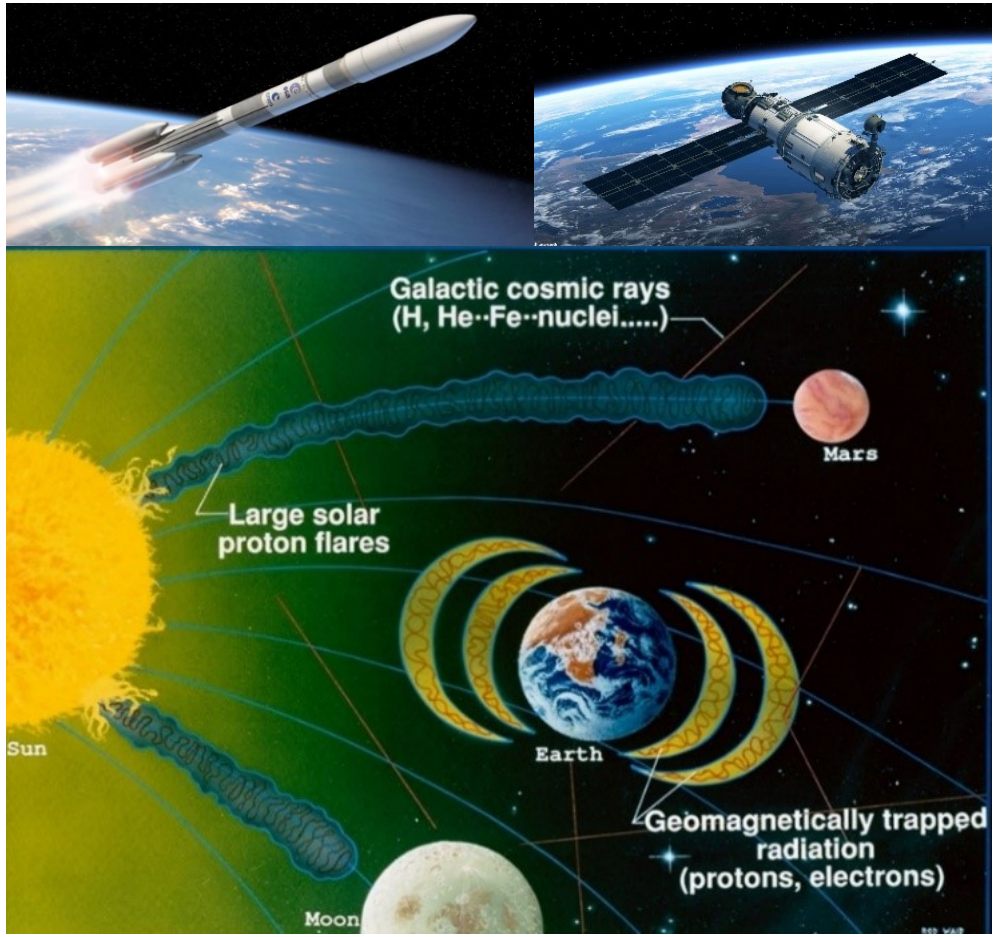
1. Introduction

Ionizing radiation in space

- Different types of radiation (gamma, x-rays, energetic particles)
- Cause malfunction or physical damage in electronics in space and at ground

Radiation sources in space

- Solar Particle Events due to explosions on the Sun
- Radiation trapped in Earth's magnetic field (Van Allen belts)
- Galactic Cosmic Rays from deep space



1. Introduction

Classification of radiation-induced effects

Cumulative Effects

- Total Ionizing Dose (TID)
- Displacement damage
- Enhanced low-dose-rate sensitivity (ELDRS)

Single Event Effects

Soft errors:
- Single Event Transient (SET)
- Single Event Upset (SEU)
- Single Event Functional Interrupt (SEFI)

Hard errors:
- Single Event Latchup (SEL)
- Single Event Gate Rupture (SEGR)
- Single Event Burnout (SEBR)

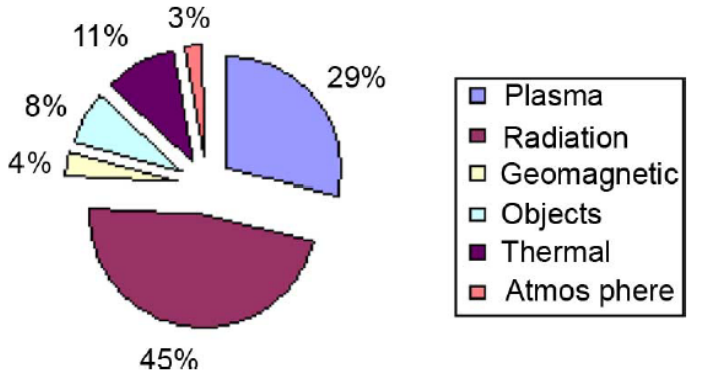
1. Introduction

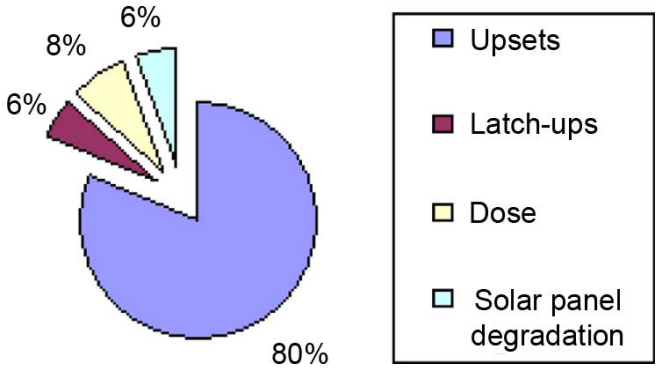
Soft errors

- Manifested as bit-flips, resulting in data loss and system malfunction
- Caused by energetic particles such as heavy ions, neutrons, protons
- Major cause of faults in ICs used in space missions

Over 40 % of all anomalies in space missions caused by environmental factors have been due to ionizing radiation

Over 80 % of radiation-induced anomalies in space missions have been caused by soft errors



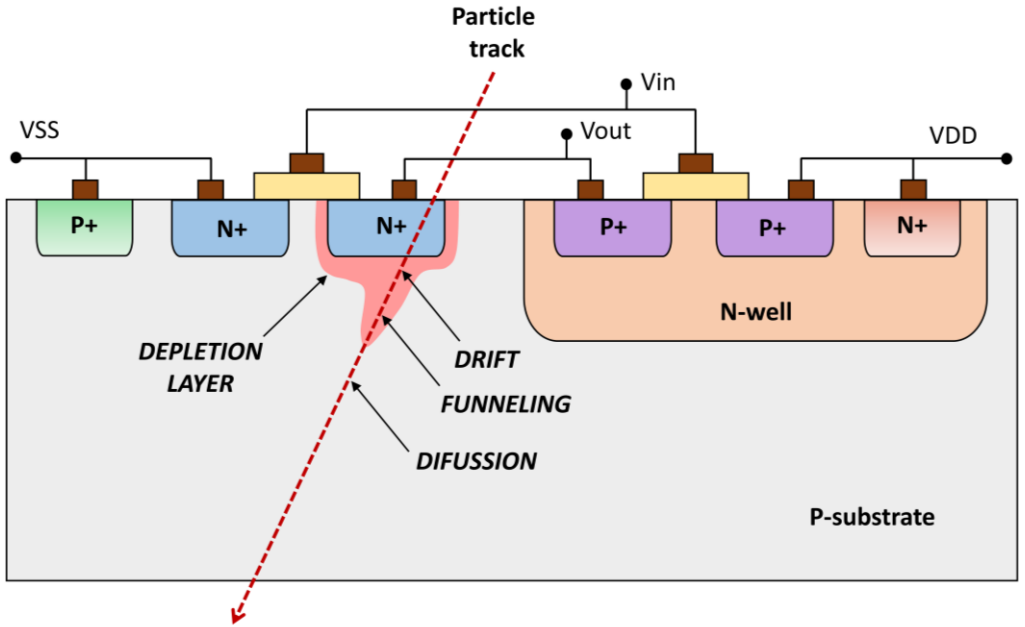


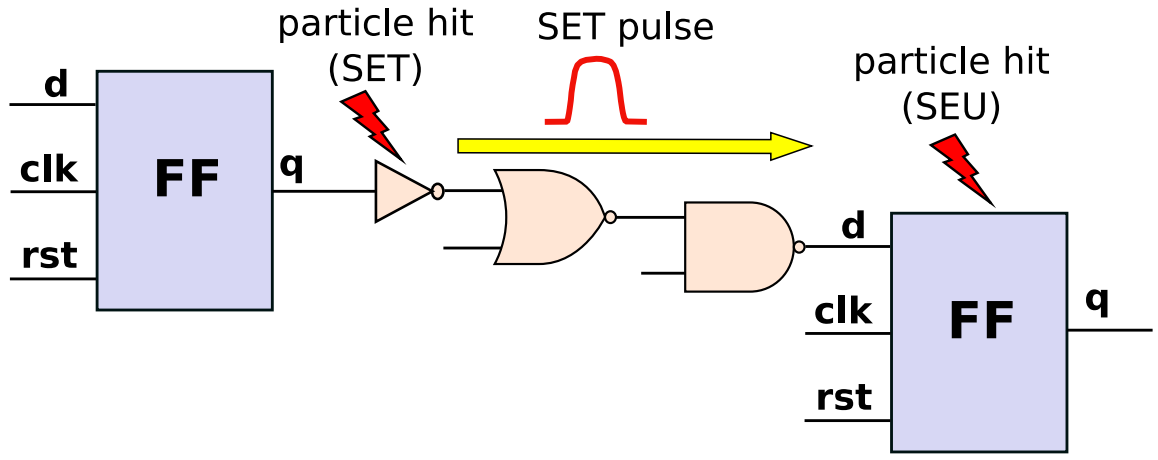
Source: **R. Ecoffet, Overview of In-Orbit Radiation Induced Spacecraft Anomalies, IEEE Transactions on Nuclear Science, 2013.**

1. Introduction

How soft errors occur?

- Particle hits a storage element, resulting in a bit-flip (**Single Event Upset - SEU**)
- Particle hits a combinational element, resulting in a voltage glitch (**Single Event Transient - SET**), which may propagate to one or more storage elements and cause one or more bit-flips



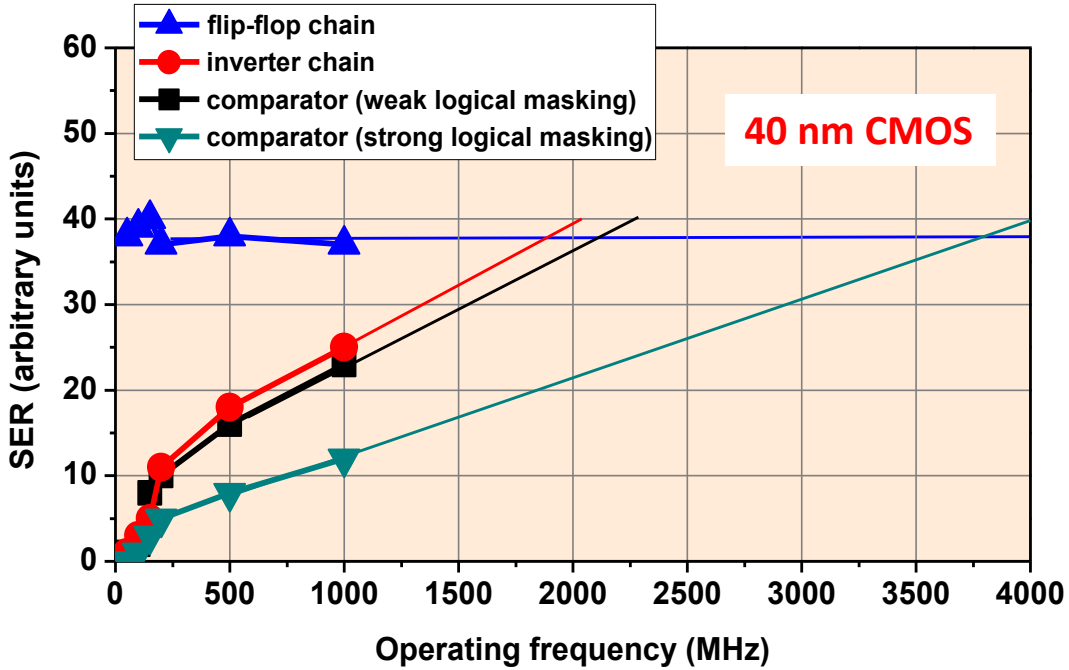


1. Introduction

Contribution of SETs to the total SER of an IC increases with technology scaling

- As operating frequency increases, SET latching probability increases
- As supply voltage decreases, SET generation probability increases
- As logic path length decreases, logical and electrical masking probabilities decrease

SETs may be particularly critical at GHz clock frequencies



Source: **N. Mahatme et al., "Comparison of Combinational and Sequential Error Rates for a Deep Submicron Process," IEEE TNS, 2011.**

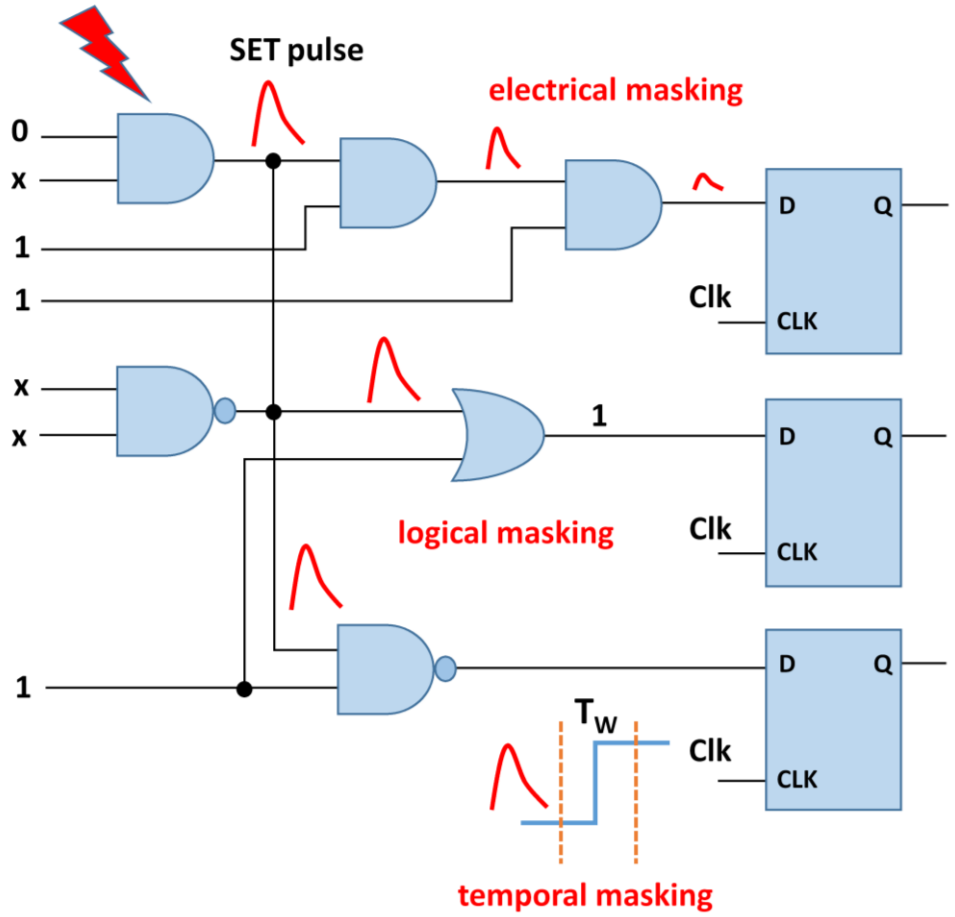
2. Fundamentals of Single Event Transients

SET generation

- If a particle deposits more charge than the critical charge of a circuit node, a SET pulse will be formed
- Generated SET pulse width depends on particle energy (LET) and design/operating/technology parameters

SET propagation

- SETs longer than propagation delay of logic gates may propagate through the circuit
- SETs may be masked by 3 masking effects: electrical, logical and temporal masking
- SET pulse width may increase during propagation due to Propagation-induced Pulse Broadening (PIPB)



2. Fundamentals of Single Event Transients

Combinational Soft Error Rate (SER) is the total number of soft errors due to SETs in a given time period

$$SER = \sum_{i=1}^{N} SER_{NOMINAL}(i) \times SER_{DERATING}(i)$$

$$SER_{NOMINAL} = k \cdot Flux \cdot Area \cdot e^{-Q_{CRIT}/Q_S}$$

$$SER_{DERATING} = Logical_{DER} \times Electrical_{DER} \times Timing_{DER}$$

SET pulse width determines *Electrical* and *Timing* masking factors

2. Fundamentals of Single Event Transients

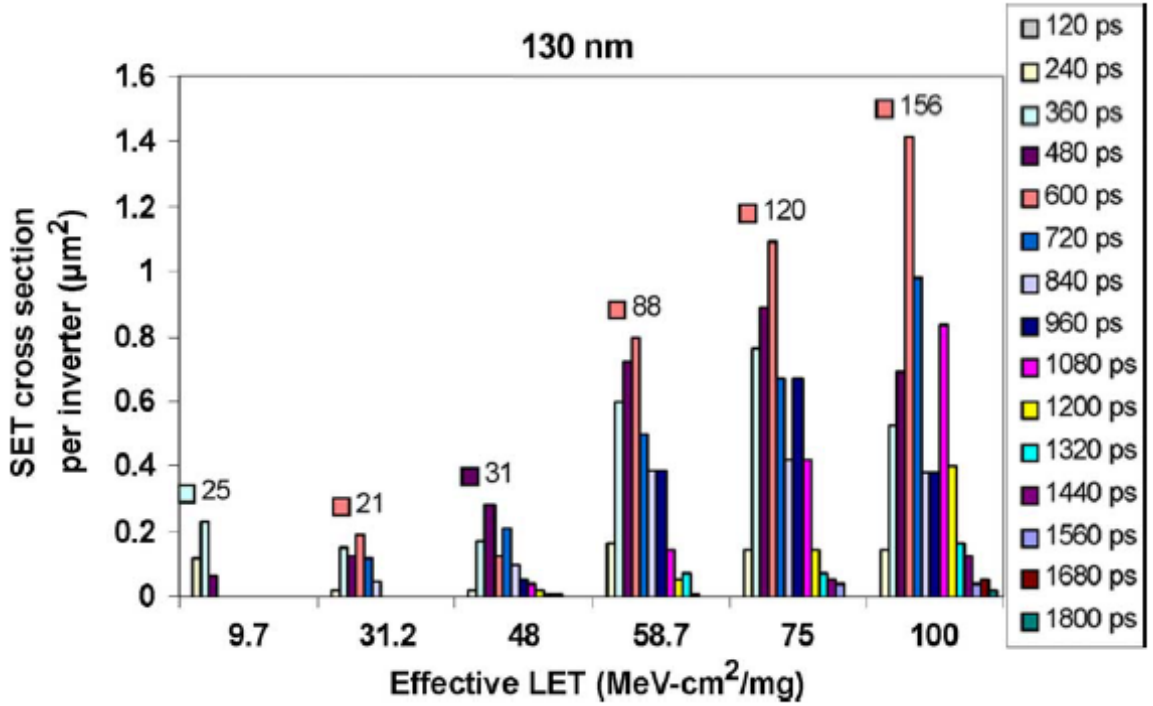
- **Generated SET pulse width dependence on different parameters**

Parameters	Impact on generated SET pulse width
Technology scales	Generally decreases
LET increases	Increases
Gate size increases	Decreases
Load capacitance increases	Increases up to certain load, and then decreases for large loads
Supply voltage increases	Decreases
Temperature increases	Increases (reverse effect for FinFET)

2. Fundamentals of Single Event Transients

Experimental SET pulse width analysis

- **Performed by irradiating a test circuit with high energy particles (e.g., heavy ions)**
- **Characterization of SET sensitivity of individual standard cells**
- **Key information obtained from experiments**
  - Threshold LET
  - SET pulse width distribution



B. Narasimhan et al., IEEE TNS, 2007.

2. Fundamentals of Single Event Transients

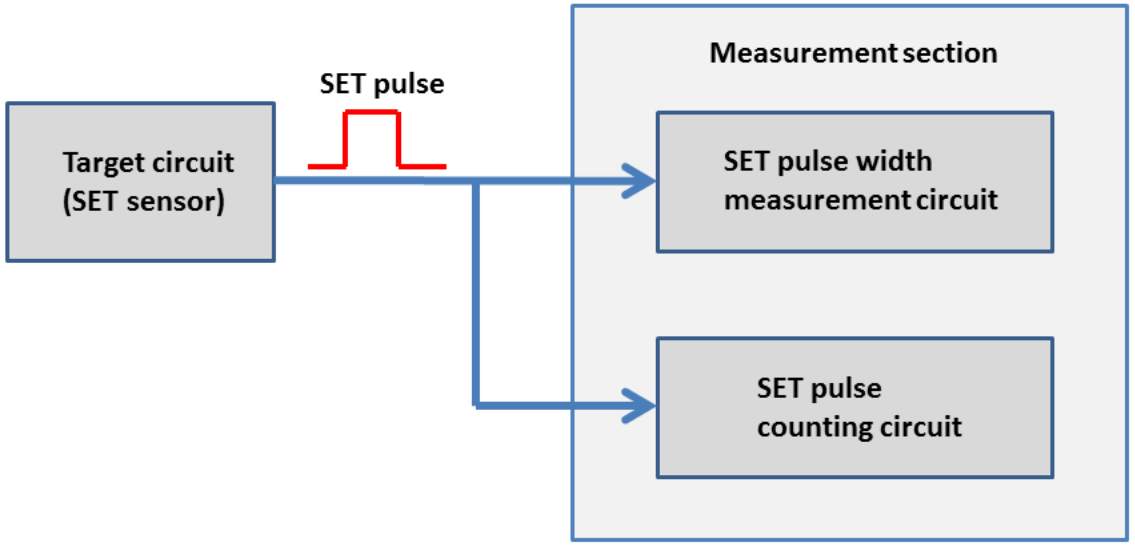
- **Impact of technology scaling on SET pulse width (published experimental results)**

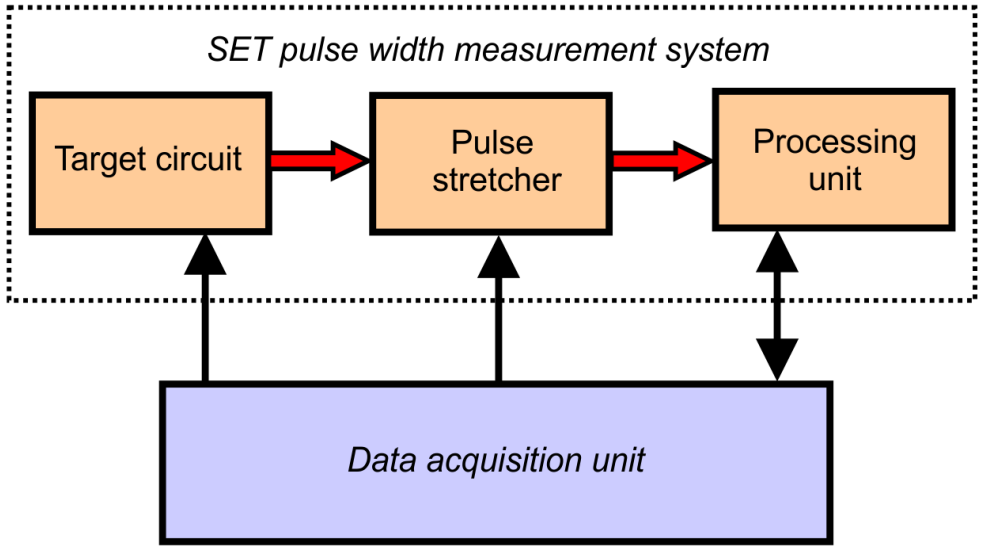
Technology node	Reference	Maximum SET width at LET = 60 MeVcm^{2}mg^{-1}	Average SET width at LET = 60 MeVcm^{2}mg^{-1}
250 nm	Benedetto et al.	1.5 ns	n/a
180 nm	Benedetto et al.	1.5 ns	n/a
130 nm	Benedetto et al.	2.7 ns	n/a
	Narasimhan et al.	1.4 ns	650 ps
90 nm	Narasimhan et al.	1.4 ns	750 ps
65 nm	Gadlage et al.	200 ps	120 ps
	Jagannathan et al.	250 ps	175 ps
28 nm	Jagannathan et al.	230 ps	165 ps

3. Design of SET Pulse Width Measurement System

General design of a SET pulse width measurement system

- Counting generated SETs
- Measuring SET pulse width

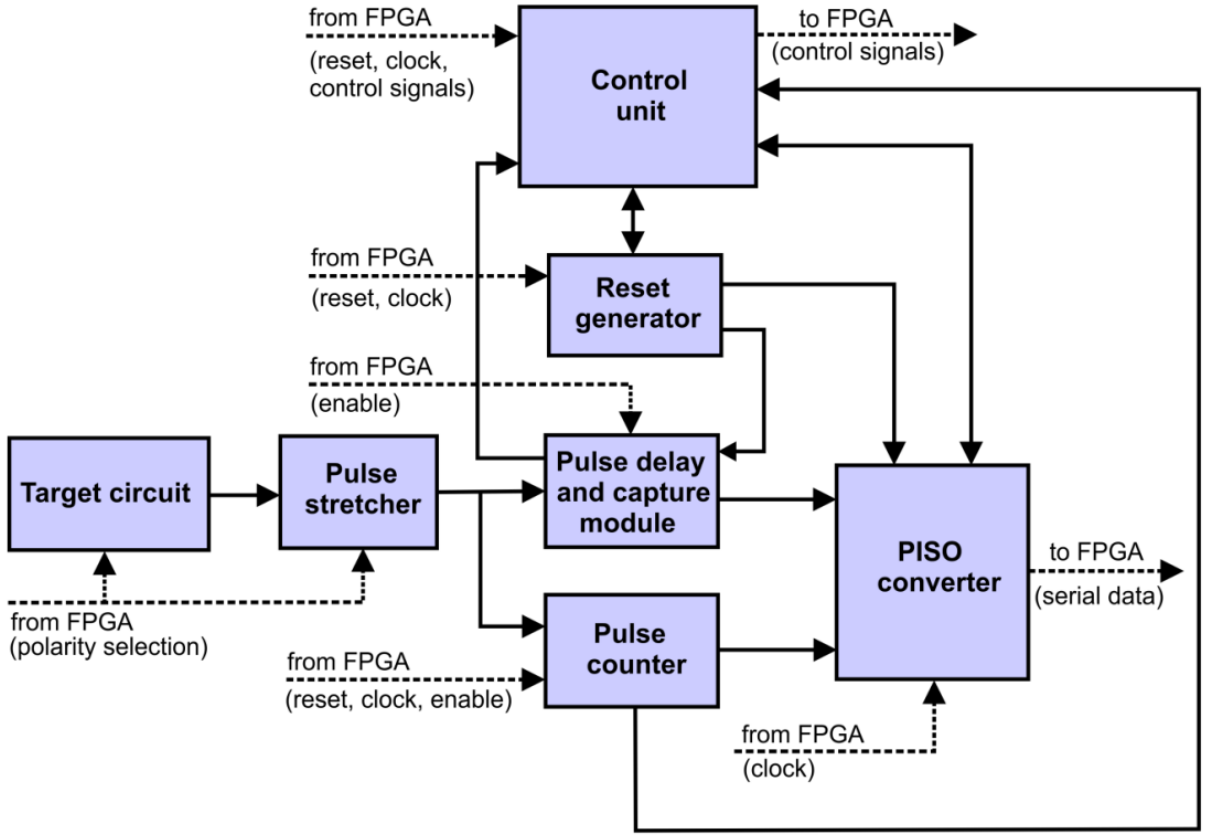




3. Design of SET Pulse Width Measurement System

Architecture of SET pulse width measurement system

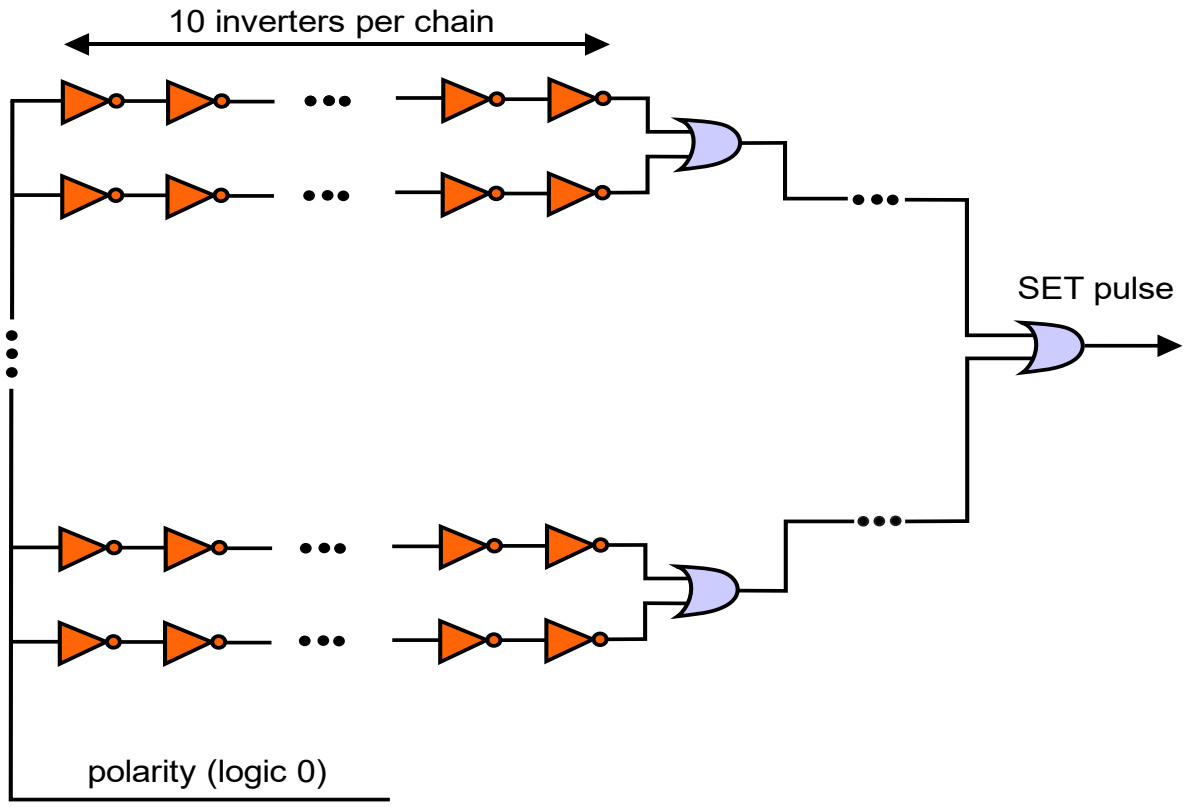
- Technology-independent design
- Simple architecture – no synchronization circuitry
- Target circuit should be larger that the rest of the system
- Pulse stretcher extends the SET pulse width to enable its propagation
- All FFs are TMR



3. Design of SET Pulse Width Measurement System

Target circuit for SET pulse width measurement

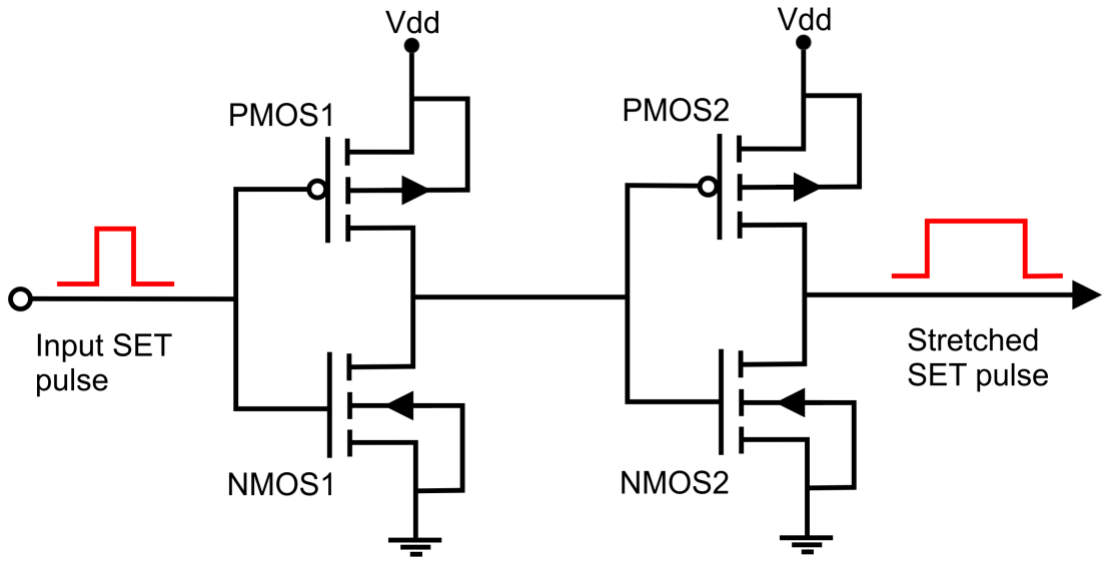
- Based on inverters, but any other standard cell could be used
- Inverters with minimum driving strength have been used
- Inverter chains should be short enough to allow SET propagation
- External signal defines the polarity of detectable SETs.



3. Design of SET Pulse Width Measurement System

Pulse stretcher

- Pulse stretching based on 2 asymmetrically-sized inverters
- Increases pulse width by several hundred ps



Transistor sizing criteria:

$W_{NMOS1} > W_{PMOS1}$

$W_{PMOS2} > W_{NMOS2}$

$W_{NMOS1} = W_{PMOS2}$

$W_{PMOS1} = W_{NMOS2}$

Output pulse width:

$T_{OUT} = T_{IN} + \Delta T$

Pulse stretching:

$\Delta T = k \cdot S$

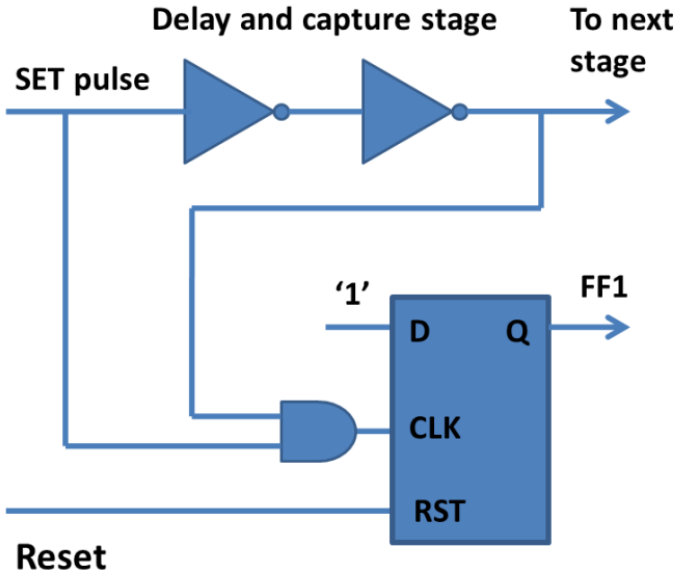
Sizing factor of pulse stretcher:

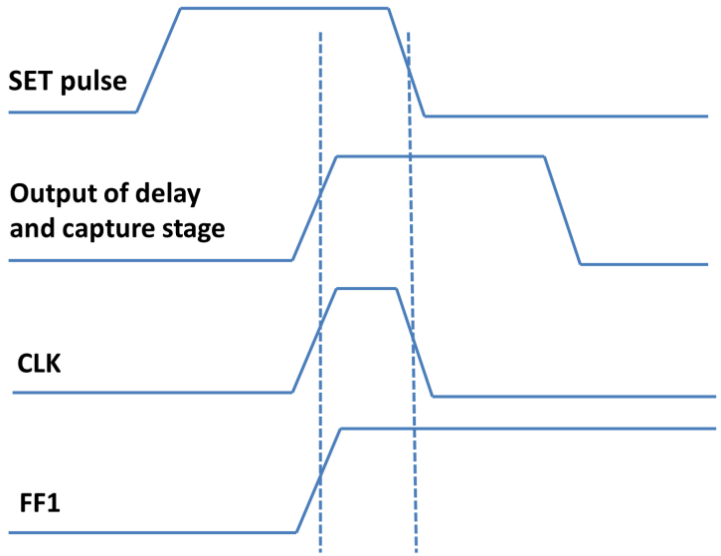
$S = W_{NMOS1}/W_{PMOS1} = W_{PMOS2}/W_{NMOS2}$

3. Design of SET Pulse Width Measurement System

Delay-and-capture unit

- Measures SET pulse width employing the principle of time-to-digital conversion
- Composed of a delay line (2 inverters) and a capturing FF

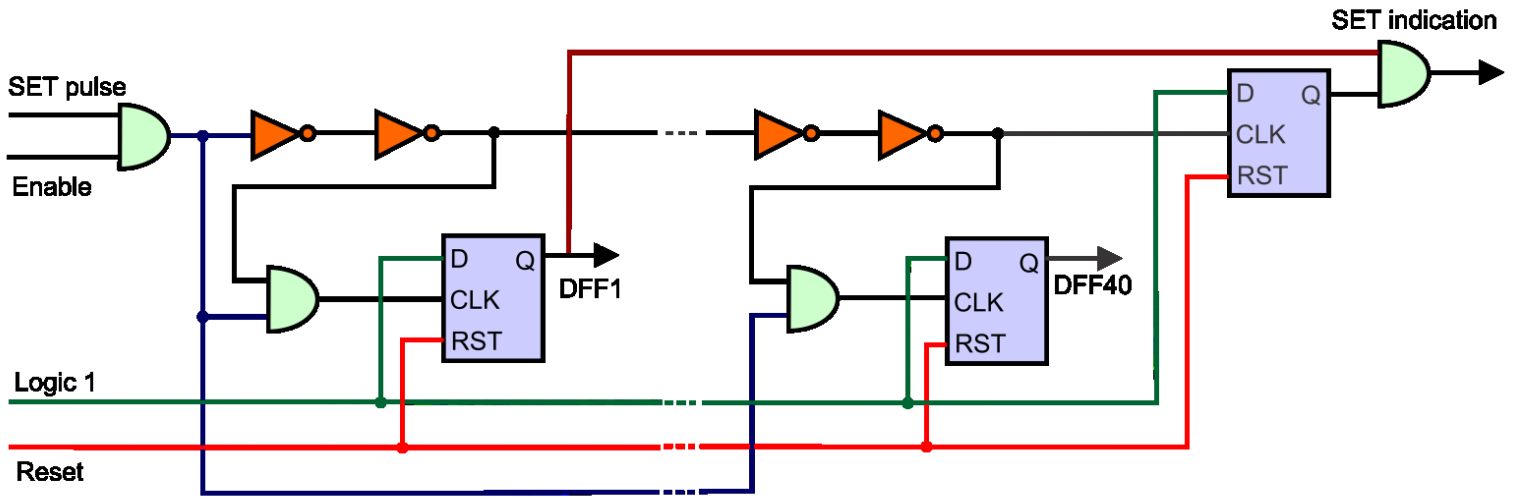




3. Design of SET Pulse Width Measurement System

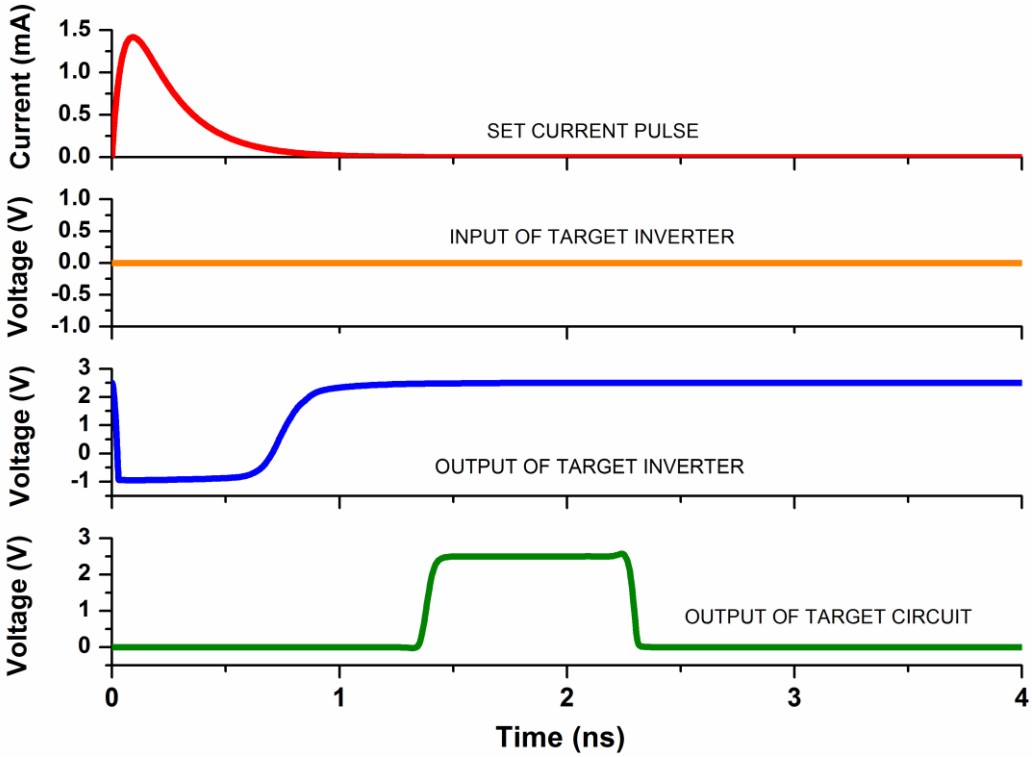
Delay-and-capture circuit

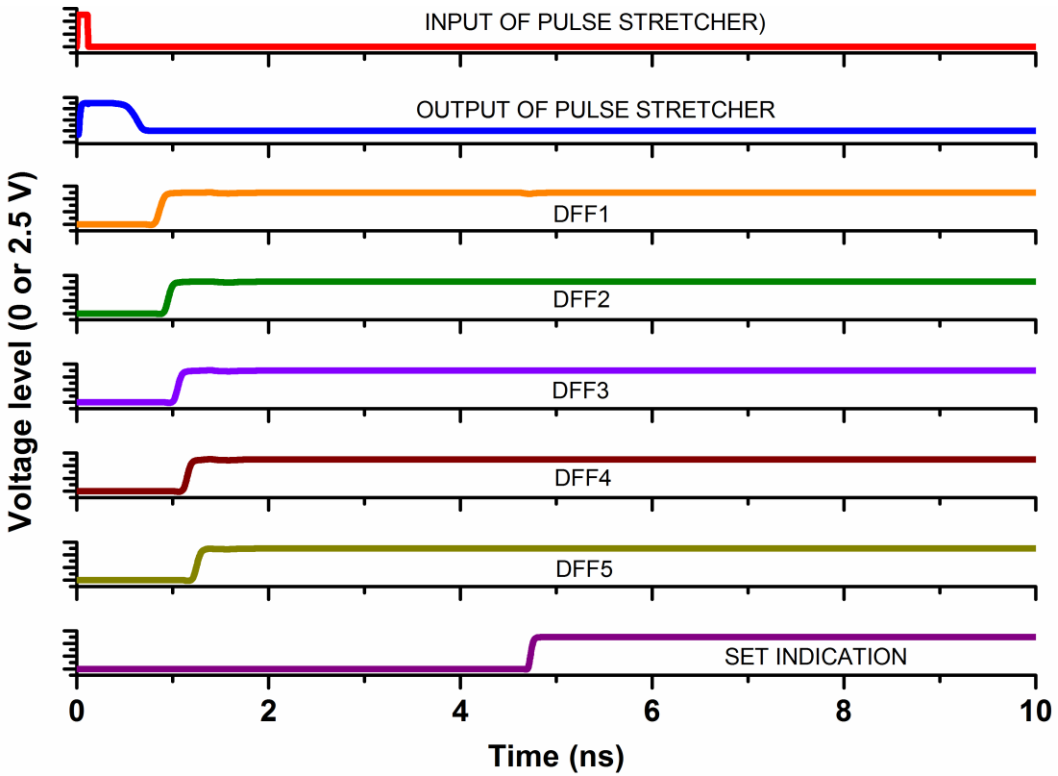
- N delay-and-capture units – N-bit sequence is equivalent to the pulse width
- Generated bit stream has the form 11..0, where number of 1s determines the pulse width
- Measurement resolution is equivalent to the delay of 2-inverter delay line



3. Design of SET Pulse Width Measurement System

Simulation results

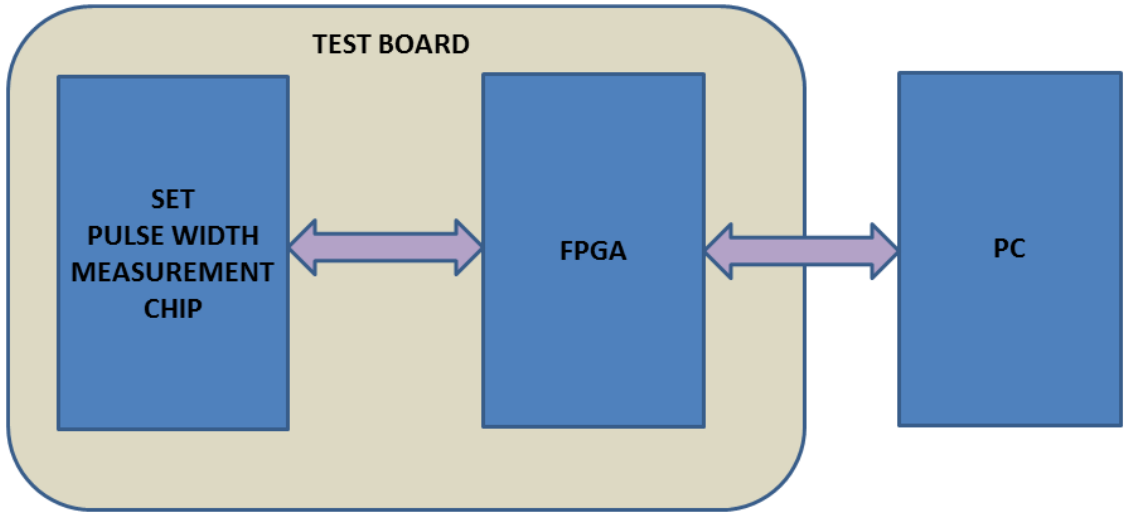


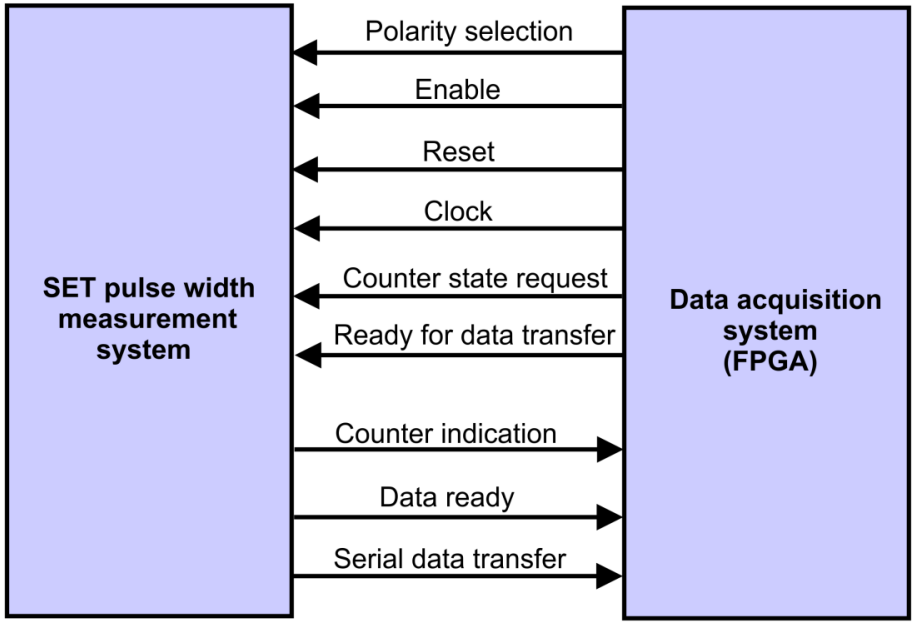


3. Design of SET Pulse Width Measurement System

Interfacing with FPGA

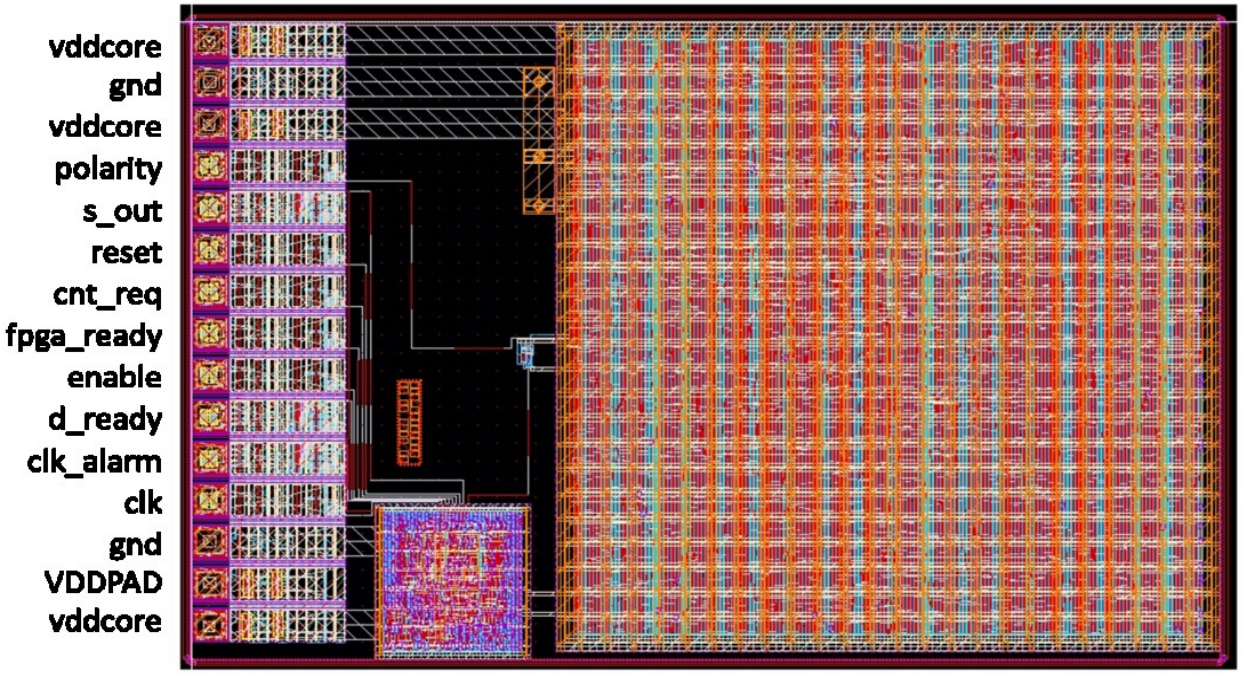
- FPGA transfers the acquired data to the PC
- FPGA generates control signals (enable, clock, reset)





3. Design of SET Pulse Width Measurement System

Implementation details



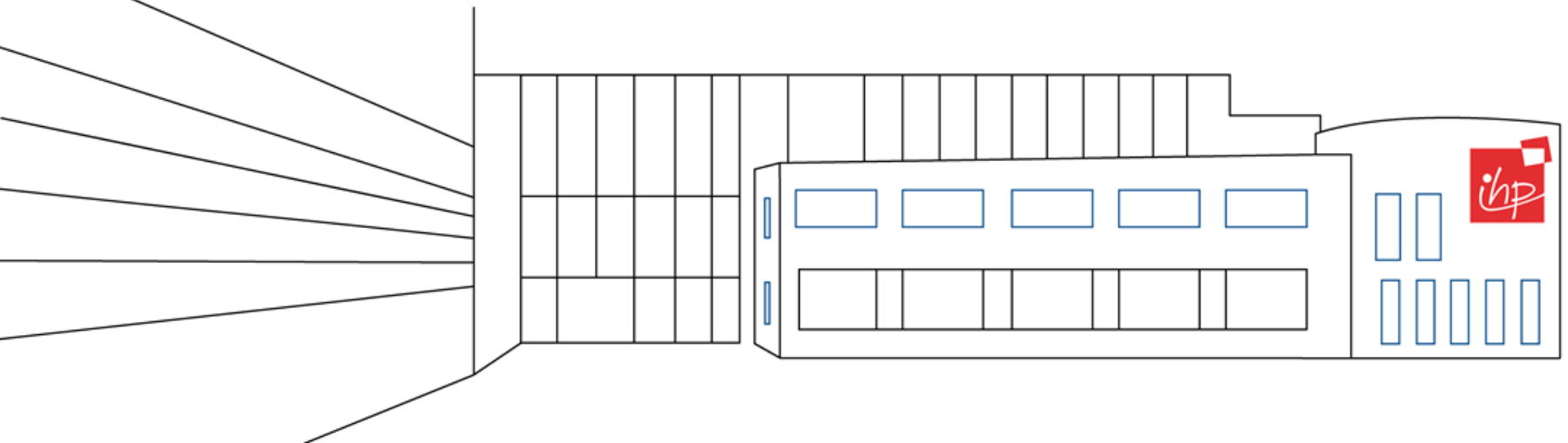
Parameter	Value
Technology	IHP 250 nm
Clock frequency	50 MHz
Core V_{DD}	2.5 V
I/O V_{DD}	3.3 V
No. of inverters in target circuit	80 000
Area of target circuit	2 mm^2
Area of processing unit	0.1 mm^2
Die size	3.6 mm^2

4. Conclusion

- **SET effects should be considered in rad-hard design**
- **Experimental characterization of SET pulse width is important for developing accurate SET models for simulation tools**
- **Experimental characterization can provide information on the sensitivity of individual standard cells and the impact of LET, temperature and supply voltage**

Thank you for your attention!

IHP GmbH – Innovations for High Performance Microelectronics
Im Technologiepark 25
15236 Frankfurt (Oder)
Tel.: +49 (0) 335 5625 527
E-Mail: andjelkovic@ihp-microelectronics.com



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