# Combined Effects of Ionizing Radiation and Electromagnetic Interference on Electronic Circuits & Systems

Fabian Vargas

10 Jan 2025

Leibniz Institute
for High
Performance
Microelectronics

# Agenda

1. IHP at a Glance
2. Importance of Testing & Qualification of ICs for Ionizing and Non-Ionizing Radiations
3. Mechanisms by which  Ionizing Radiation Affects Electronics and How they Impact IC Lifetime
4. The Need of Combined Tests for Ionizing and Non-Ionizing Radiations
5. TID & SEU Measurement Techniques at the IC Level
6. Mitigation Approaches
7. Case-Study on Combined Test

# IHP at a Glance

# IHP at a Glance

Positioning

- IHP is the **European research and innovation centre** for **silicon-based systems**, ultrahigh-frequency circuits and technologies
- The research focuses on **socially relevant topics** such as communication, mobility, health & environment, industry & agriculture, sustainability and security.
- With its research programmes, the IHP makes **an important contribution to the technological sovereignty** of Germany and Europe

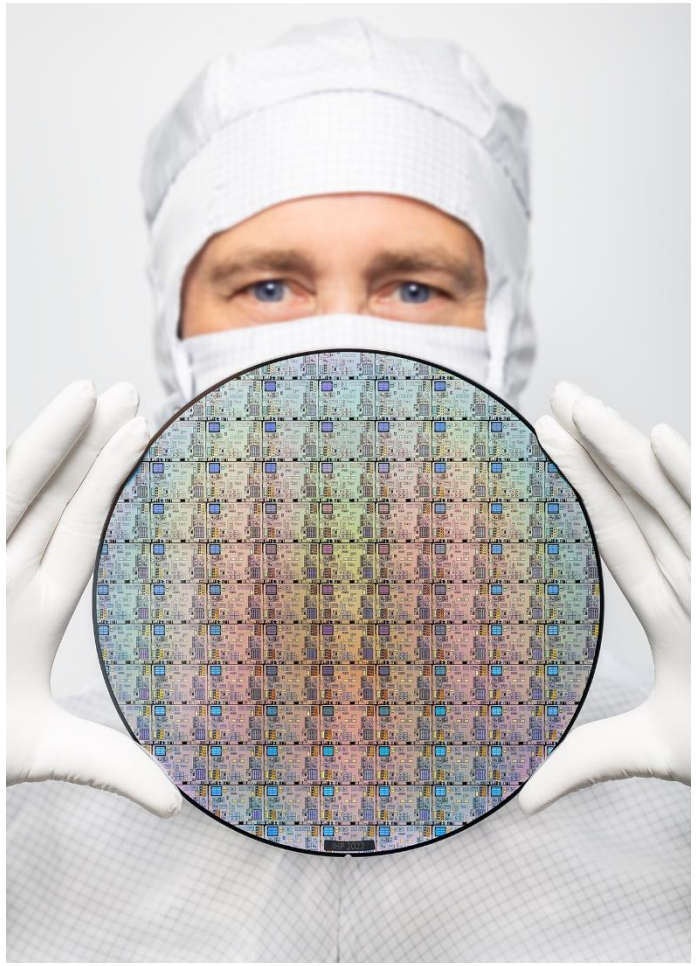
*Vision*

*"We create foundations and prototype applications based on future silicon-based technologies and systems for a digitalised and networked world as well as for the sustainable preservation of our natural living conditions."*

# IHP at a Glance

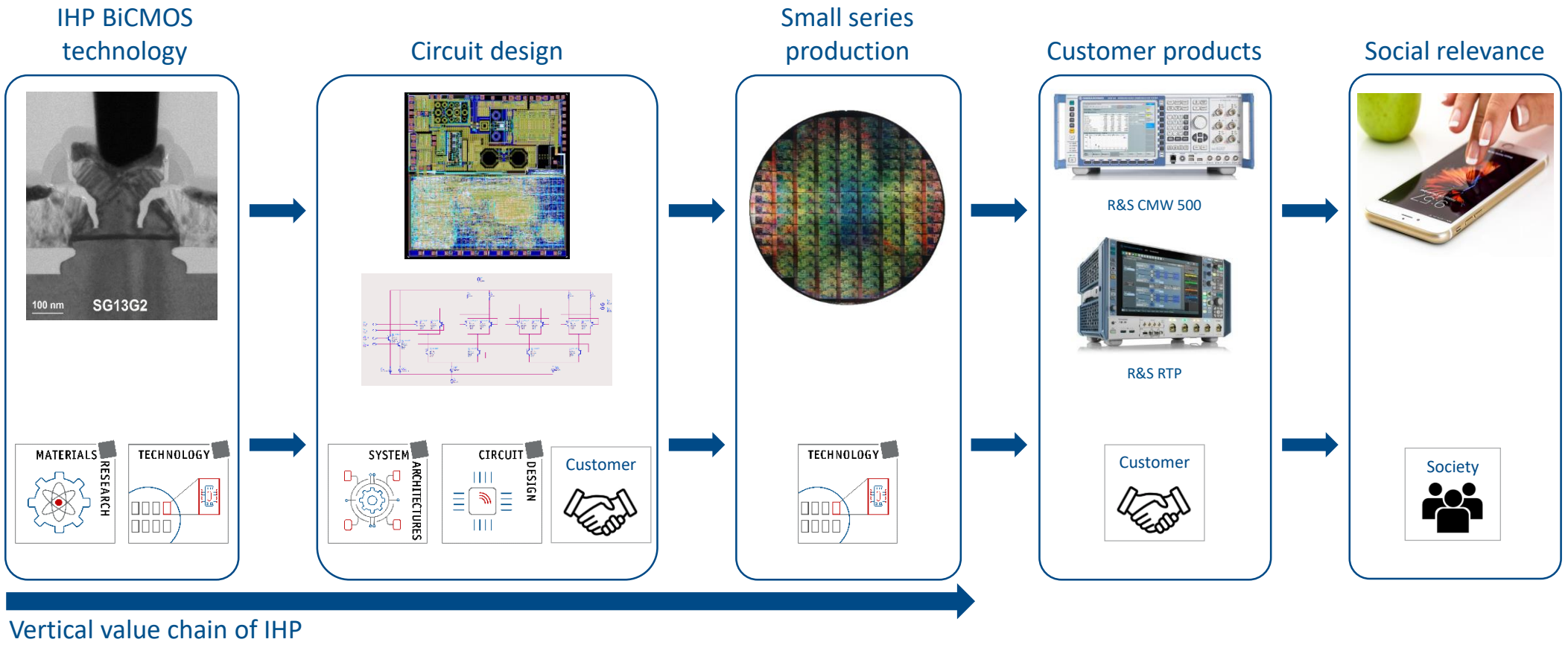
Profile and Strengths

- **Vertical research** concept from materials research and technology to circuits and systems
- **International leadership and visibility** in all of its research areas
- **Unique selling point** of a **200mm pilot line** for state-of-the-art BiCMOS technologies, operated under **industry-like conditions, 24/7**, for the provision of prototypes and low-volume production runs.
- **Qualified technological platform** with direct access for science and industry

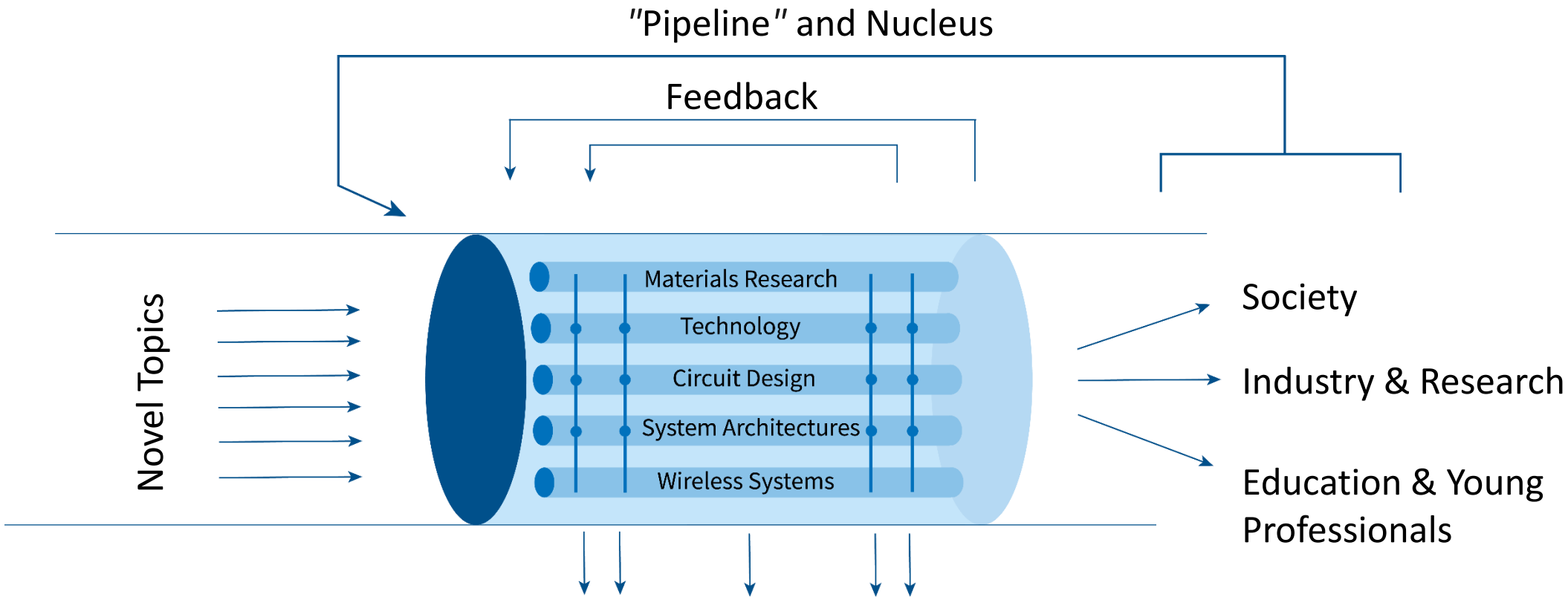


# Example of Vertical Value Chain

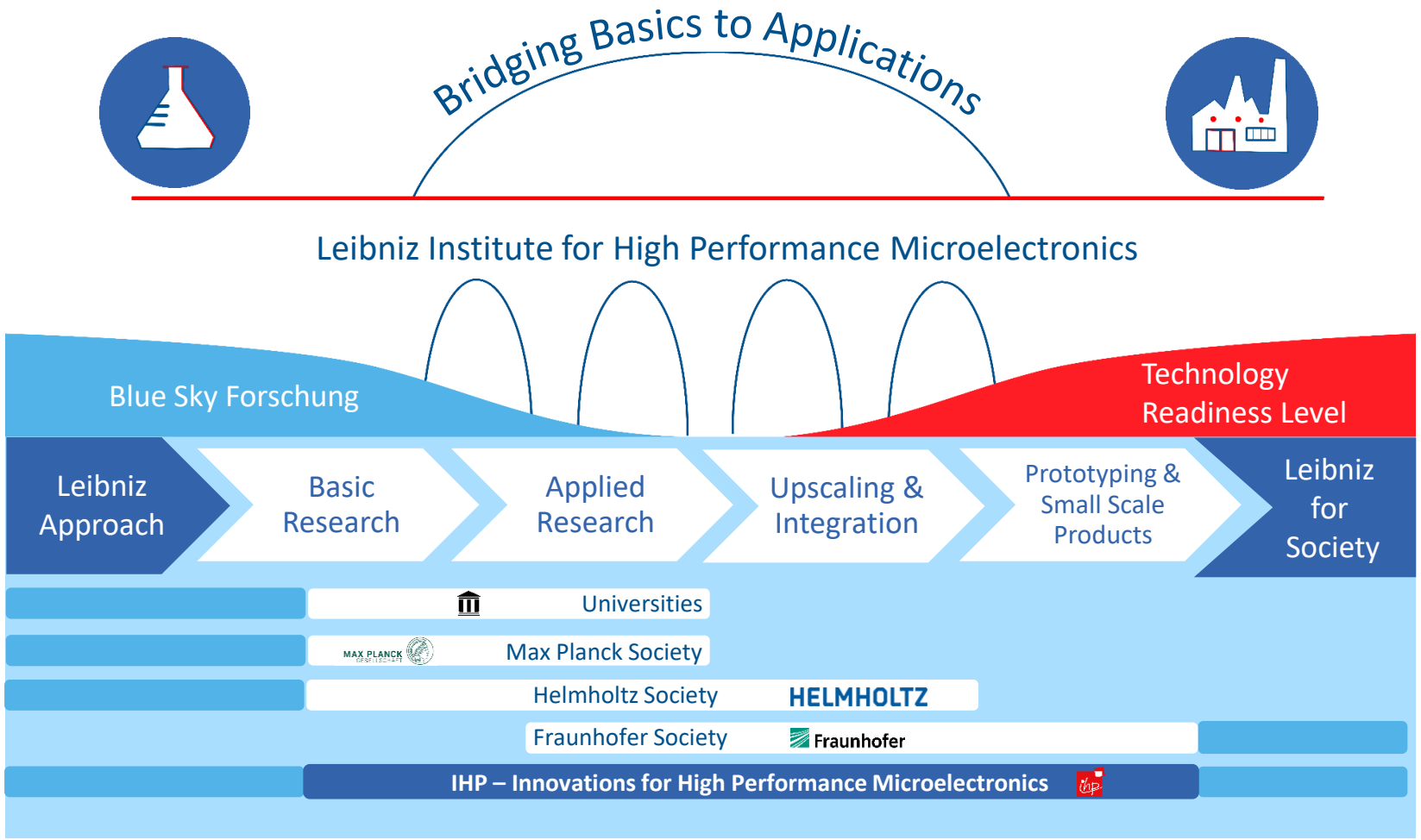
Use of the qualified IHP BiCMOS technology



# Holistic Research Approach



# Strategic Positioning



# Importance of Testing & Qualification of ICs for Ionizing and Non-Ionizing Radiations

# Introduction – Why Rad Test is Important

*Timeline*

- **1954 - 57**: Single-event upsets (SEUs) were 1st described (**above-ground nuclear testing**): anomalies in electronic monitoring equipment

- **1960s**: problems **were observed in space electronics** (difficult to separate *soft* failures from other forms of interference

- **1972** - **73**: **Hughes satellite experienced SEU** (communication with the satellite was lost during 96s). 1st SEU paper (IEEE TNS Journal)

- **1979**: 1st descriptions about the mechanism whereby a **sea-level cosmic ray** could cause a SEU in electronics

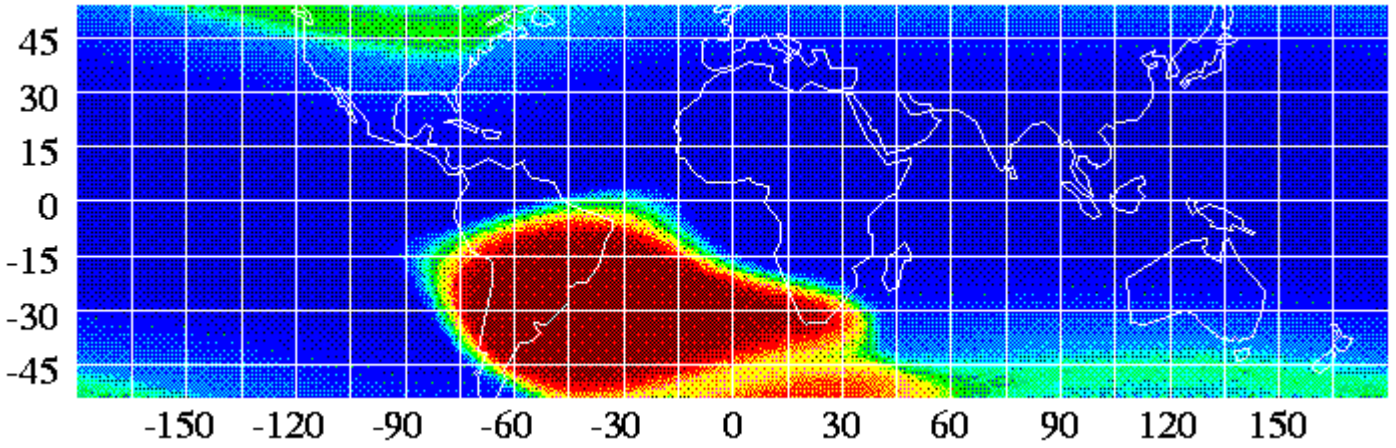
- **1984 - 90**: **systematic recordings of SEUs** on the **Tracking Data Relay Satellite System (TDRS-x) that provided communications for LEO satellites** (Hubble Space Telescope, Landsat), **Space Shuttle** (IEEE TNS, vol 38, n.6, Dec. 1991)

- since the beggining (**1990**): **Hubble Telescope has been stroggled with SEUs** (replaced SEU-sensitive RAM chips by rad-hard ones)

# Introduction – Why Rad Test is Important

**South Atlantic Anomaly** (**SAA**) is an area where the Earth's inner **Van Allen radiation belt** comes closest to the Earth's surface, dipping down to an altitude of 200 km.

This leads to an **increased flux of energetic particles** in this region and exposes orbiting satellites to higher-than-usual levels of radiation (so, **functional failure**).



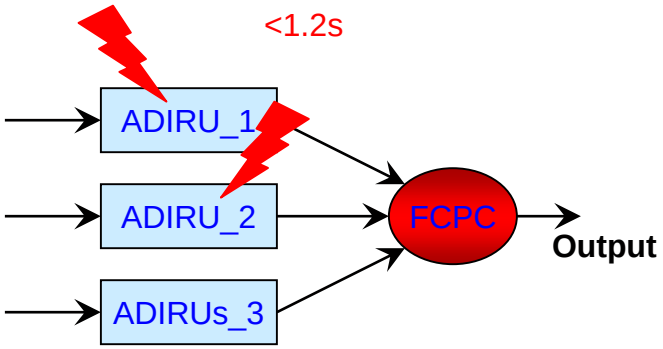
# Introduction – Why Rad Test is Important

A SEU is suspect to have occurred in the flight computers of the **Airbus A330** during **Qantas Flight 72 on 7 Oct. 2008 (Singapore-Perth)** which almost resulted in aircraft crash:

→ the aircraft made a sudden **uncommanded pitch down manoeuvre**, rapidly descending **200 m**.

Passanger expericenced “0 Gravity”

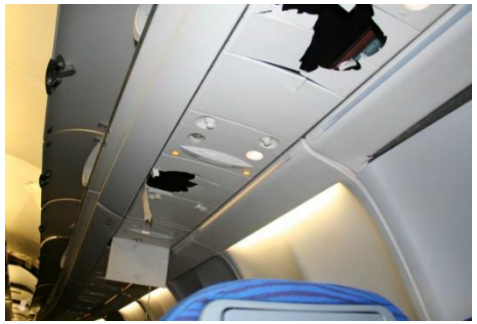
- **A**ir **D**ata **I**nertial **R**eference **U**nit (**ADIRU**): computes the AOA (Angle of Attack)
- **F**light **C**ontrol **P**rimary **C**omputer (**FCPC**): main computer unit



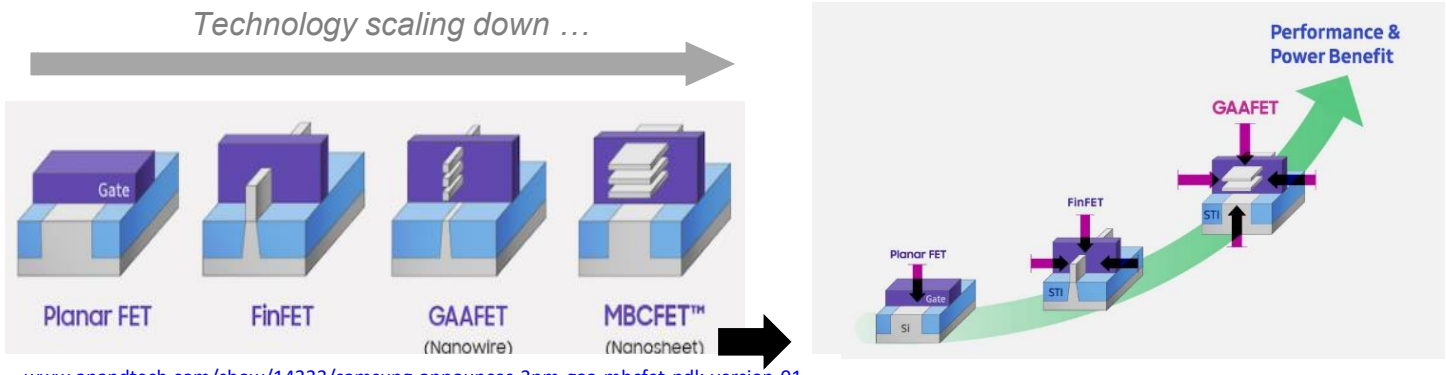

Tripple Modular Redundancy - TMR

When all 3 ADIRUs’ outputs agree (normal operation), **the average value** of ADIRU_1 & ADIRU_2 is used by the FCPC for computation

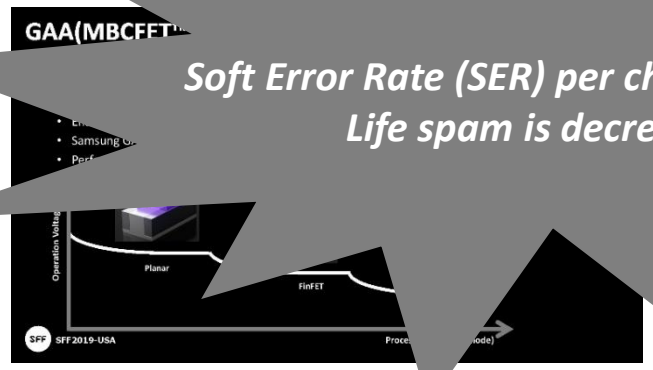
If either ADIRU_1 or ADIRU_2 significantly **deviates** from the other 2 values, the FCPC uses a memorized value for **1.2s**



# Technology Trends Impact on ICs




www.anandtech.com/show/14333/samsung-announces-3nm-gaa-mbcfet-pdk-version-01
Gate All Around, Multi-Bridge Channel FET



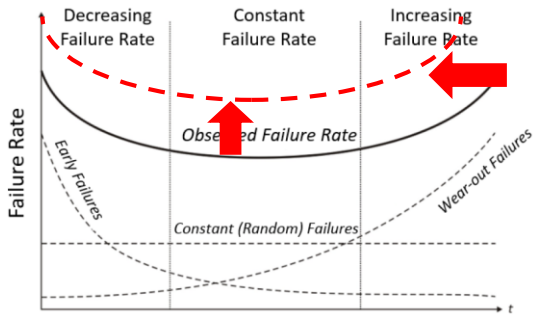

***Soft Error Rate (SER) per chip is increasing!***
***Life spam is decreasing!***

**Hot Topics for the incoming years !!!**

Single-Event Upsets (SEU)
&
Single-Event Transients (SET):

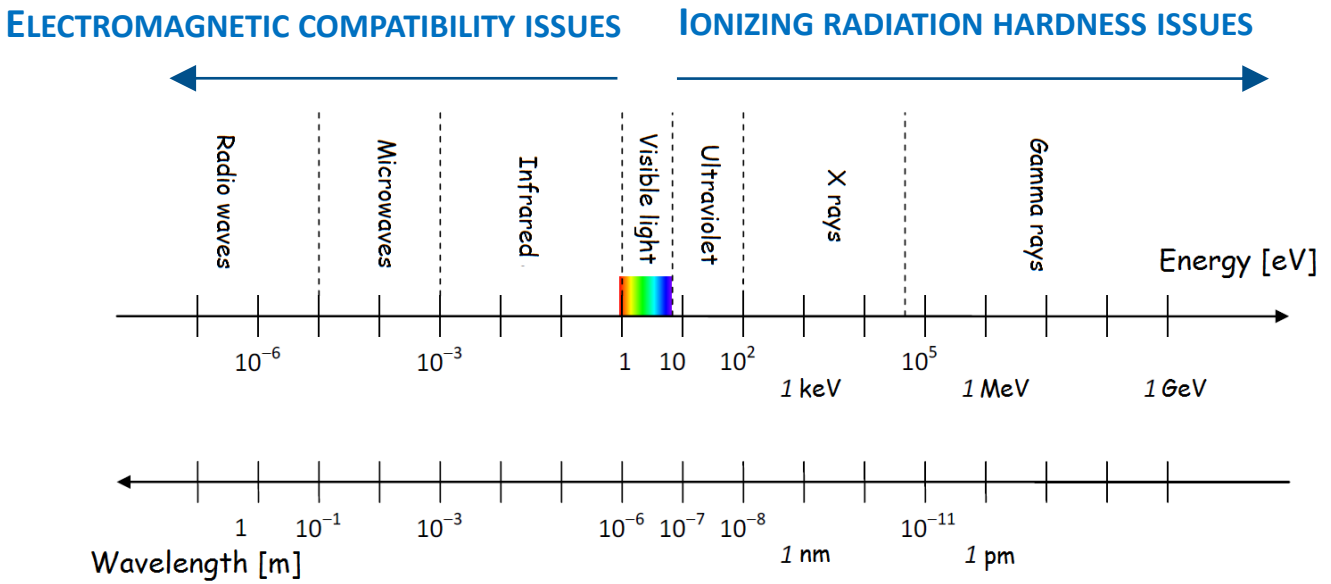
Total Ionizing Dose (TID):

Aging:

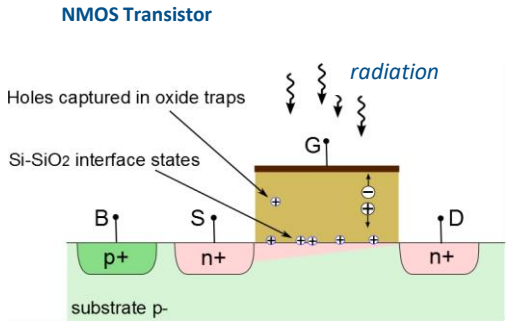


# Mechanisms by which Ionizing Radiation Affects Electronics and How they Impact IC Lifetime

# Frontier Between Ionizing & Non-Ionizing Radiations



# Total-Ionizing Dose (TID) in MOS



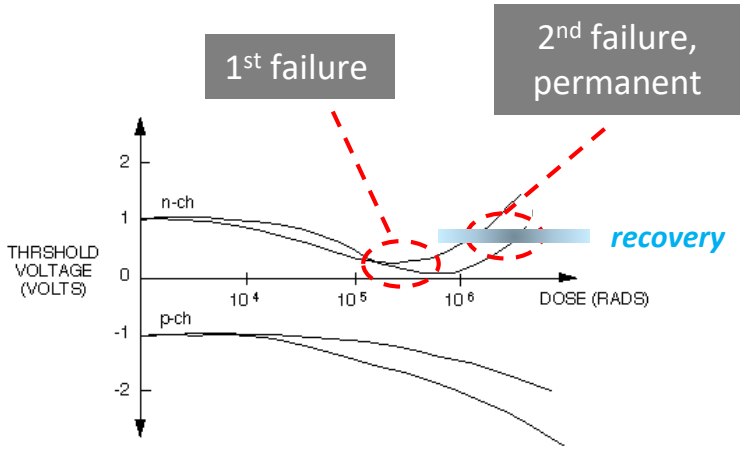

**TID** effects on CMOS ICs are caused primarily by positive charge trapped in insulating layers

⬇

For CMOS ICs, the main TID effect is the increase of leakage currents and change in $V_{th}$ of the devices

⬇

For high doses, a permanent functional failure of the circuit is observed.



# Single-Event Upset (SEU) in MOS

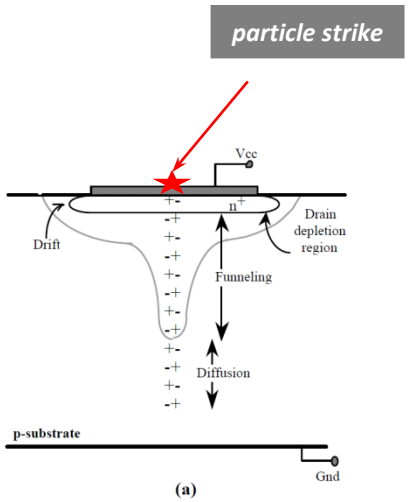
**Radiation (SEU) effects on CMOS ICs are mainly caused by high-energy particles striking reverse biased drain depletion region of off-transistors**

⬇

**For CMOS ICs, the main SEU effect is the loss of information stored in memory elements (FFs, RAMs)**

⬇

**Transient functional failure of the circuit is observed**



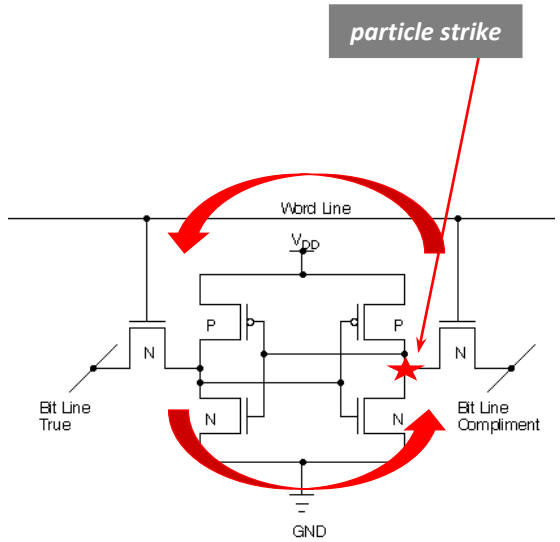




**Fig. 1.** Illustration of the charge collection mechanism that cause single-event upset: **(a)** particle strike and charge generation; **(b)** current pulse shape generated in the n+p junction during the collection of the charge.

# Single-Event Transient (SET) in MOS

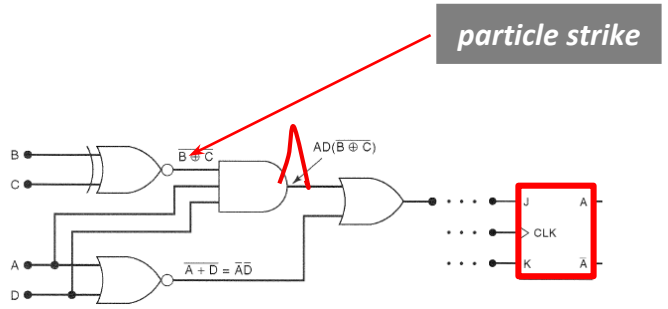
**Radiation (SET) effects on CMOS ICs are mainly caused by high-energy particles striking logic along with critical paths**

⬇

**For CMOS ICs, the main SET effect is the loss of information stored in memory elements (FFs, RAMs)**

⬇

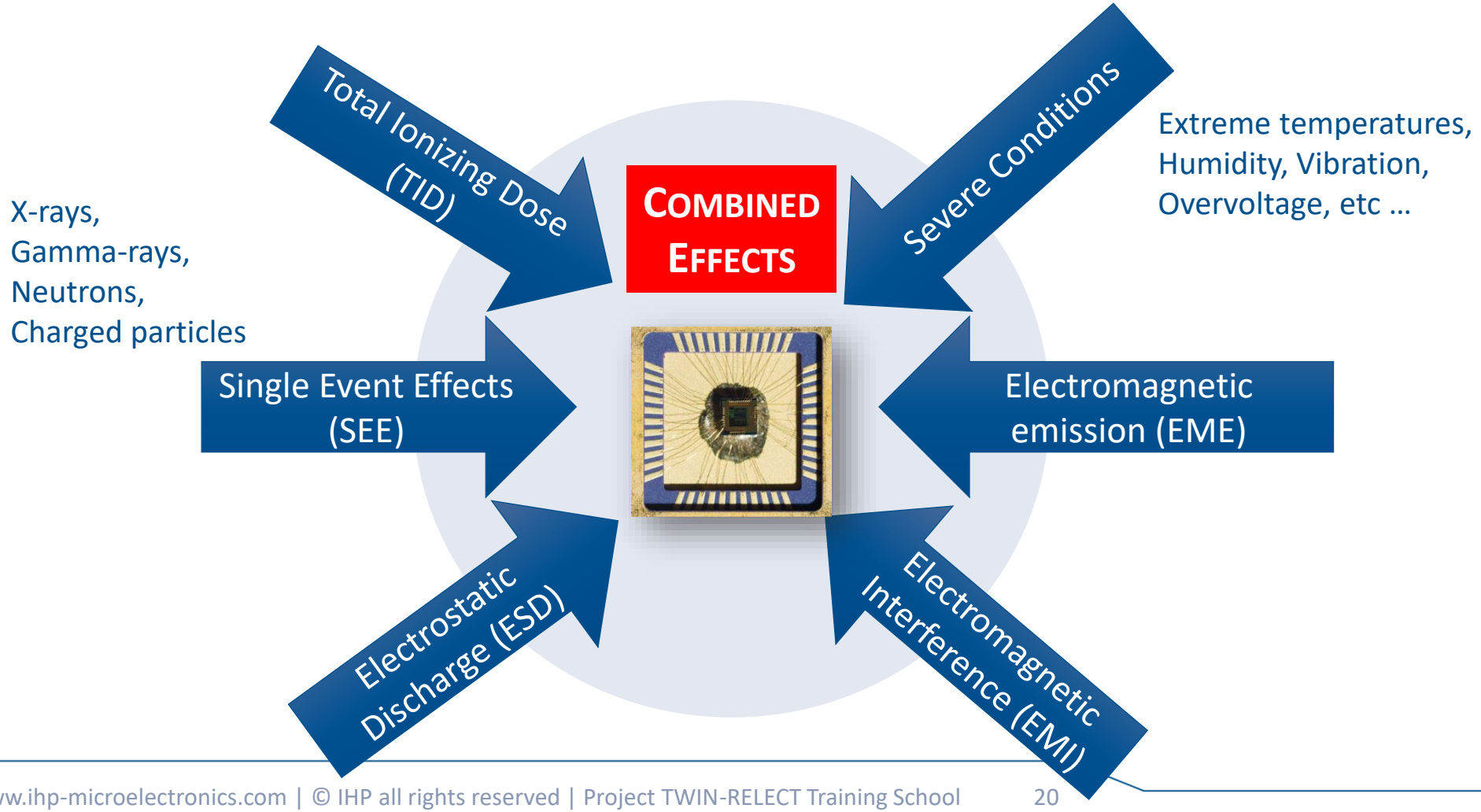
**Transient functional failure of the circuit is observed**



# The Need of Combined Tests for Ionizing and Non-Ionizing Radiations

# The Need for Combined Tests

- In a real system, various interferences can occur simultaneously.



# The Need for Combined Tests

**Only a few works** addressing the problem: trying to understand and quantify the combined effects of ionizing (**total-ionizing dose: TID**) and non-ionizing (**EMI**) radiations on ICs

**The Effects on Cardiac Pacemakers of Ionizing Radiation and Electromagnetic Interference from Radiotherapy Machines**
*(Int. Journal of Radiation Oncology Biol. Phys. Vol. 4. pp. IO55-IO58, 1978)*

**Pacemaker Failure Due to Radiation Therapy**
*(PACE. Vol. 5, pp156-159, March-April 1982)*

**When cancer patients with implanted pacers undergo radiation therapy** it is important to known whether the treatment will have any deleterious effects on the pacer, thus placing the patient in jeopardy from malfunction. Malfunction may consist of continuous or intermittent spurious signals or an interruption of normal pacer signals.

**Radiation therapy exposes a pacemaker to ionizing radiation alone ($^{60}$Co), or ionizing radiation plus strong electromagnetic fields** (linear accelerators and betatrons), which may induce noise and interference into reactive electronic circuits.

*"In our study, the observed **effect on pacemaker function was severe enough to justify some concern**"*

# The Need for Combined Tests

*From the best of our knowledge ...*

**Electromagnetic Interference and Ionizing Radiation Effects on CMOS Devices**
*(IEEE TRANS. ON PLASMA SCIENCE, VOL. 40, NO. 6, JUNE 2012)*

They observed: N- and PMOS devices presented **shift and distortion of the threshold voltage and current transfer characteristics**, leading to **reduced noise margins** and **logic instability**.

**They concluded: "*EMI + TID combination*** *proved most damaging, when compared to* ***isolated*** *EMI and ionizing radiation experiments"*

None work, except from our group, focused on the combined effects of ionizing (**soft errors in memory elements**) and non-ionizing (**EMI**) radiations on ICs

# The Need for Combined Tests

*From the best of our knowledge ...*

Absence of a **standard** to rule combined tests

***(currently, only a Draft Recommendation from ITU:***
***"Overview of particle radiation effects on telecommunications systems", Geneva, Oct. 2016)***

Our studies have shown a **considerable reliability degradation** for systems operating in harsh environments (such as space, where satellite electronics is exposed to the combined effects of ioninzing rad: TID/soft errors and EMI)

***(Analysis of SRAM-Based FPGA SEU Sensitivity to Combined EMI and TID-Imprinted Effects, IEEE TRANS. ON NUCLEAR SCIENCE, VOL. 63, JUNE 2016)***

# The Need for Combined Tests

**It is a common practice that …**

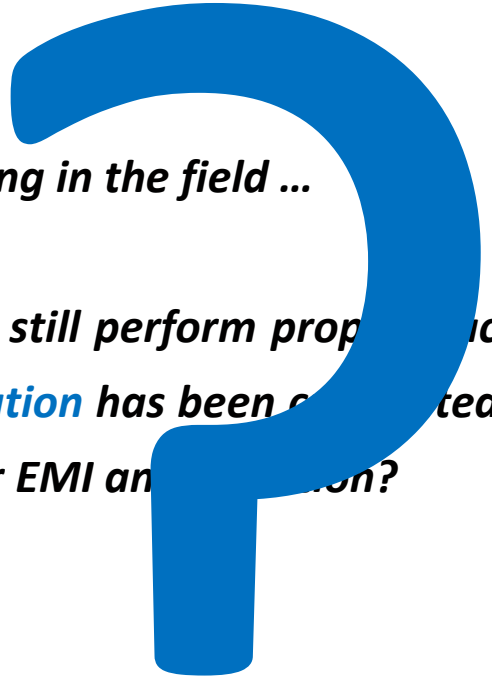
**engineers qualify electronic systems to EMI, TID or SEU, or eventually to all of them, but NOT taking into account the combined effects one phenomenon may take over the other.**

**e.g., assume a given part of an embedded system for satellite is certified by a set of EMI tests according to specific stds**

# The Need for Combined Tests

***After a given period of time operating in the field …***

***Who can ensure that this part will still perform prop… according to the same set of EMI stds, after a given level of TID radiation has been a…ted over time on the system, if the part was certified independently for EMI an…on?***



***Moreover, who can ensure that the system will be approved for the same set of EMI stds, if operating in a harsh environment with den… of high-energy particles (SEEs)?***

# The Need for Combined Tests

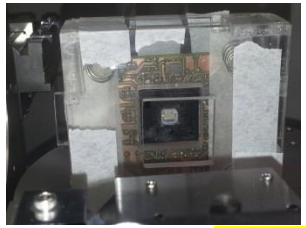
***In the light of this problem ...***

**We ...**

- **analyze the impact of combined tests for EMI + radiation (TID/SEU) on the reliability of electronic components**
- **propose a new methodology for design and test ICs that takes this combination into account in order to qualify state-of-the-art COTS ICs**

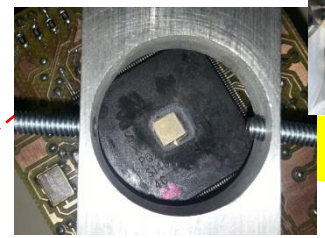
# TID & SEU Measurement Techniques at the IC Level

# Combined Tests: EMI + Ionizing Radiation

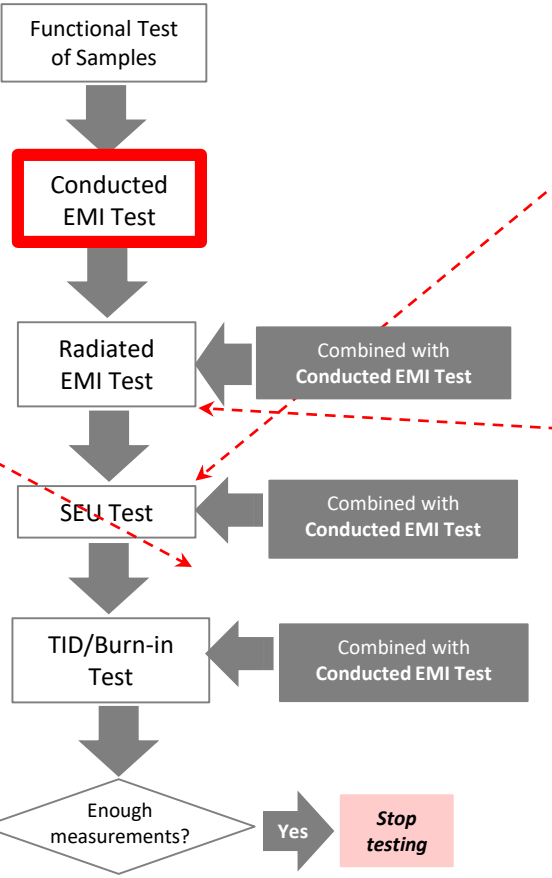


**X-Ray**

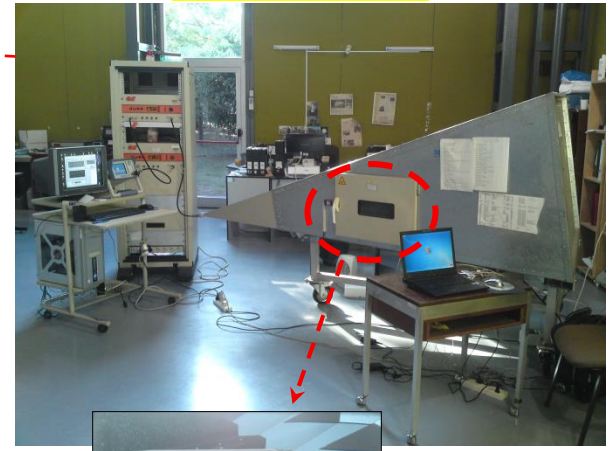
**Co$^{60}$ (Gamma Cell)**



**SEU**




**Radiated EMI Test (G-TEM Cell Test Method)**



# Ionizing radiation Testing Stds

US MIL-STD 883E

Establishes uniform methods, controls, and procedures for testing microelectronic devices suitable for use within military and aerospace electroni c systems

| METHOD NO. | ENVIRONMENTAL TESTS |
|---|---|
| 1001 | Barometric pressure, reduced (altitude operation) |
| 1002 | Immersion |
| 1003 | Insulation resistance |
| 1004.7 | Moisture resistance |
| 1005.8 | Steady state life |
| 1006 | Intermittent life |
| 1007 | Agree life |
| 1008.2 | Stabilization bake |
| 1009.8 | Salt atmosphere (corrosion) |
| 1010.7 | Temperature cycling |
| 1011.9 | Thermal shock |
| 1012.1 | Thermal characteristics |
| 1013 | Dew point |
| 1014.10 | Seal |
| 1015.9 | Burn-in test |
| 1016 | Life/reliability characterization tests |
| 1017.2 | Neutron irradiation |
| 1018.2 | Internal water-vapor content |
| 1019.4 | Ionizing radiation (total dose) test procedure |
| 1020.1 | Dose rate induced latchup test procedure |
| 1021.2 | Dose rate upset testing of digital microcircuits |
| 1022 | Mosfet threshold voltage |
| 1023.2 | Dose rate response of linear microcircuits |
| 1030.1 | Preseal burn-in |
| 1031 | Thin film corrosion test |
| 1032.1 | Package induced soft error test procedure (due to alpha particles) |
| 1033 | Endurance life test |
| 1034 | Die penetrant test (for plastic devices) |

# Ionizing Radiation Testing Stds

**European Space Agency**

**Agence Spaciale Européenne**

**TOTAL DOSE STEADY-STATE IRRADIATION**

**TEST METHOD**

**ESA/SCC BASIC SPECIFICATION No. 22900**

**SINGLE EVENT EFFECTS TEST METHOD**

**AND GUIDELINES**

**ESA/SCC Basic Specification No. 25100**

**space components**
**coordination group**

# Lab Equipment for Ionizing Radiation Test

**Goal**:

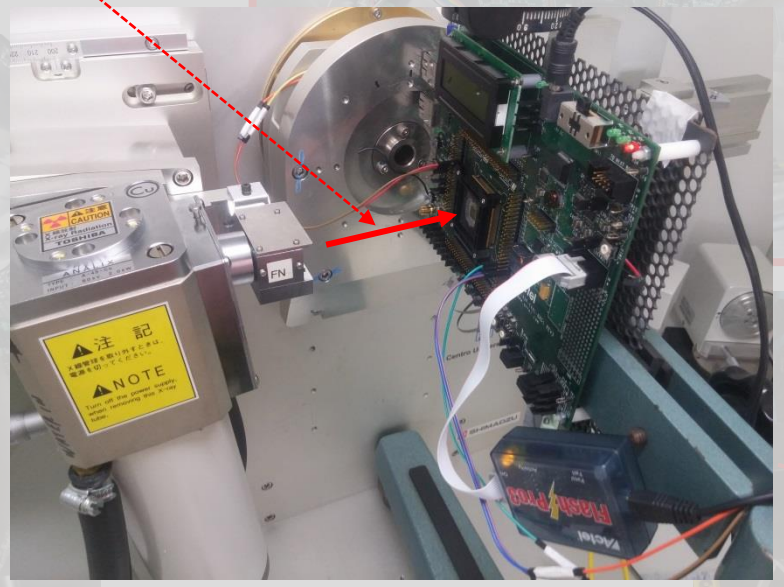
**SEU** sensitivity w.r.t. $V_{DD}$

**Disruption** and **TID**

**Microsemi ProAsic3E1500**

**TID**
**(X-Ray Diffractometer)**

Beam direction




SEU
(Heavy Ions Accelerator)

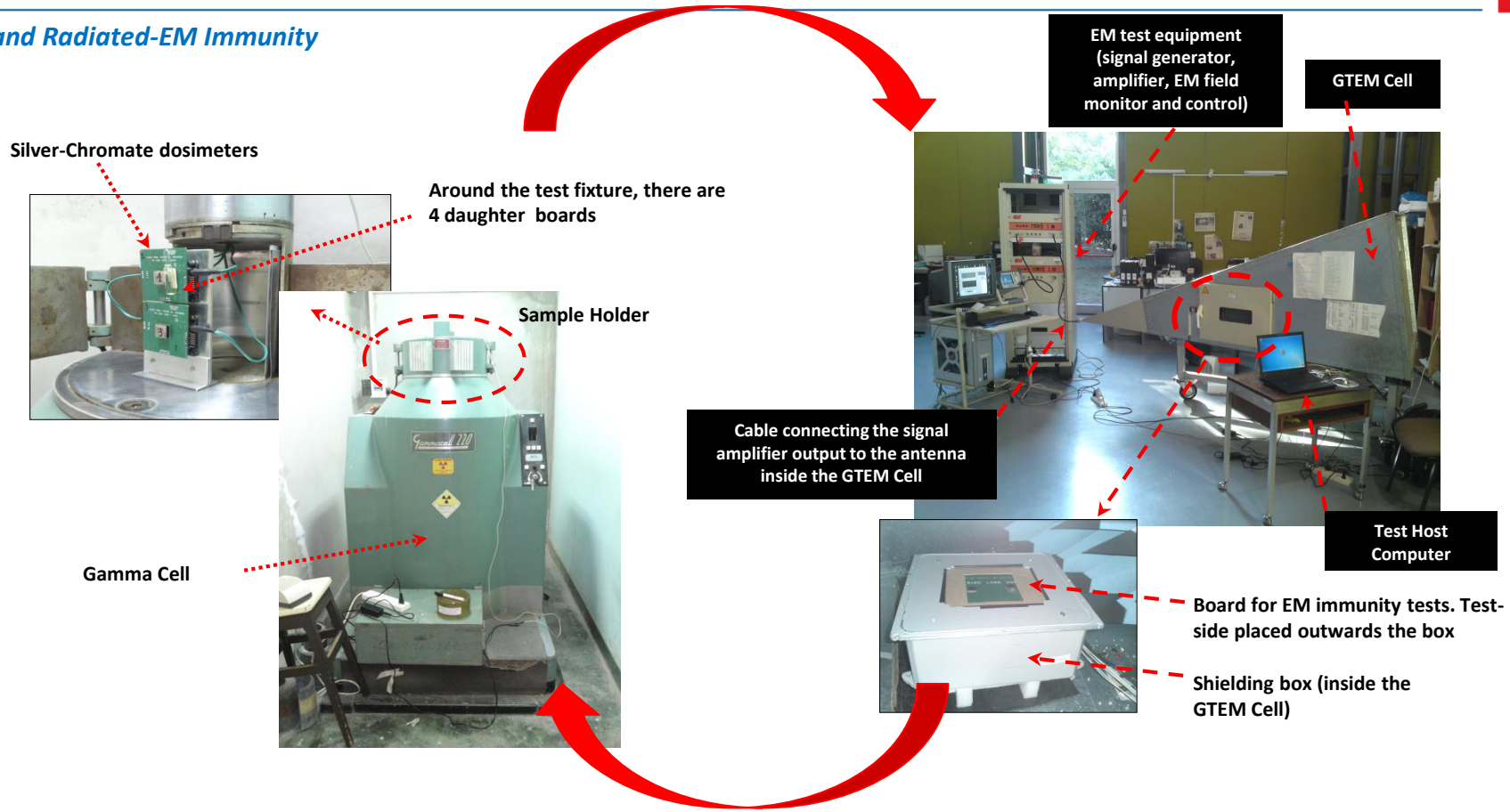
Local Test Host Computer

IEC 61.0004-29-Compliant
EMI Noise Generator

# Lab Equipment for Ionizing Radiation Test

Combined tests: ***TID ($Co^{60}$) and Radiated-EM Immunity***

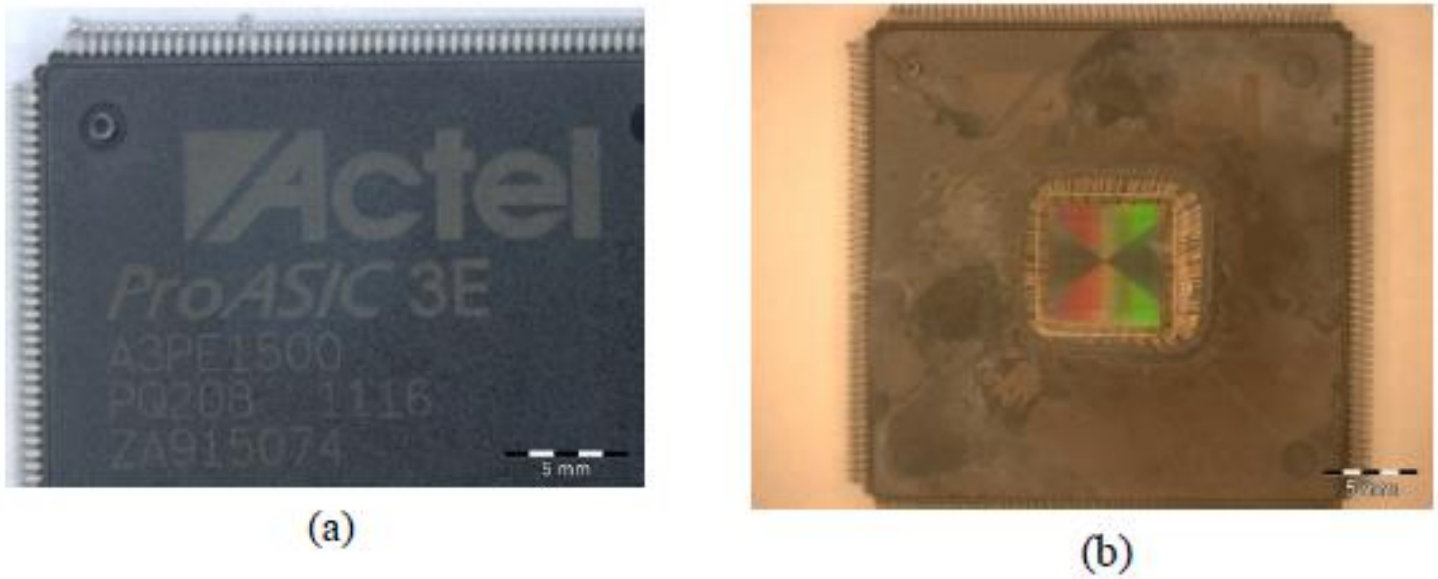
**Test Environment**




Radiation source used for gamma radiations.

Environment for radiated EM immunity measurements.

# Lab Equipment for Ionizing Radiation Test

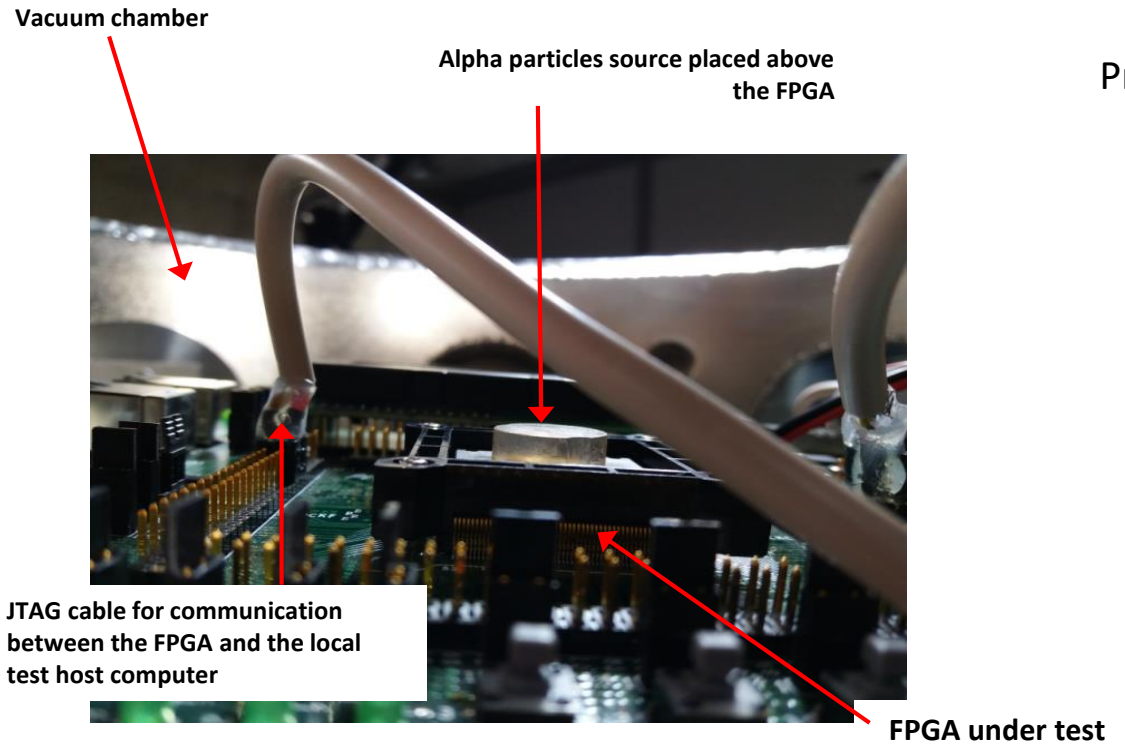



**Microsemi ProAsic3E A3PE1500 FPGA**:
(a) Packaged device;
(b) Unpacked, ready for radiation (SEU and TID) tests.

(commonly used for automotive and aerospace apps)

# Lab Equipment for Ionizing Radiation Test

## SEU Test:




**Test setup for the $^{241}$Am source**

ProASIC3E FPGA exposed to 5.4 MeV alpha particles emitted by a $^{241}$Am source

Alpha-particle flux:.
Appr. 1,300 part/cm$^2$.s
(13.7 particles/second /millisteradian)

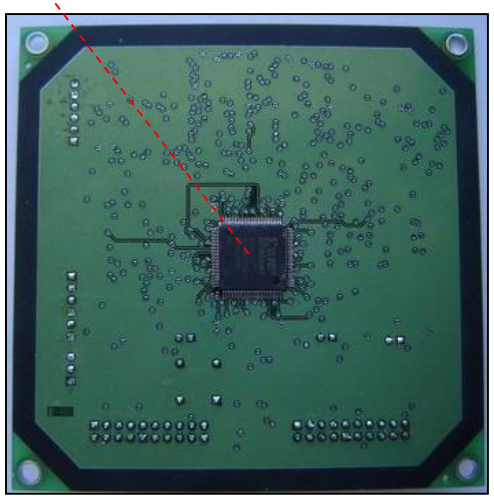
**Microsemi ProAsic3E A3PE1500**

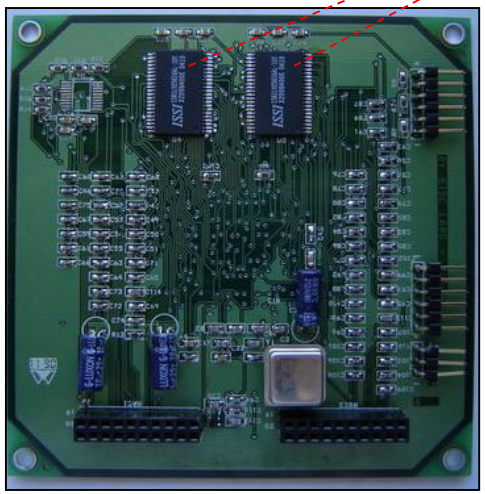
# Platforms for Combined Test

FPGA (System-on-Chip)

16MB SRAM (RTOS + user application)

System under Test





Top view

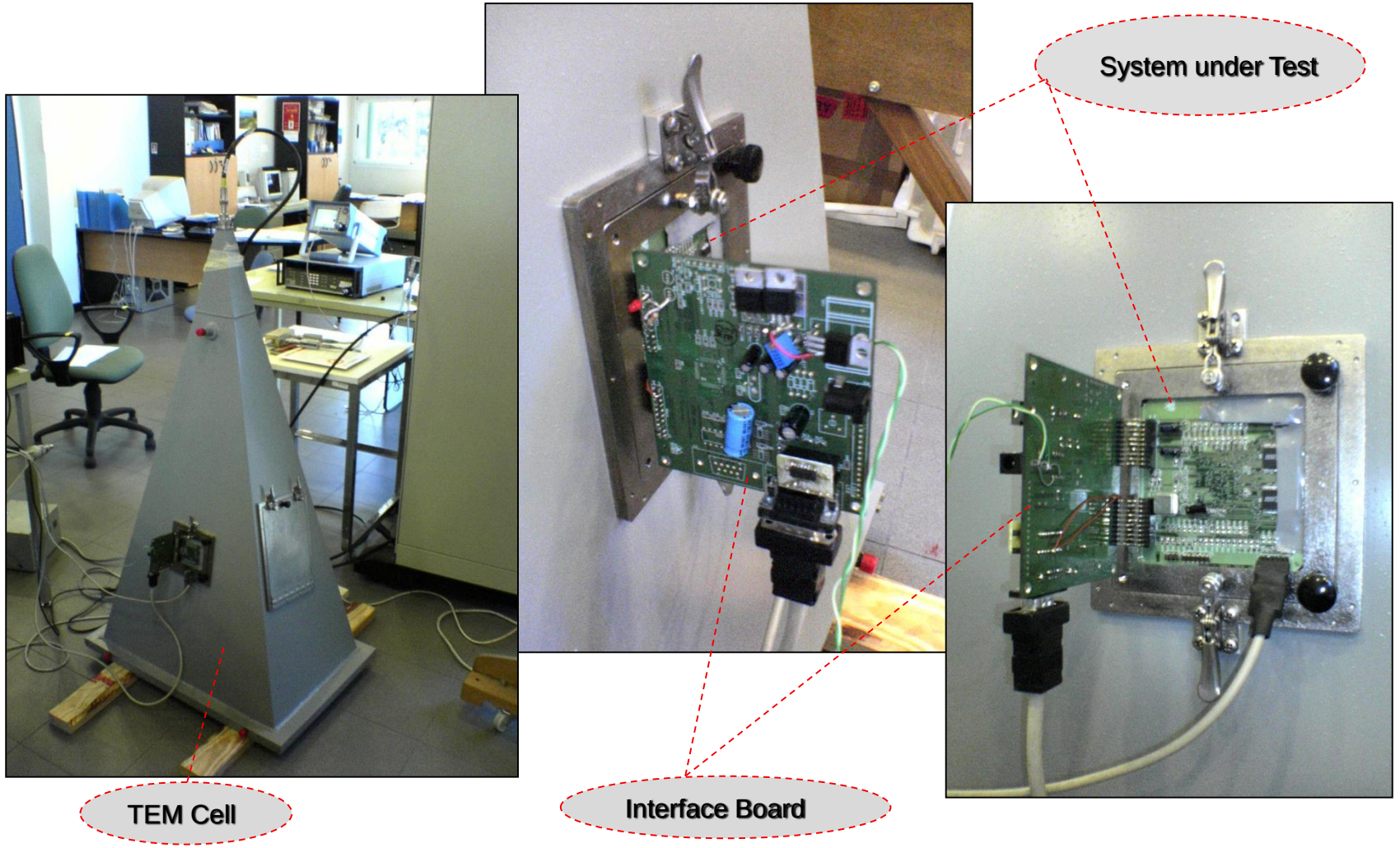
Bottom view

**IEC 62.132-2 std compliant board.**

**Four-layers: Gnd (top) - signal - signal - Vdd (botton).**

1st

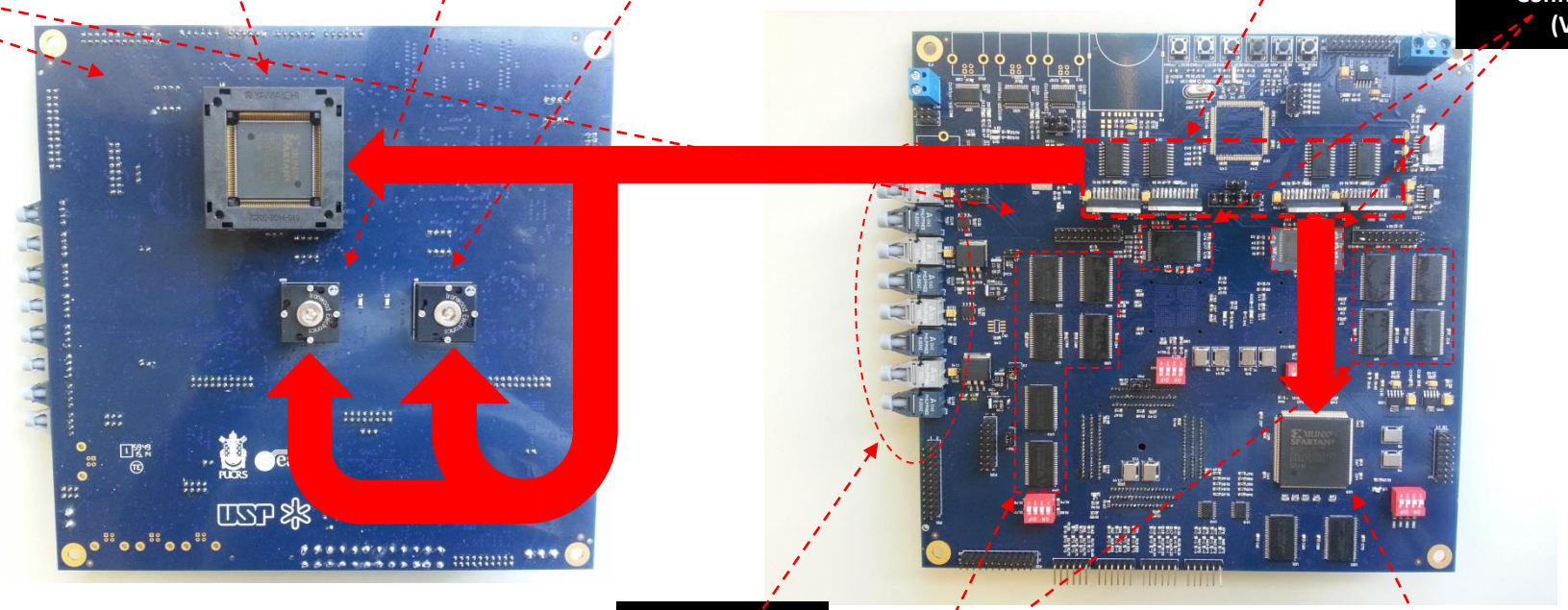
# Platforms for Combined Test




1st

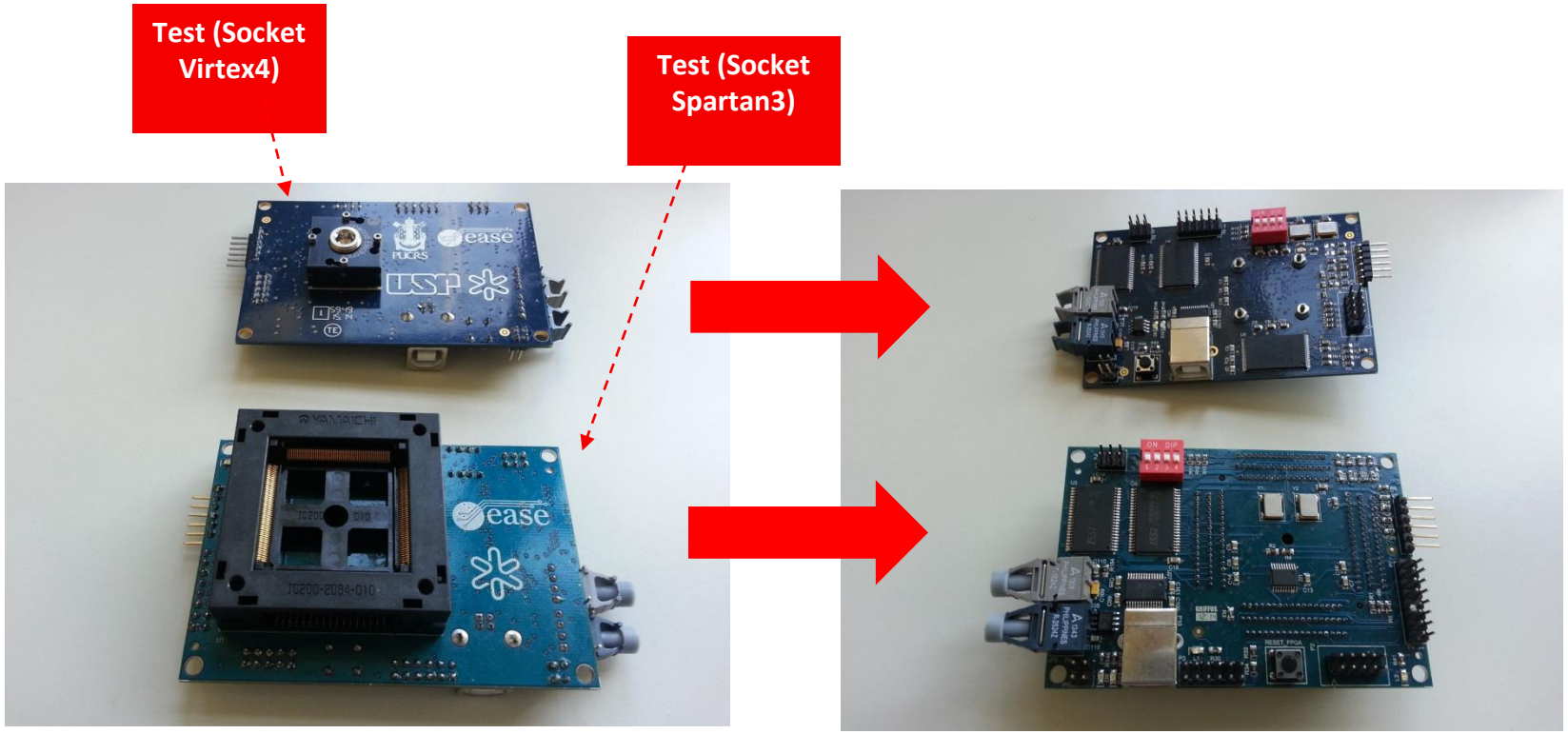
# Platforms for Combined Test

**12-layer Motherboard for Combined EMI x Radiation tests**




4th

# Platforms for Combined Test




Top (test side)

Bottom (glue logic)

4th

**6-layer Daughterboards for Combined EMI x Radiation tests**

# Mitigation Approaches

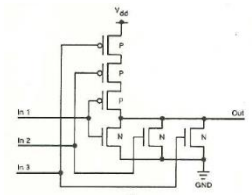
# Mitigating Total-Ionizing Dose (TID)

- ***Use of guardbands: slow down clock frenquency (add extra timing margins)***

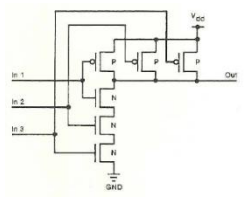
- ***Prefer use of modern technologies (insead of old, mature ones): scaling down is always a good option since nanotechnologies (typically under 65nm) are strongly TID-tolerant***

- ***Use of TID-tolerant std cells library (build-up pMOS devices much larger than nMOS devices, replace NOR gates by Nand ones, etc ....)***

CMOS circuit schematic:
(a) NOR gate; (b) NAND gate:



(a)



(b)

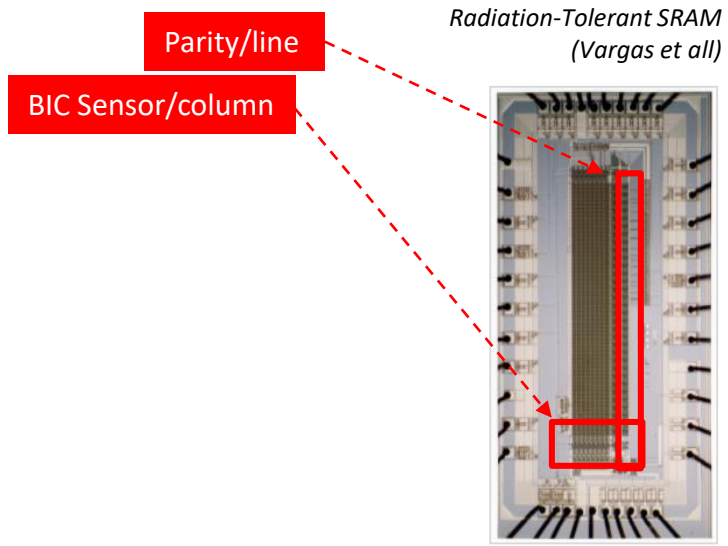
NAND gate has shown in $Co^{60}$ tests to retain a higher degree of its original noise margins with radiation and is thus the preferred logic gate for hardened IC designs.

If NOR gates must be used in circuits designed for space, the # of inputs (i.e., the fan-in) should be minimized.

# Mitigating Total-Ionizing Dose (TID)

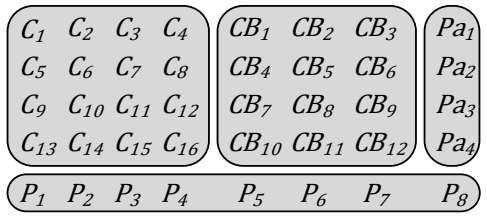
***Use of HW, SW, Time & Information (EDAC) Redundancy such as TMR, Functional Units Duplication with Comparator, Interleaving, etc ...***

- ***Use of Build-In Current Sensors (BICSs)***

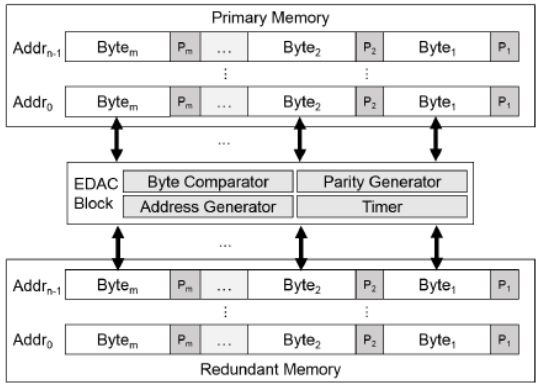


# Mitigating Single-Event Upset (SEU)

***EDAC in Memory Array*: *Parity*, Hamming Extended, Checksum, CRC, Reed-Muller, Matrix, CLC, ...**




**Codified CLC word model**

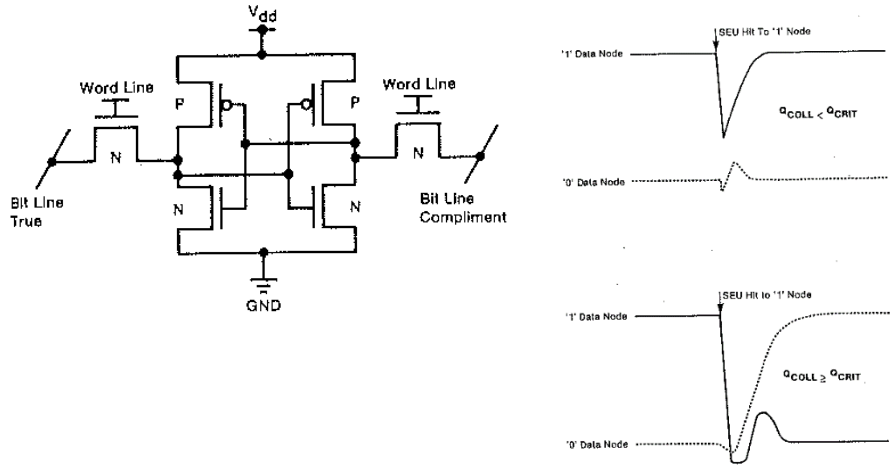



**Parity-per-Byte and Duplication (PBD) Approach**

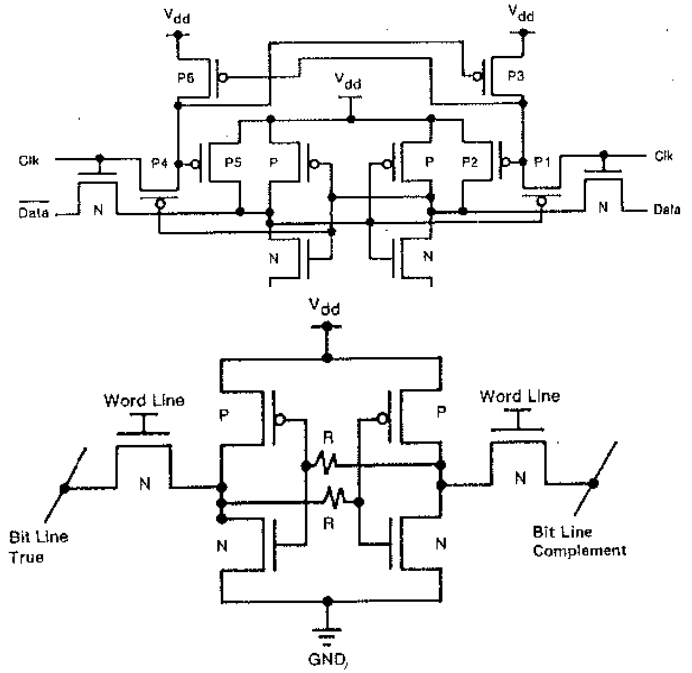
# Mitigating Single-Event Upset (SEU)

**Use of SEU-tolerant std cells library: design rad-hard SRAM cells**

Classic CMOS SRAM cell schematic and the critical charge ($Q_{crit}$):




Design-hardened CMOS SRAM cell schematics:



# Mitigating TID & SEU

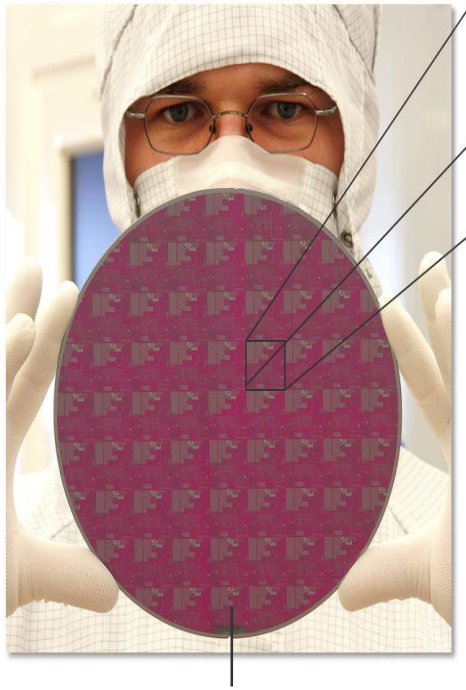
Use of **130nm BiCMOS RadHard IHP** (SG13RH): **phase 2 evaluation testing i.a.w. 2269010 (Endurance)**.

*For inclusion in the **ESA preferred parts list (EPPL)** for space applications.*

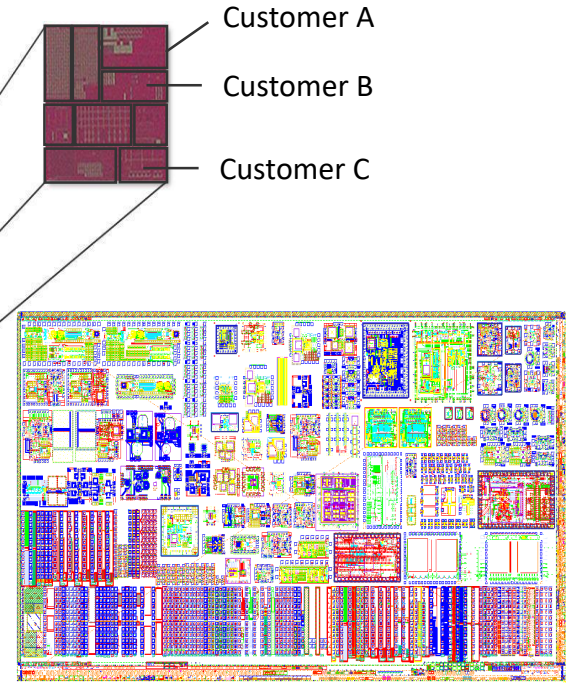
**RHBD Library**: **ELT** Transistors, **TMD FF with Voter and Self-Correction Mechanism** (clockless, instant error mitigation).

Std version of this technology: **available on Open PDK**.

**Moreover: service approach - Multi Project Wafer**



200 mm Silicon Wafer



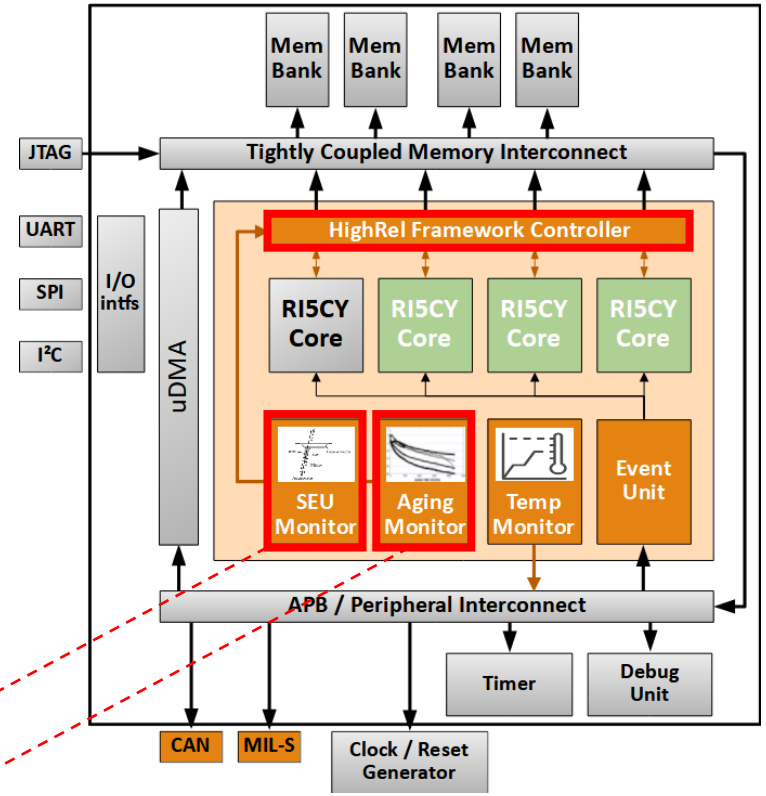

Internal and external customer layouts and structures for technology research (3-5 technologies in one mask set)

# TetRISC SoC Solution

A **highly reliable resilient quad-core multiprocessing system**: **TetRISC** (**TET**ra Core System based on **RISC**-V) **SoC**, has been developed

It monitors **multiple fault sources** to **adjust (in real-time) system reliability** in harsh environments

Based on the **open-source PULPissimo** single-core architecture.




Allows **EDAC** and **Error Rate prediction**

Allows **aging prediction**

# TetRISC SoC Goal and Main Modules

**TetRISC objectives**:

1. implement a **RISC-V based resilient multiprocessing system**
2. enable **on-chip *reliability* monitoring**
3. **dynamically reconfigure the system** into different **operating modes in real-time** (based on **multiple on-chip sensors** and **user requirements**)
   - **3.1 (A)** Normal, **(B)** Dup&Comp, **(C)** Triple-Molule Redundancy, and **(D)** N-Module Redundancy (NMR)
   - 3.2 Can be combined with **Clock Gating** Approach

**Final Goal:** **achieve optimized switching** between different operating modes (to enable trade-off: **reliability ↔ power consumption ↔ performance**)

# On-Chip Sensor: SEU Monitor & In-Flight SEU Rate Prediction

Each memory word comprises **40 bits** (**32** bits used for data storage + **8** EDAC bits).

SEU Monitor:

(A) based on an Error Detection and Correction (**EDAC**) method, a **scrubbing** module, and a **dedicated process to identify** all upsets and distinguish the type of faults that occurs in each SRAM word.

(B) **integrated into the memory interface controller** of the Tightly Coupled Memory Interconnect (TCMI).

# On-Chip Sensor: SEU Monitor & In-Flight SEU Rate Prediction

In addition to **EDAC-based on Extended Hamming Code** to detect and correct errors in memory…

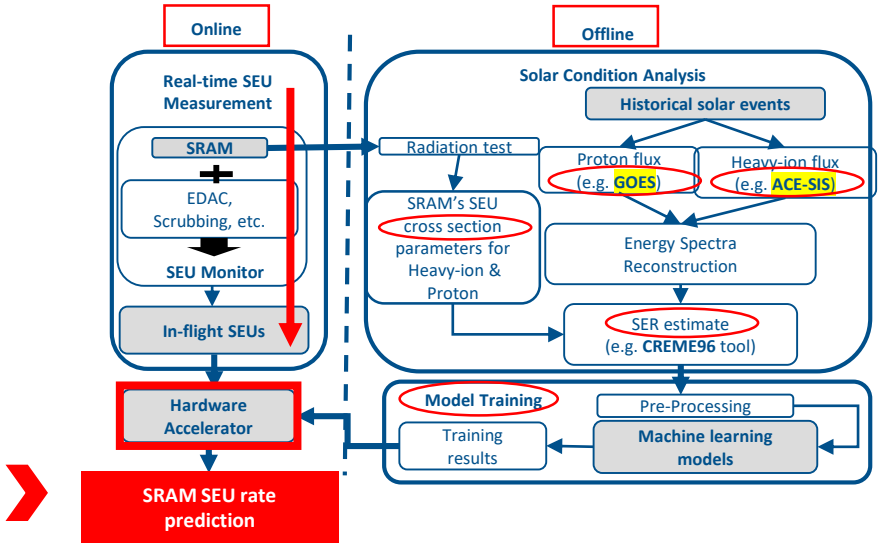
… the proposed SEU monitor can also **predict in-flight SRAM SEU rate**

based on **AI training** and **HW accelerator**:

(A) cross-section determination

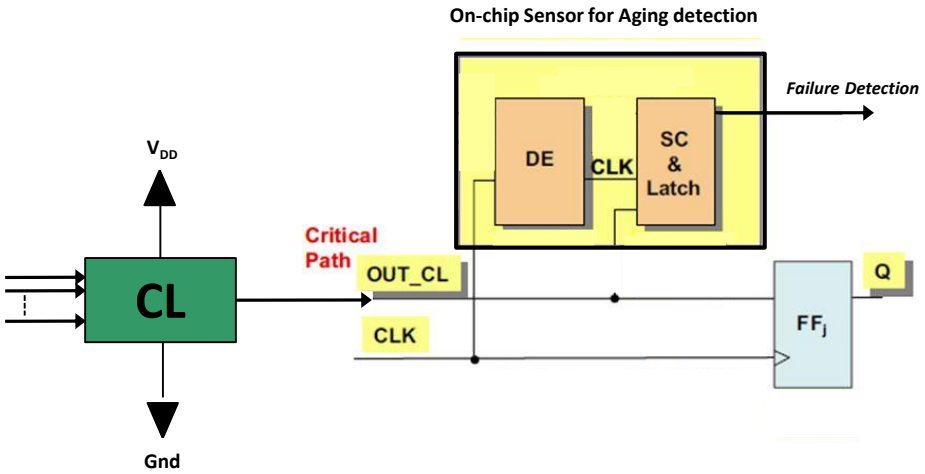
(B) use of available **public historical space particle flux databases:** (**GOES**) and (**ACE-SIS**) from previous space missions

(C) **Machine Learning** Model



# On-chip Aging Sensor

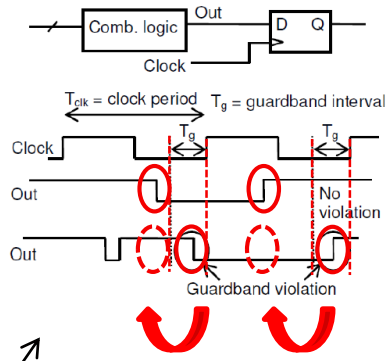
M. Valdés, J. Freijedo, M. J. Moure, J. J. Rodríguez-Andina, J. Semião; F. Vargas, I. C. Teixeira, J. P. Teixeira
"**Programmable sensor for on-line checking of signal integrity in FPGA-based systems subject to aging effects**"
2011 12th Latin American Test Workshop (LATW)
doi: 10.1109/LATW.2011.5985926.




According to the **degree of aging detected** by the sensor, **it increases the $V_{DD}$ source**.

**Fresh circuit**

**Old circuit**




Aging sensor detects ***guardband* violation** during circuit operation.

**Other counter measures:**

**Application of rejuvenation algorithms**

**Op frequency reduction**

**Power up spare units**

**etc …**

# TetRISC Demonstrators

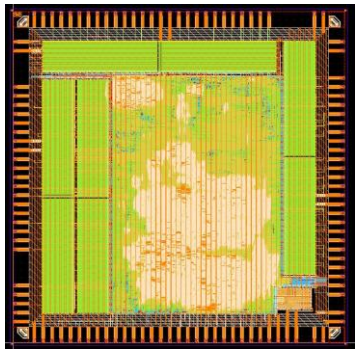
## (1) ASIC Demonstrator

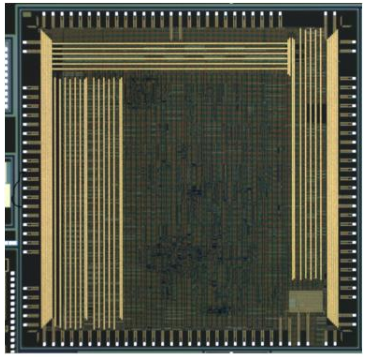
Manufactured in **130nm BiCMOS RadHard** IHP Technology
TETRISC SoC in **Ceramic-Socket**
Wafer probe test: approved
Currently: under **packaging process**
**Board manufactured** and ready

**Scale4Edge Chip**
RISC-V processor
**43.56 mm²**

(39.17% allocated to four 8192 x 40-bit shared L2 SRAM blocks that can also serve as sensing elements for radiation monitoring)

**Tape-out: July 2022**





# TetRISC Demonstrators

## (2) FPGA Demonstrator

**ARTIX-7 FPGA**
IHP Fault injection in cores (RTL) → **Saboteurs**
**Fault injection by means of switch at board level**
LCD display outputs **detection status**



TETRISC operating in the **following modes** during **fault injection** campaign in cores:

Quadruple Modular Redundancy (**QMR**)

# QMR with Fault Injection

**QMR for cores 0,1,2,3** with **Master Core 0**

Expect:

During QMR, cores 0,1,2,3 run the same task and display the result of core0

The framework controller can detect the erroneous core & the majority output can be determined if only one or two cores fail

The output display can show the correct output of C0, and fault core status could be restored if possible

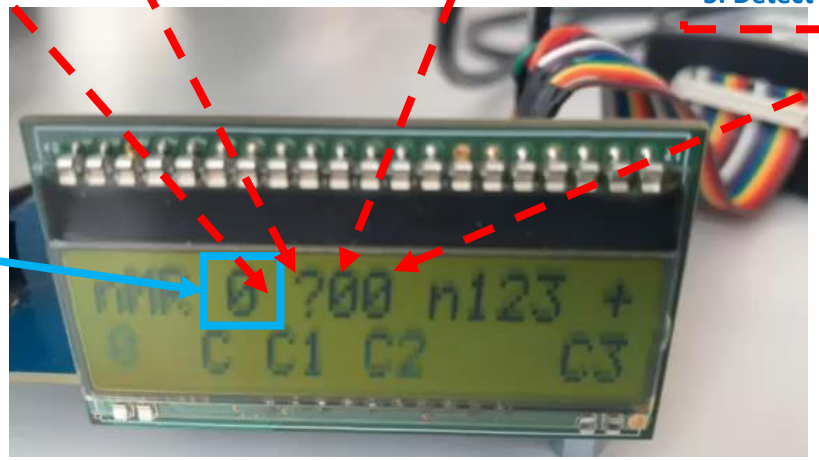
Majority output cannot decide: show in step 5

**Enabled cores: all cores enable (1111:?)**

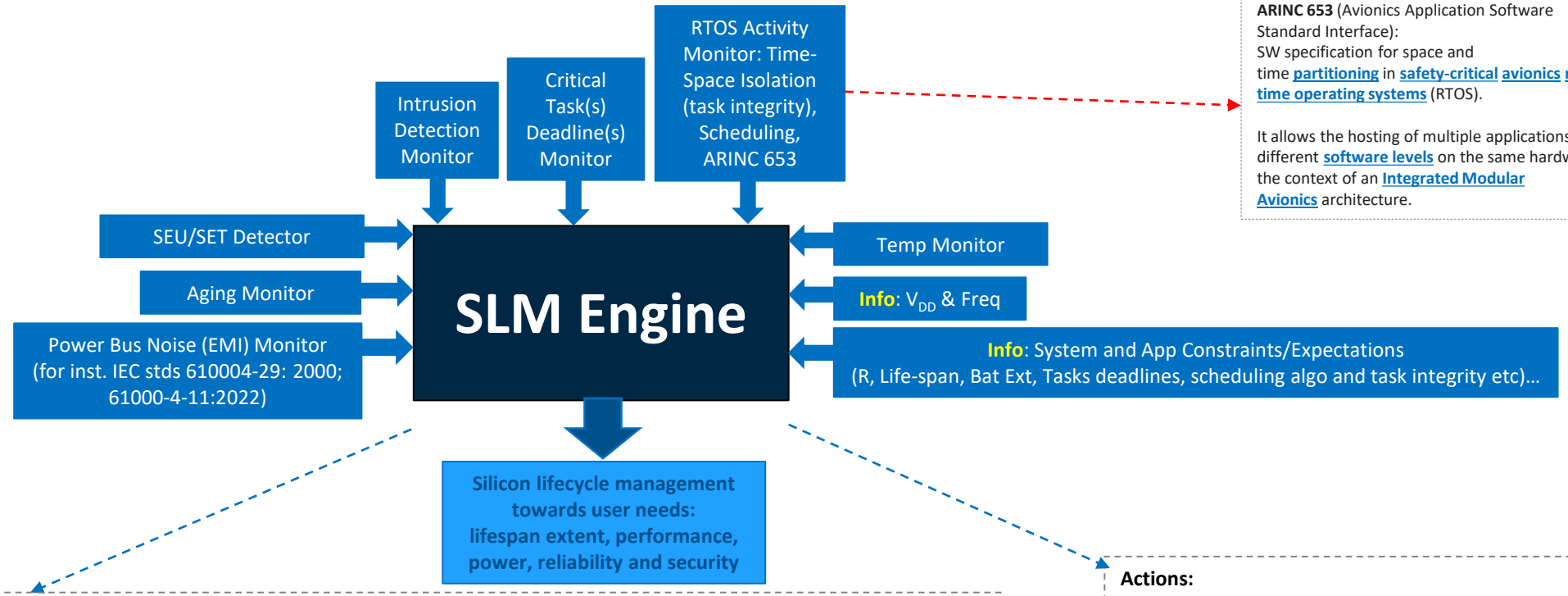
Cores in NMR:
**1. 0000:0**
2.-5. **QMR 1111:?**

Fault cores:
1.-2. Not detect fault
**3. Detect fault core 0 (0000:1)**
**4. Detect fault core 0&3 (1001:9)**
**5. Detect fault core 1&2&3 (1110:>)**

FPGA input seq:
1. No fault injection & use default mode
2. Active mode
3. **Fault inject on Core 0 (0001:1)**
4. **Fault inject on Core 0&3 (1001:9)**
5. **Fault inject on Core 0&1&3 (1101:=)**



# Resilient System for Critical Applications




**ARINC 653** (Avionics Application Software Standard Interface):
SW specification for space and time **partitioning** in **safety-critical** **avionics** **real-time operating systems** (RTOS).

It allows the hosting of multiple applications of different **software levels** on the same hardware in the context of an **Integrated Modular Avionics** architecture.

**Reactions/Countermeasures:**

- Increase/Reduce $V_{DD}$, Op. Freq to guarantee expected lifespan, reliability, power, performance, ...
- Activate/Deactivate HW-SW-Time-Info Redundancy as response to SEU/SET/EMI
- Retire/Activate redundant cold/hot spare blocks to counteract with aging
- Execute rejuvenation algorithm to partially anneal aging
- Kill/Hold less critical task(s), Restric system resource access (RAM, Bus, I/O) to guarantee crit. task(s) deadline/integrity
- Change/Restart task scheduling algorithm (to recover from scheduling faults)

**Actions:**

- Power-on check for aging
- Periodical (off-line/deterministic) sanity checks for aging
- Online check for SEU/SET, EMI
- Online check for task scheduling, deadline, and integrity

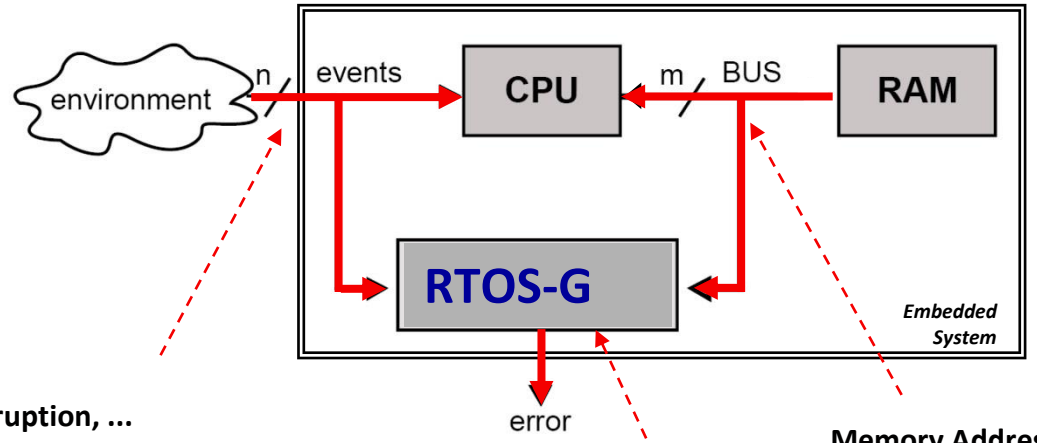
# Case-Study on Combined Test

# Combined Test: Conducted EMI and TID

**IP Core: RTOS-Guardian (RTOS-G), a watchdog to monitor RTOS activity in embedded systems**

☞ **the RTOS-G targets faults that ESCAPE detection by the native structures present in the RTOS kernel.**

# Combined Test: Conducted EMI and TID




**Events: Tick, interruption, ...**

**(Reference for**

**Task Context Switching)**

**RTOS-G identifies the current task under execution by correlating addresses flowing through the bus with the information stored in an Address Table generated during the compilation process.**

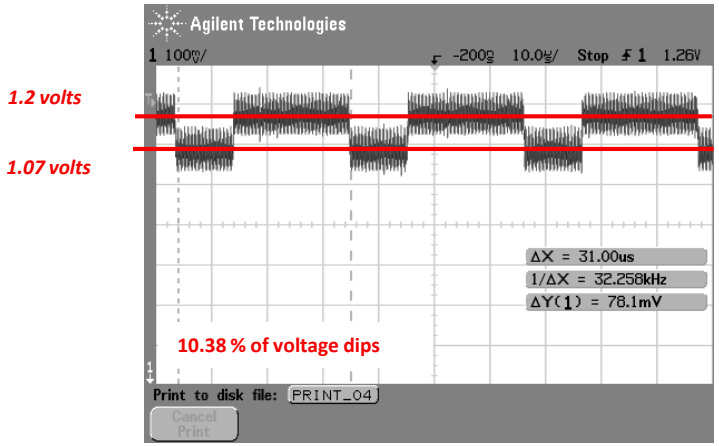
**Memory Addresses accessed by the processor.**

**Block diagram of the target embedded system**

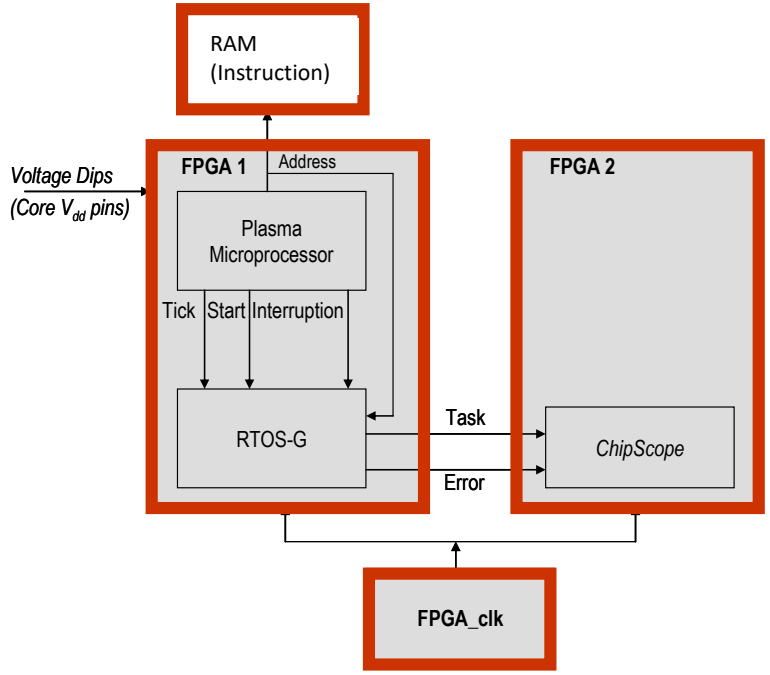
# Combined Test: Conducted EMI and TID

**Fault injection campaign:** ***generated according to the IEC 61.000-4-29 Int. Std. for conducted EMI on the DC input power port of (fresh) FPGA 1***

**Voltage dips** were randomly injected at the **FPGA 1 $V_{dd}$ input pins** at a frequency of **25.68 kHz** and consisted of dips of about **10.83% of the nominal $V_{dd}$**.




Injected noise at the FPGA power bus (conducted EMI)




Fault injection environment

# Combined Test: Conducted EMI and TID

**Results for Fault Detection**

***As long as more complex services of the kernel are used, the higher is the RTOS error detection.***

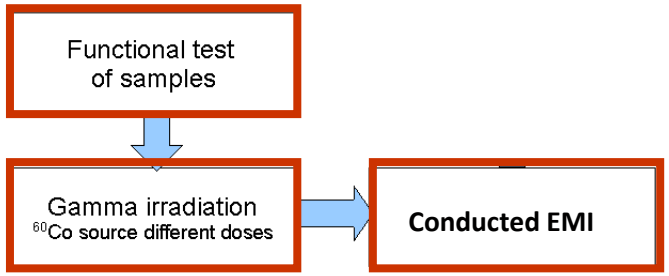
| Benchmark | RTOS Kernel [%] | RTOS-G [%] |
|---|---|---|
| *BM1* | 2.40 | 99.90 |
| *BM2* | 25.90 | 100.00 |
| *BM3* | 45.80 | 100.00 |
| *Average* | *24.70* | *99.97* |

*The native fault detection mechanism (**assert() function**) is called by the kernel every time RTOS runs its services (message queues, semaphores).*

# Combined Test: Conducted EMI and TID

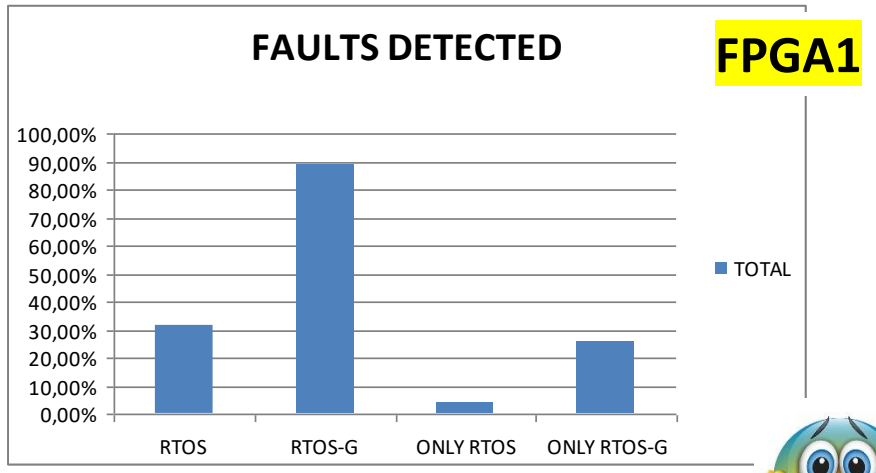

**Fault injection campaign:**

***TID irradiation of FPGA1 in a Gamma Cell with $Co^{60}$***



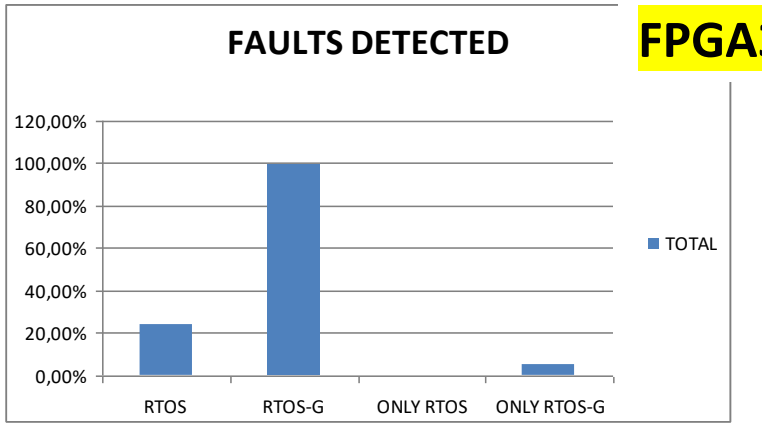

| Experiment | FPGA0 (krads) | FPGA1 (krads) | FPGA2 (krads) | FPGA3 (krads) | FPGA4 (krads) |
|---|---|---|---|---|---|
| 1st experiment | 0 | 5.6 | 51.9 | 111.0 | 216.0 |
| 2nd experiment | 0 | 217.6 | 263.9 | 323.0 | --- |

# Combined Test: Conducted EMI and TID



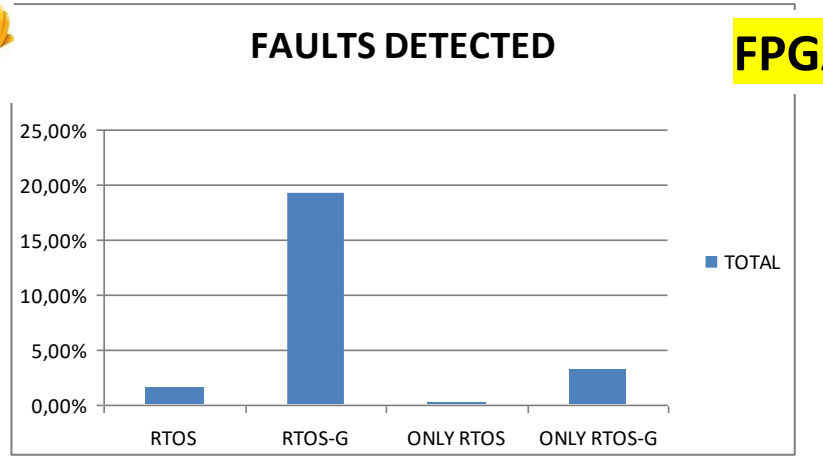

**FPGA1**

**RTOS: 18,00%**




**FPGA3**

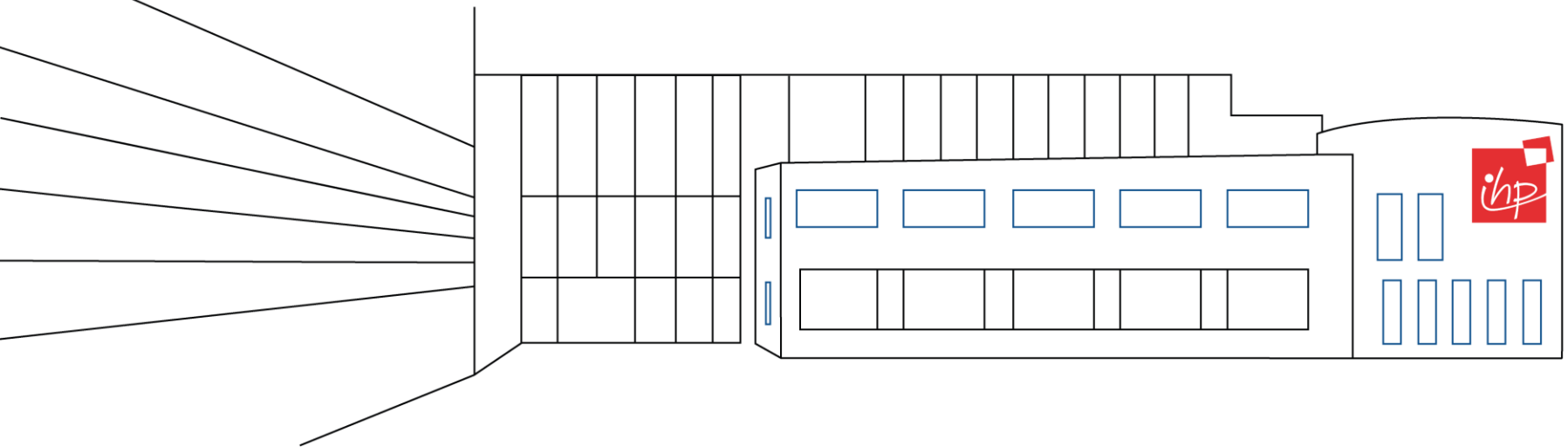
**RTOS-G: 68,67%**




**FPGA2**

# Thank you for your attention!

**IHP GmbH – Leibniz Institute for High Performance Microelectronics**
Im Technologiepark 25
15236 Frankfurt (Oder)
Tel.: +49 (0) 335 5625  494
E-Mail:  vargas@ihp-microelectronics.com



Leibniz Association