TWINRELECT 1st Scientific Workshop
Fault Modeling & Techniques for Fault Tolerance Analysis
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Probabilistic Single Event Transient Analysis & Optimisation for VLSI Circuits using Static Timing Analysis Principles

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UK Research and Innovation

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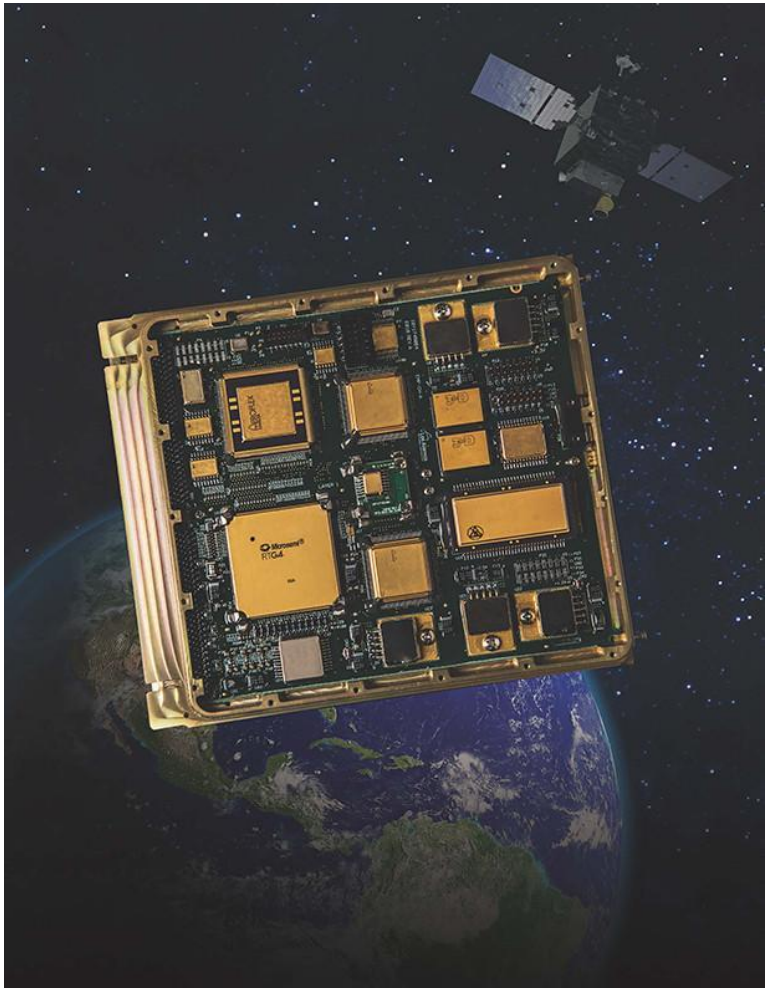
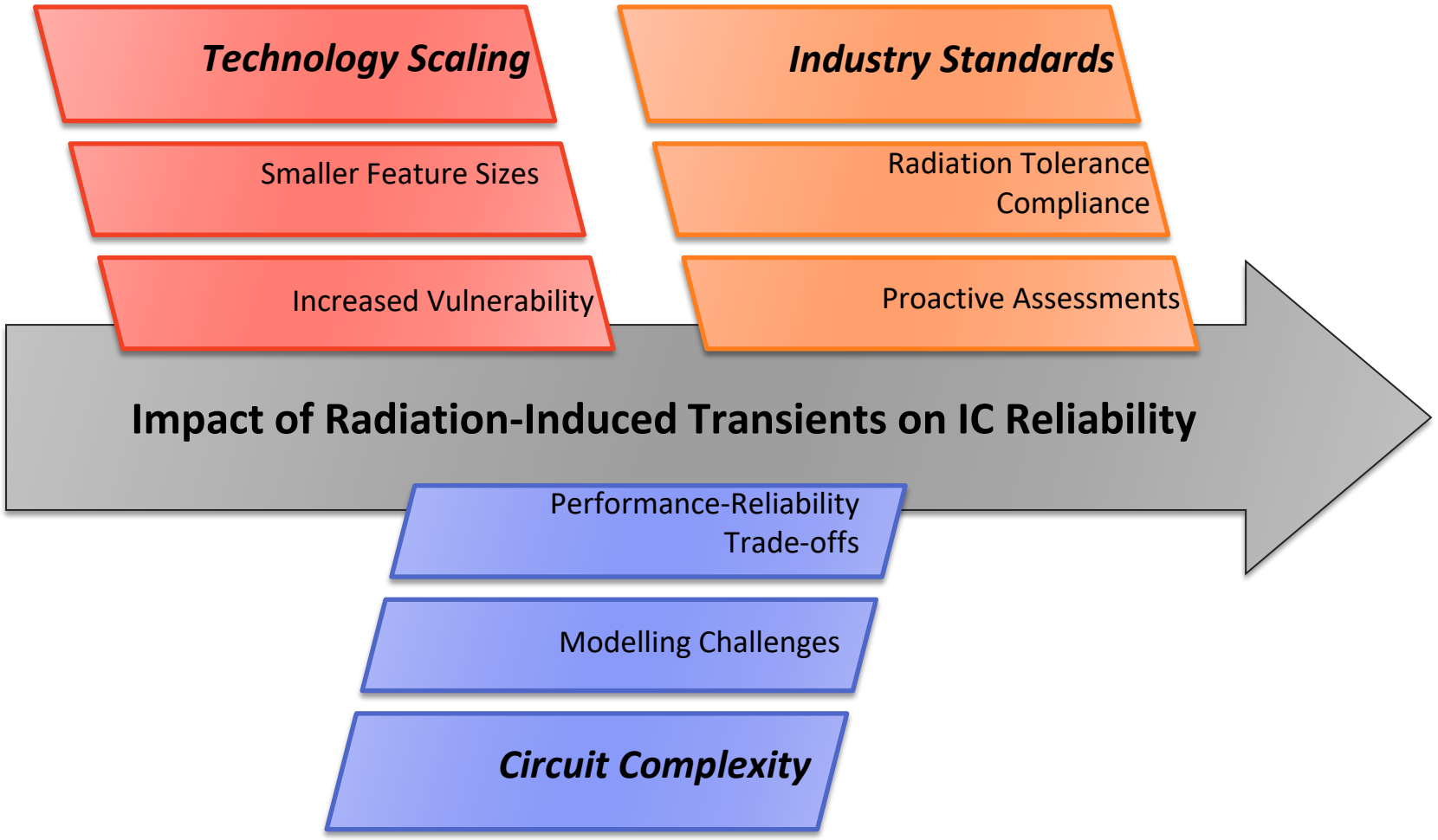
Outline

- **Introduction**
- Background & Motivation
- STA-based SET Analysis
- Sensitivity Metrics
- Integration into EDA Flows
- SET In-Place Optimisations (SIPO)
- Preliminary Results
- Future Directions
- DEMO
- Conclusions



Radiation-Induced Reliability Challenges in ICs



IC Vulnerability to Ionising Radiation

Space Applications

ICs used in space missions face high radiation exposure risks.

Medical Electronics

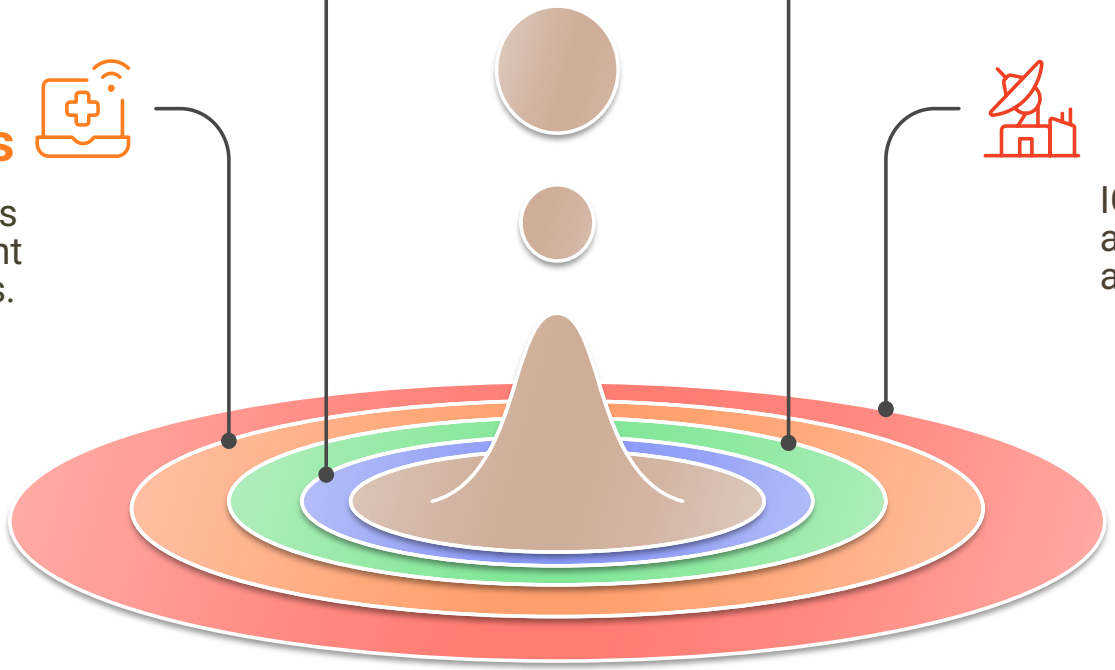
ICs in medical devices are essential for patient care and diagnostics.

Avionics

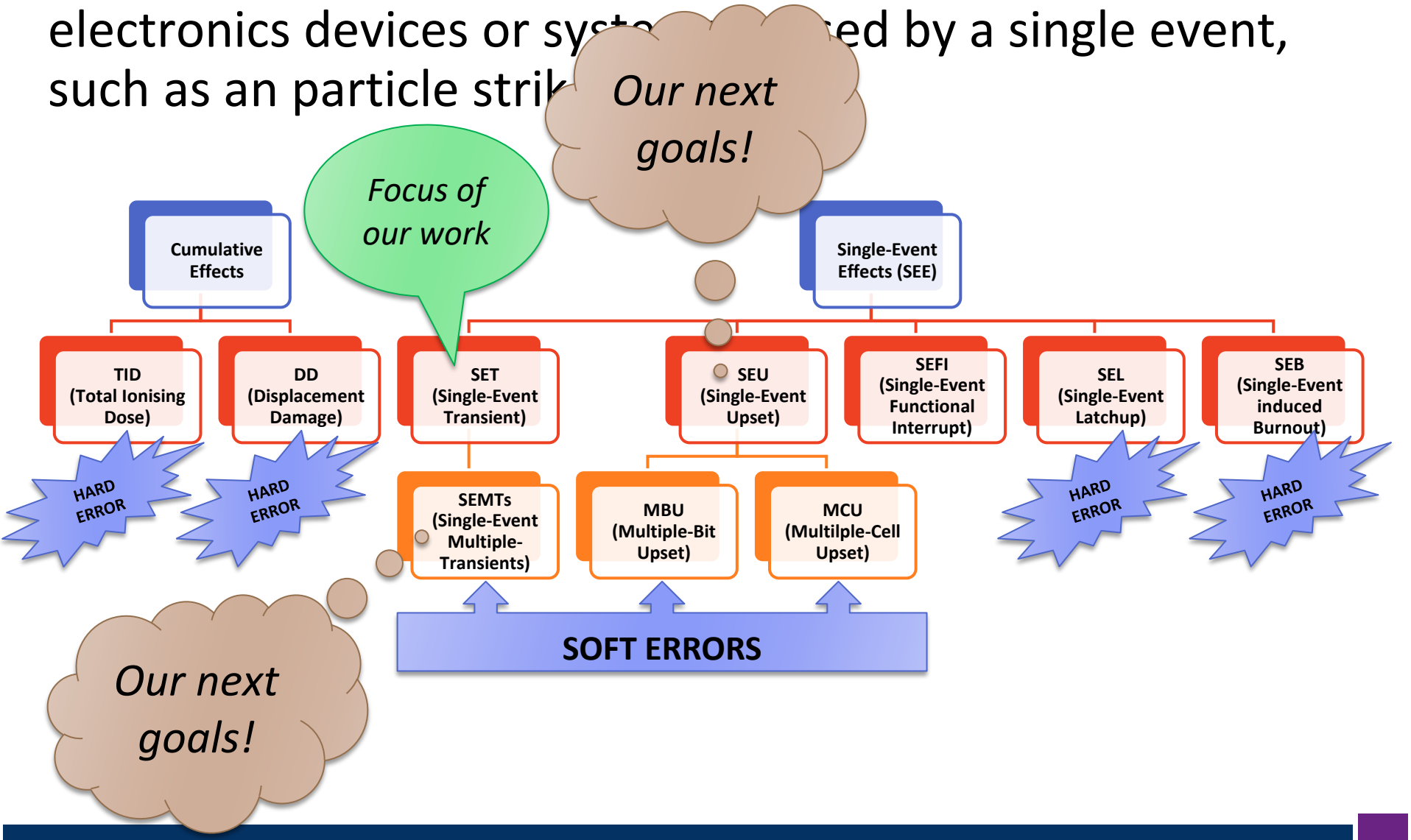
ICs in aircraft are critical for navigation and control systems.

Military Electronics

ICs in military systems are crucial for defense and communication.



Single Event Effects (SEEs) are upsets occurring in electronics devices or syste ed by a single event, such as an particle strik



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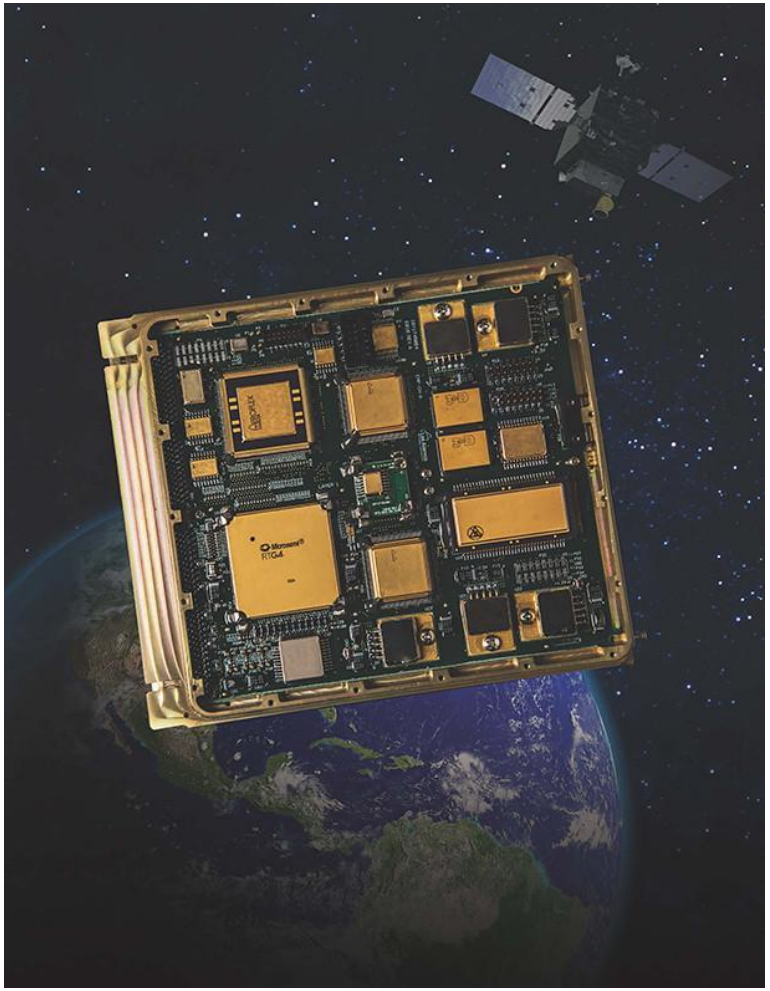
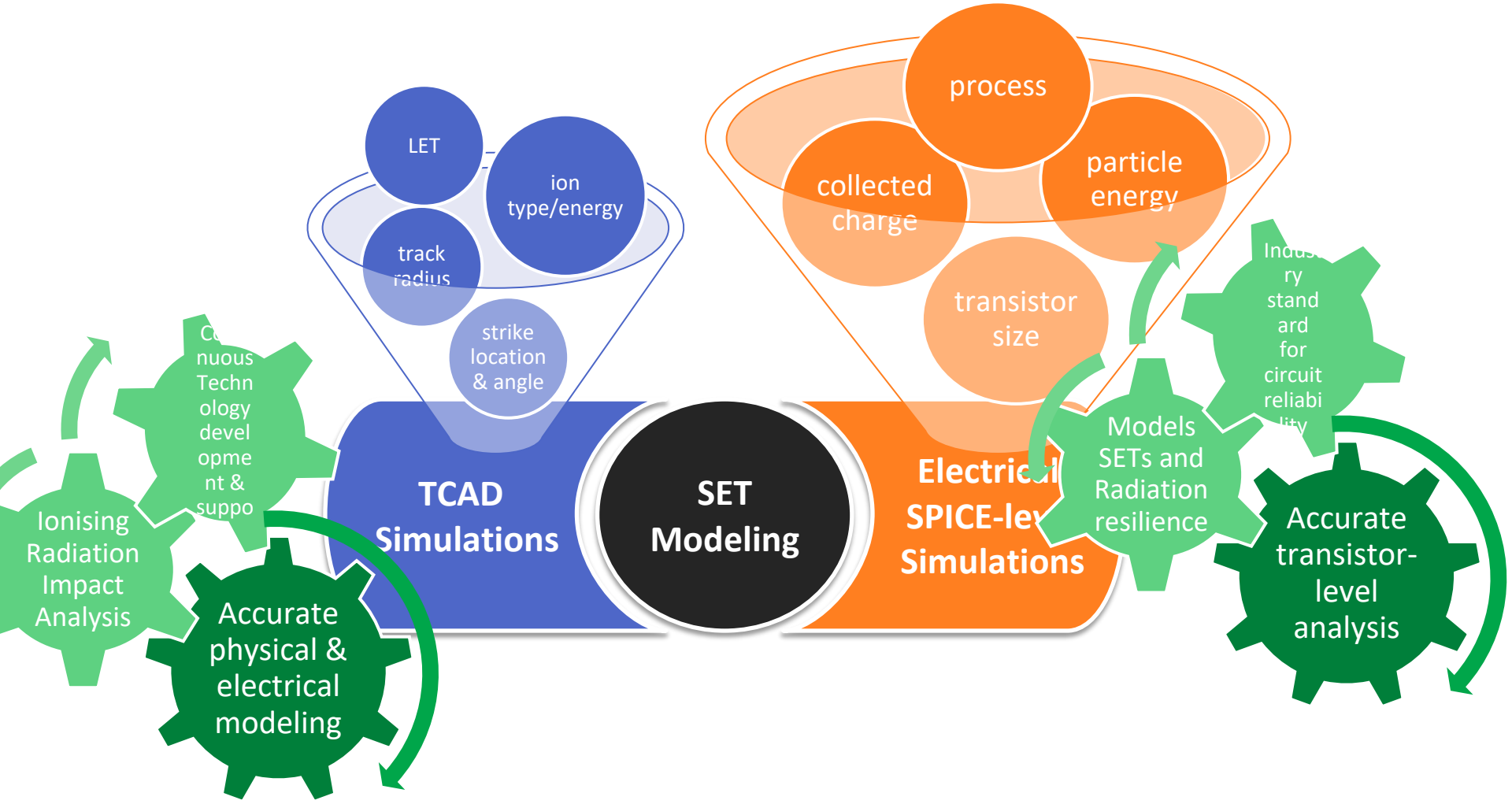
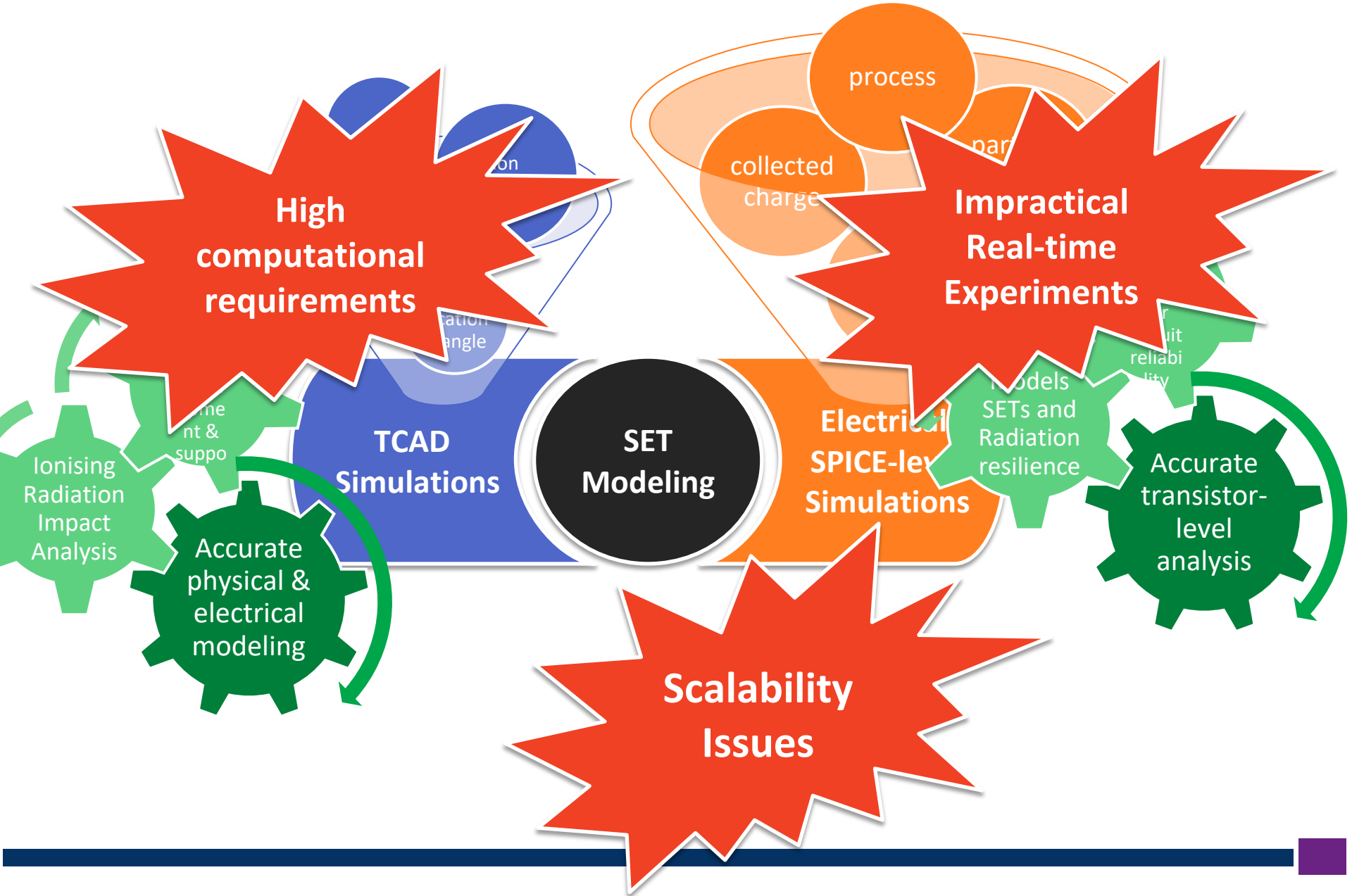


Single Event Transient Analysis



Single Event Transient Analysis



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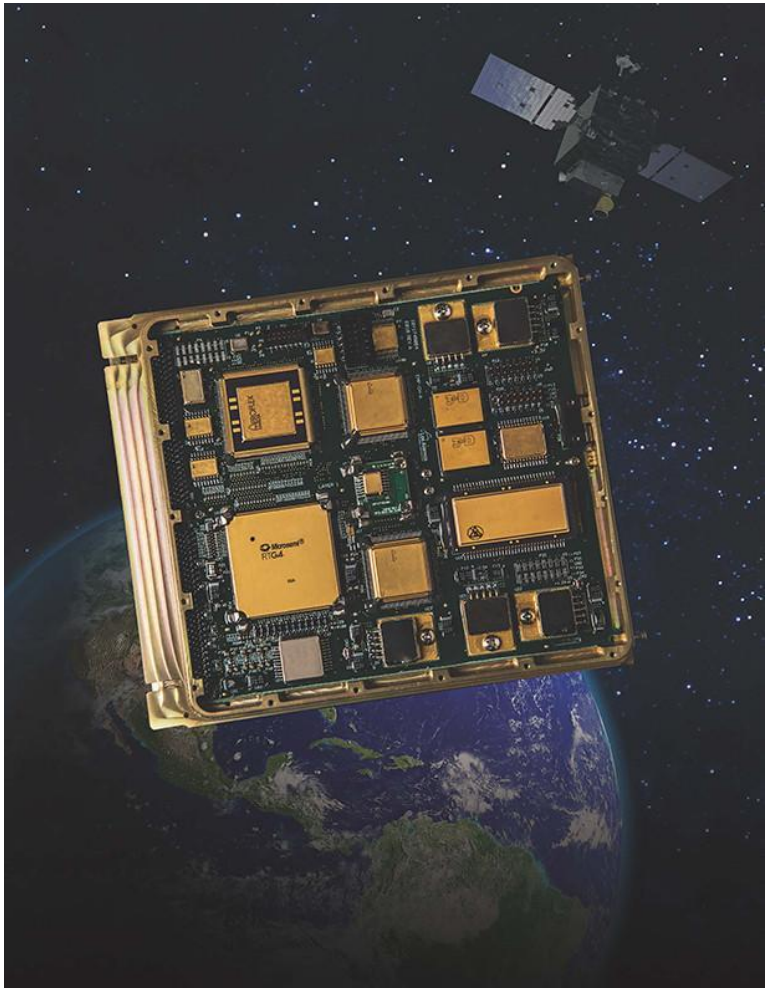
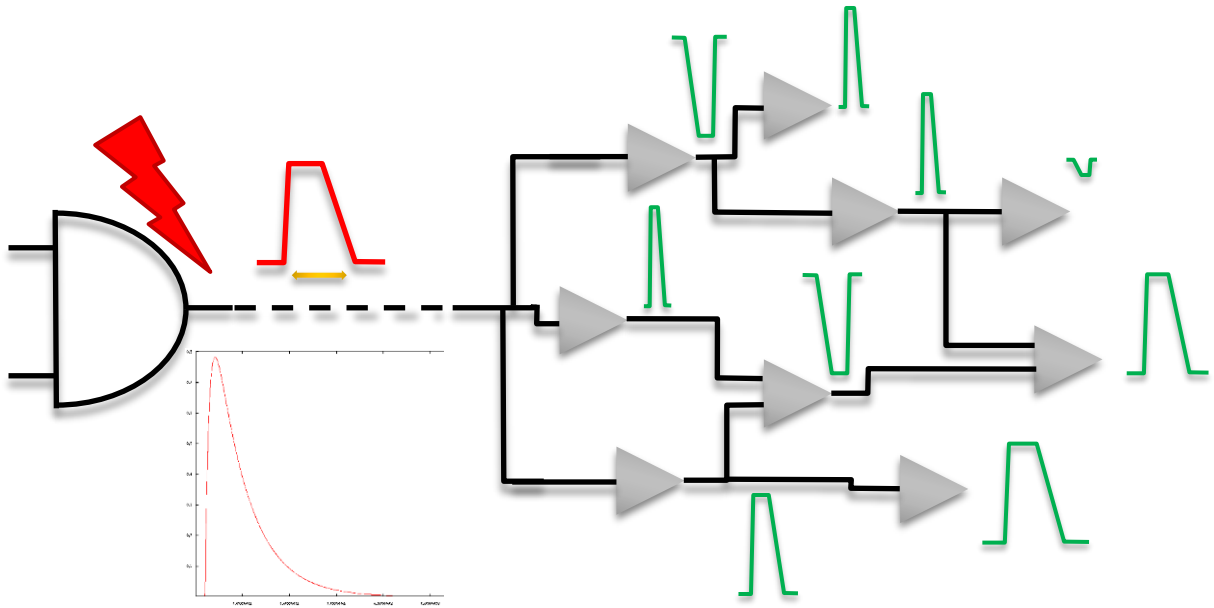


Problem Formulation

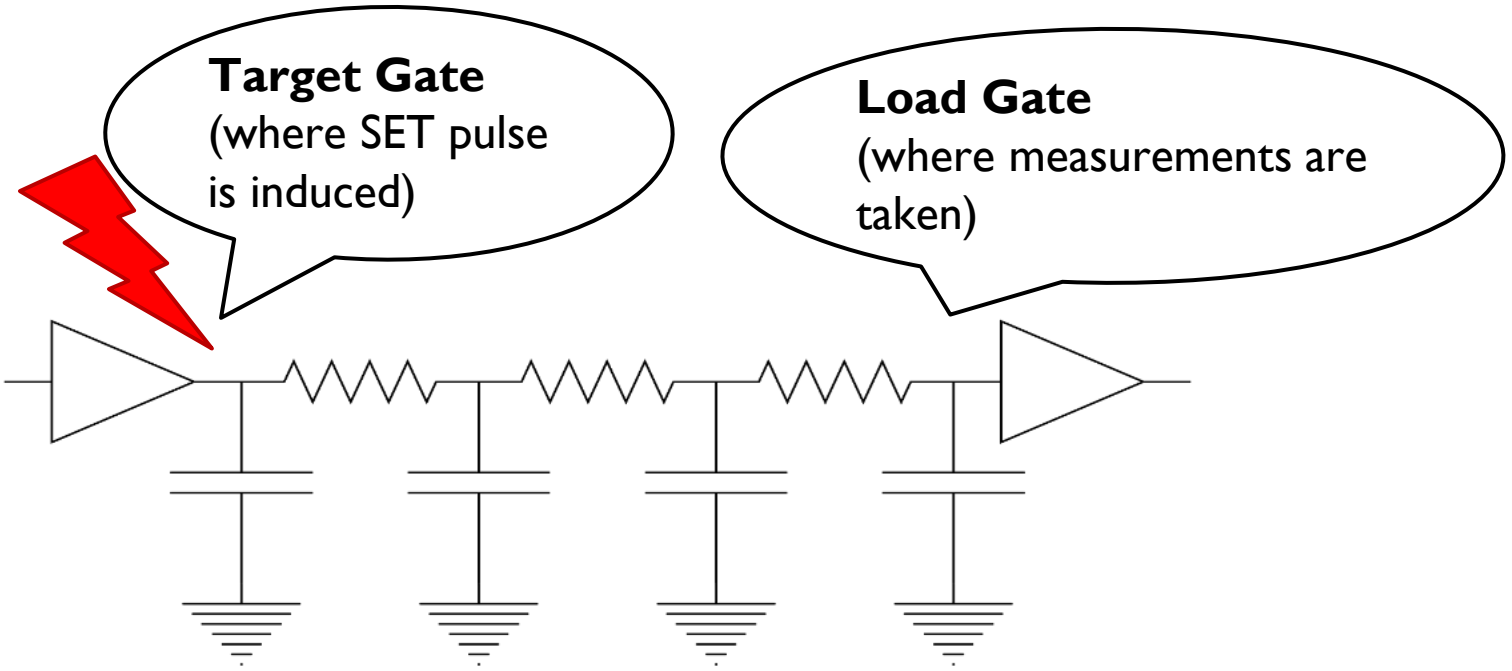
- A particle strike might strike a gate and generate a SET pulse.
- The generated SET pulse at the output of the struck gate is then propagated to the forward logic cone.
- UPSET supports both SET Generation & STA-based SET Propagation.



UPSET SET Generation

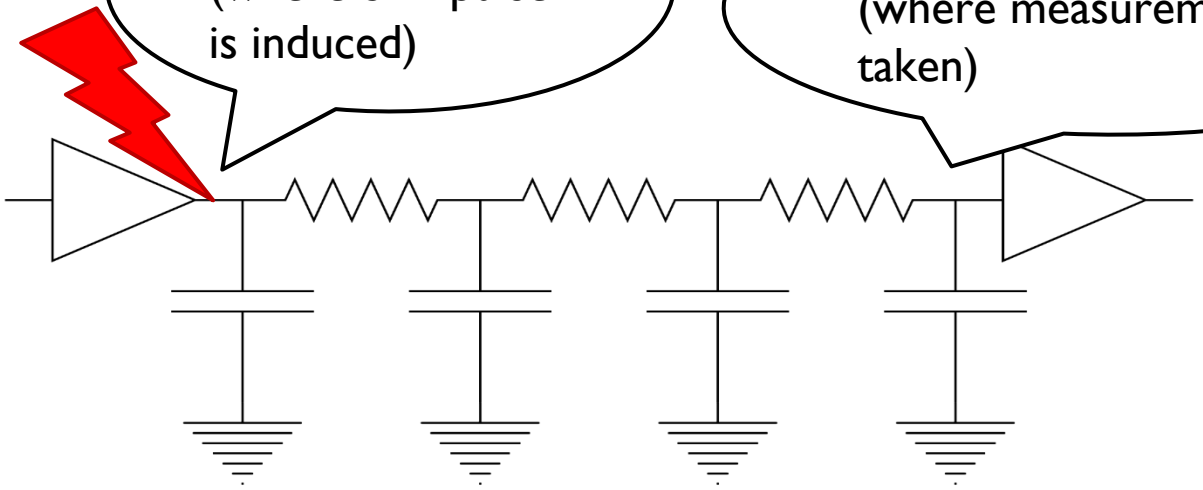
Modeling of Particle Strike & Generation at the target gate

- SET Generation at the strike point
  - Use of the equivalent analog circuit for the affected gate and its successors
  - Perform custom simulation for this subcircuit.

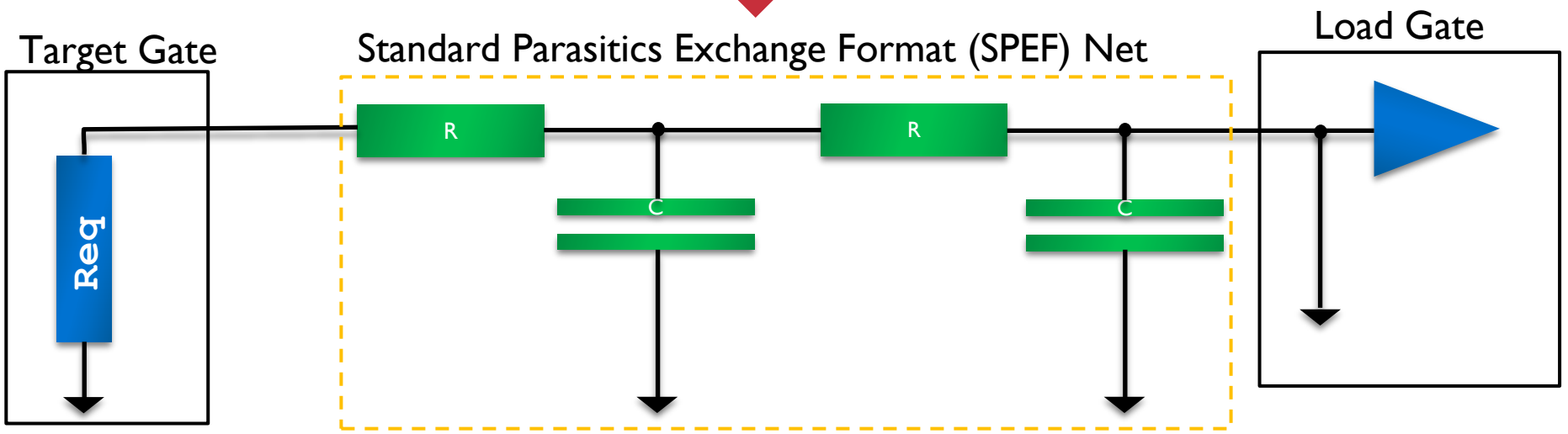


Target Gate
(where SET pulse is induced)

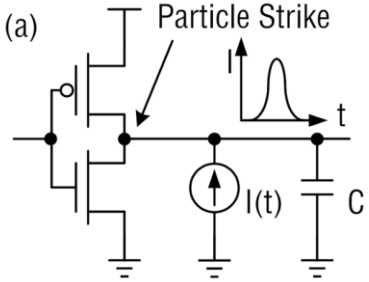
Load Gate
(where measurements are taken)

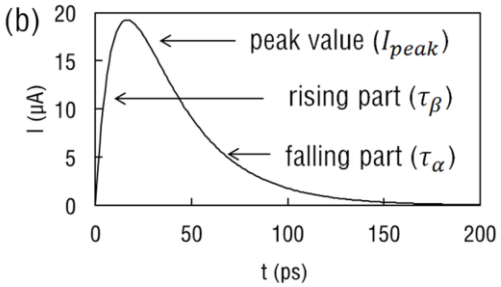


Equivalent Analog Circuit



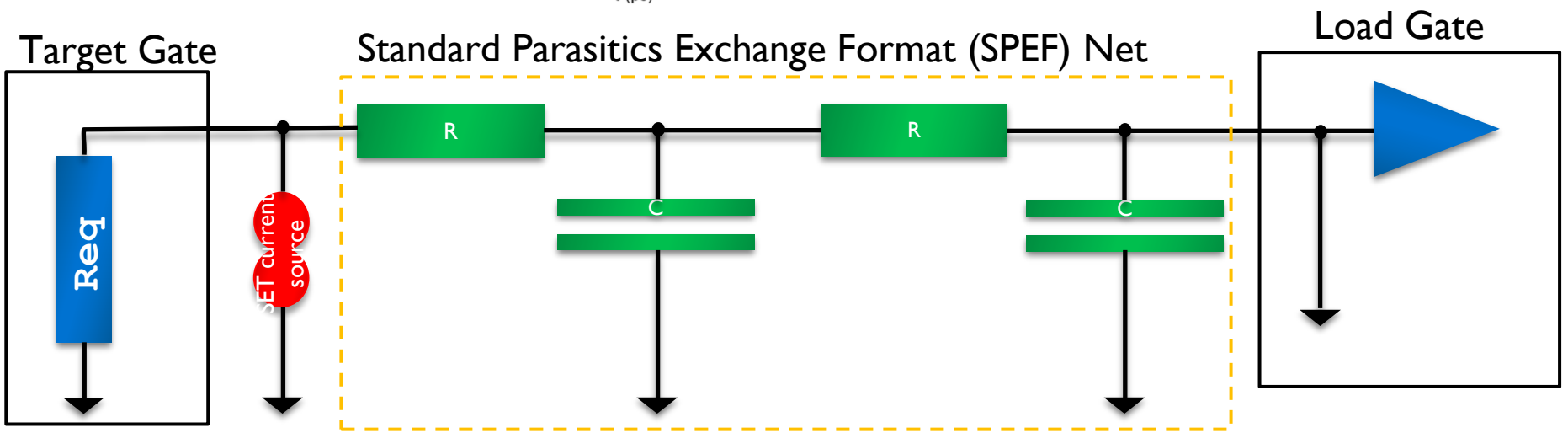
- The particle strike is described by a current source connected to the output of the target gate
  - UPSET in its current version supports the widely used **Double Exponential (DEXP) Current Source Model**





$$I(t) = I_{peak} \cdot (e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}})$$

$$I_{peak} = \frac{Q}{\tau_\alpha - \tau_\beta} \quad \tau_\alpha = \frac{k\epsilon_0}{\mu q N D}$$

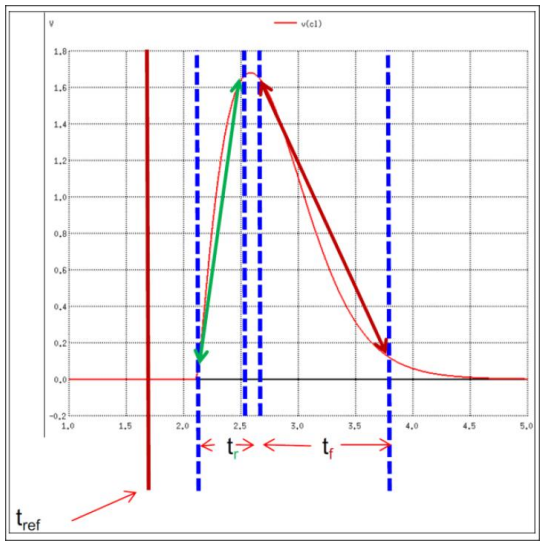


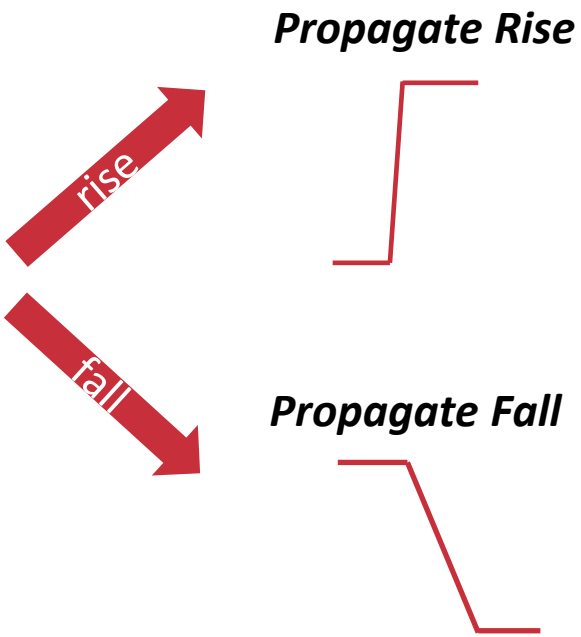
UPSET SET Propagation

STA-based SET Propagation

STA-based SET Propagation

- The generated SET pulse is propagated to the forward logic cone
- The SET pulse can be decomposed to a rise and fall edge

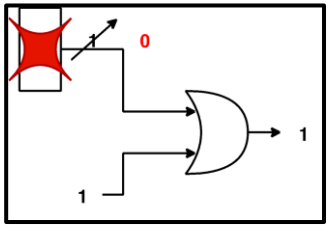




- STA can be used to propagate each edge separately
  - each edge is described by its arrival time and slew

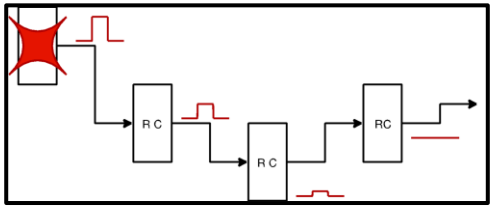
STA-based SET Propagation | Masking Mechanisms

- The propagation of a SET to the forward logic cone depends on the effects of the three masking mechanisms
  - **logical masking**
  - **electrical masking**
  - **timing-window masking**



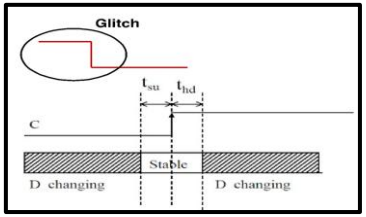
Logical Masking

Fault masked by a side-input being at gate's controlling value



Electrical Masking

Fault masked due to parasitic capacitance and resistance of the subsequent gates and wires



Timing-window Masking

Fault masked due to its arrival outside the [SETUP, HOLD] window, when FF captures the data

Logical Masking & Circuit State Definition

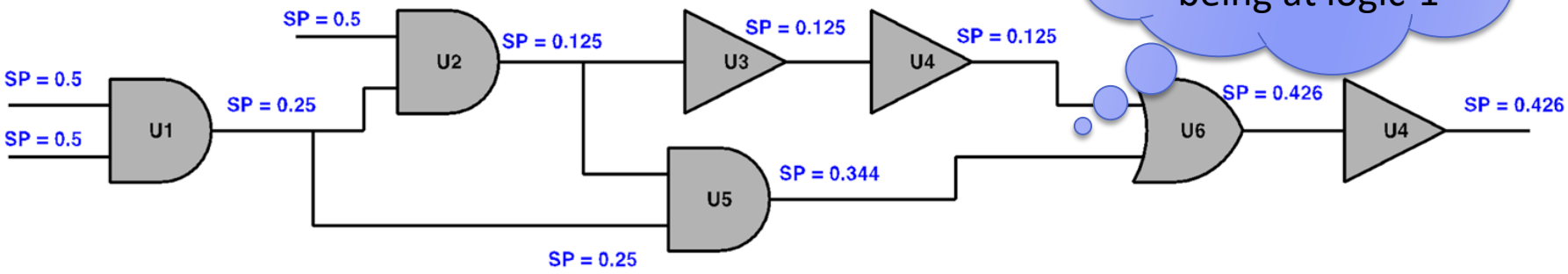
- Vector-based SET Analysis
  - The traditional methodology for specifying the current state of the circuit is by setting values to the circuit gatepins.
  - Accurate **BUT** it requires the evaluation of all the input vectors
    - increase in analysis runtime
- Probabilistic SET Analysis
  - The user can specify the current circuit state by annotating the average circuit behaviour, assigning a static probability to each gate pin.
  - Either SAIF or TCL commands
    - The user can also annotate the static probabilities for the circuit starting points and let UPSET annotate the rest of the circuit.

Logic Gate	Probability Equation
AND2	$P_{out=1} = P_{a=1} * P_{b=1}$
OR2	$P_{out=1} = P_{a=1} + P_{a=0} * P_{b=1}$
NAND2	$P_{out=1} = P_{a=0} + P_{a=1} * P_{b=0}$
NOR2	$P_{out=1} = P_{a=0} * P_{b=0}$
XOR2	$P_{out=1} = (P_{a=0} * P_{b=1}) + (P_{a=1} * P_{b=0})$
XNOR2	$P_{out=1} = (P_{a=0} * P_{b=0}) + (P_{a=1} * P_{b=1})$
INV	$P_{out=1} = P_{a=0}$
BUF	$P_{out=1} = P_{a=1}$

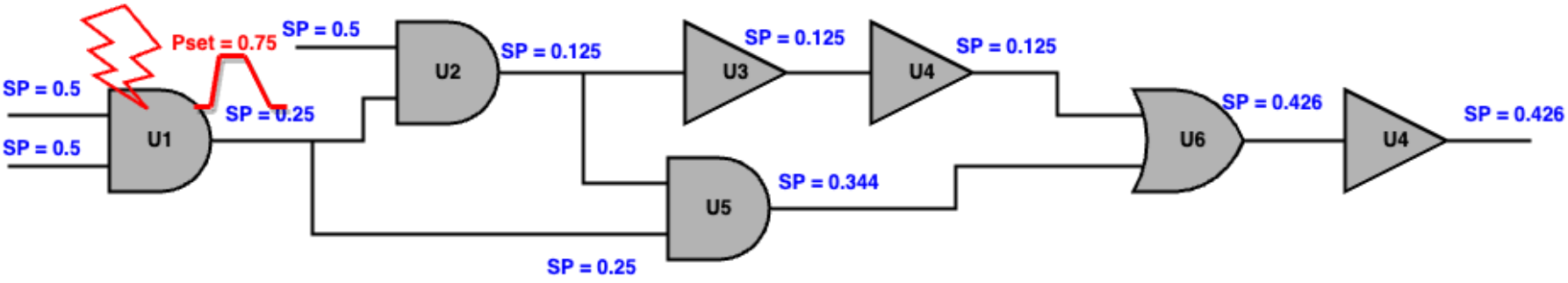
Probabilistic SET Analysis: Example Ci

SP indicates the static probability of the gatepin being at logic-1

- Example Circuit:

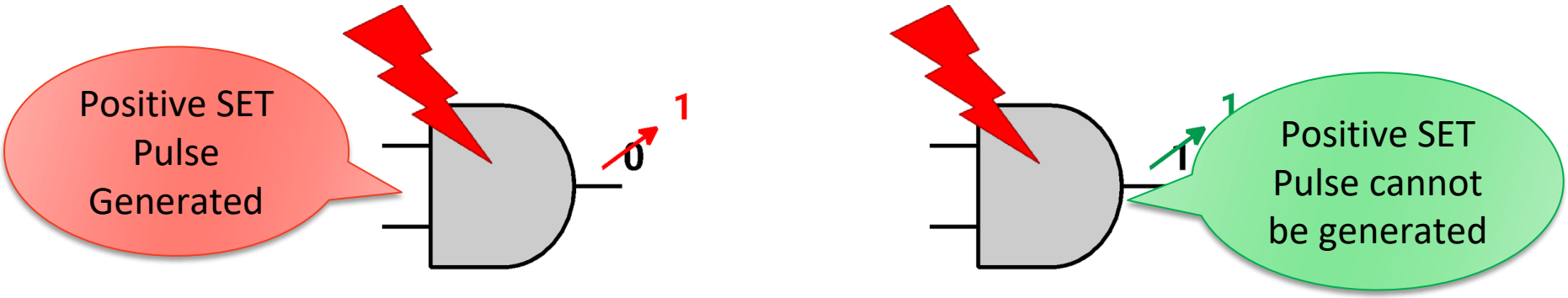


- A particle strikes gate U1, and a positive SET pulse is produced at the output

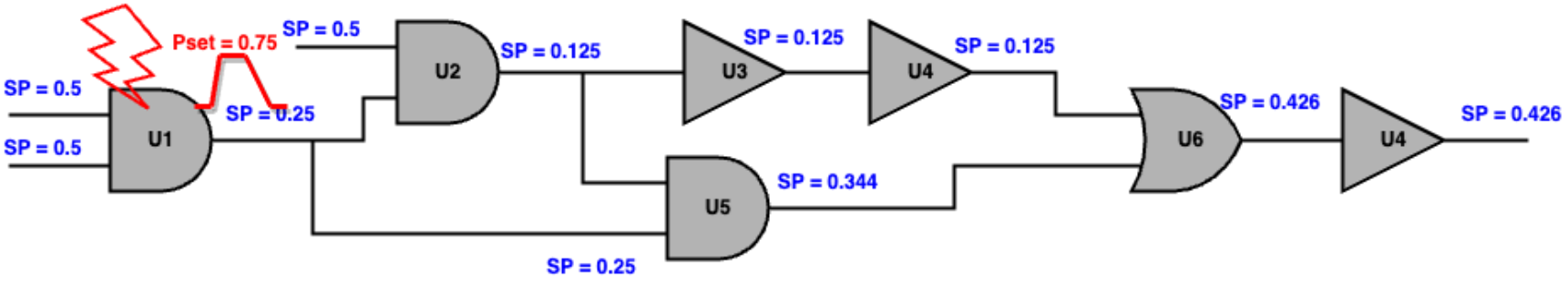


Probabilistic SET Analysis: *Initial SET Probability after strike*

- Generating a SET pulse requires the target gate to be at the appropriate logic state

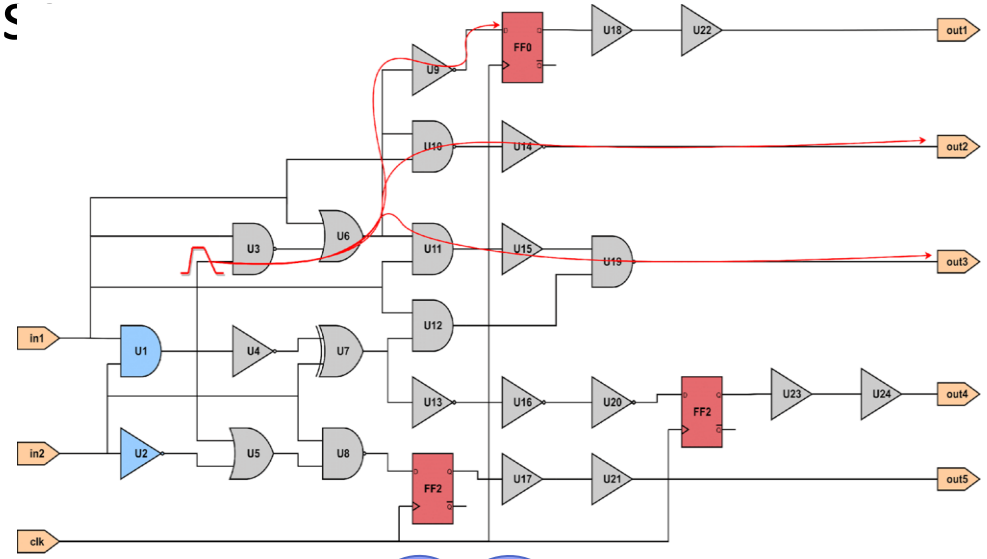


- So, the initial SET probability:
  - $P_{SET}^{init}(G_i) = \begin{cases} P_0(G_i), & positive\ SET\ pulse\ generation \\ P_1(G_i), & negative\ SET\ pulse\ generation \end{cases}$



Probabilistic SET Propagation

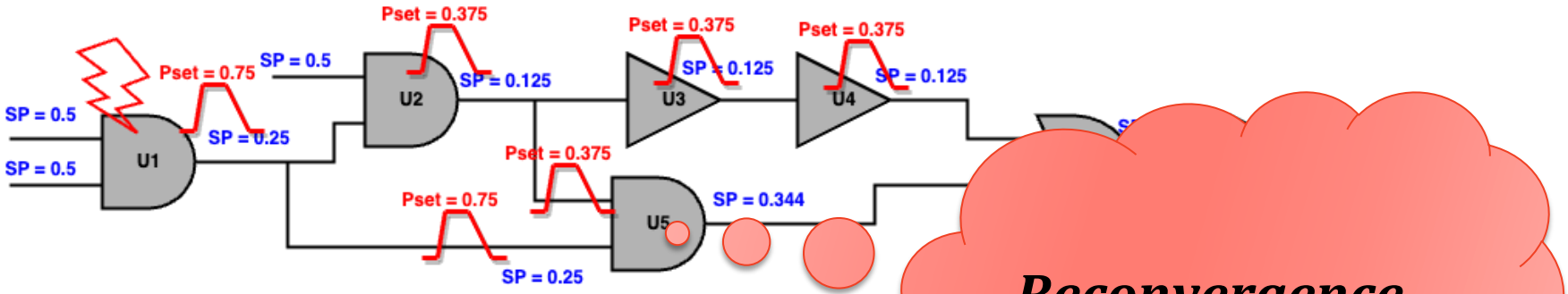
- A SET probability is computed along the propagation of the SET puls to the forward logic cone
  - Indicates the probability of the SET reaching a gatepin
- 2 supported SET Propagation modes:
  - **“Vanilla” STA-mode**
  - **TimeStamp-based STA-mode**



they differ only in case of reconvergence

Probabilistic SET Propagation: *Non-Reconvergence*

- The computation of the SET probability at the output of a gate considers:
  - The probability of the input SET, and
  - The static probabilities of all side input combinations, allowing the propagation of the SET pulse through the gate.



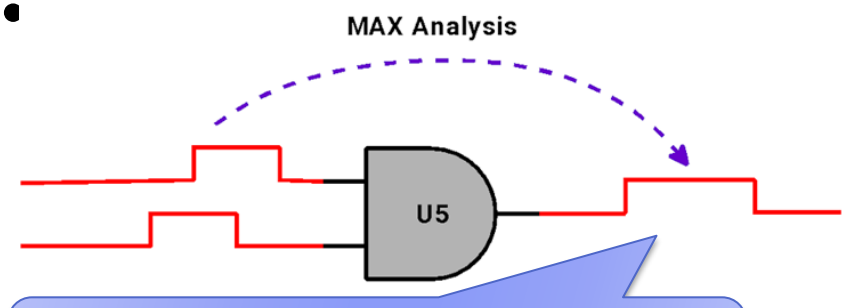
- For the example:
  - SET reaches U2 (AND):
    - $P_{SET}(U2) = P_{SET}(U2|B) \times SP(U2|A) = 0.75 \times 0.$ [illegible] 375
  - SET reaches U3 and U4 (BUFs):
    - $P_{SET}(U3) = 0.375$ & $P_{SET}(U4) = 0.375$

no side inputs

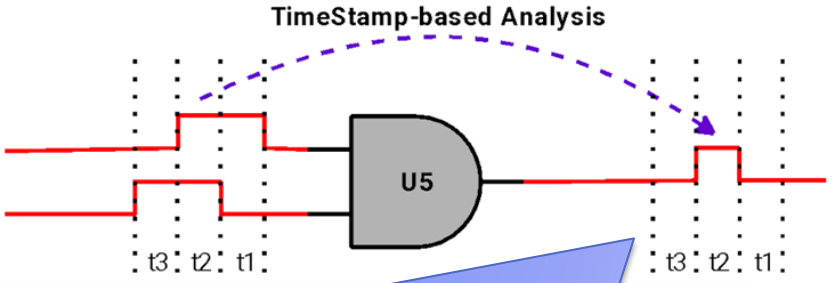
Probabilistic SET Propagation : *Reconvergence*

- The difference between the 2 supported SET propagation modes lies in the handling of the

SET Propagation Modes	Reconvergence Handling
"Vanilla" STA-mode	MAX Analysis considering each input SET pulse separately
TimeStamp-based STA-mode	TimeStamp-based Analysis considering the arrival times of the input SET pulses and the Boolean function of the examining gate



[earliest rise edge, latest fall edge]



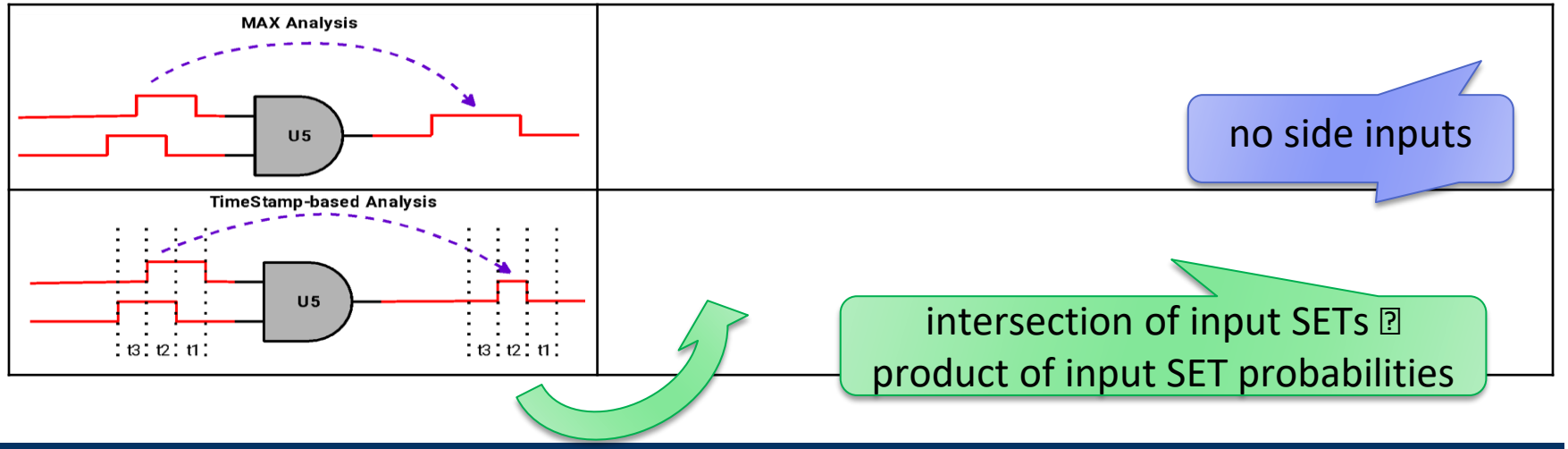
Boolean evaluation @ U5 considering the arrival times of the input SET pulses ⍰ output SET is the intersection of the input SET pulses

Probabilistic SET Propagation: *Reconvergence*

- Similar to the SET pulse shape, the SET probability computation differs based on the propagation mode:

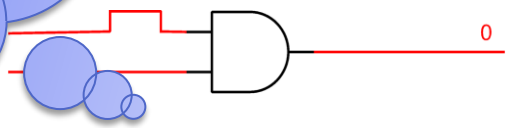
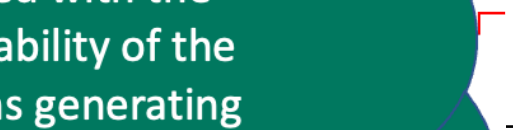
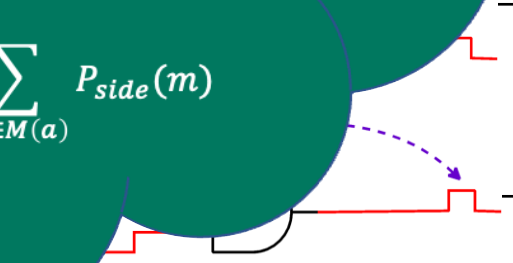
SET Propagation Mode	SET Probability Computation
”Vanilla” STA-mode	
TimeStamp-based STA-mode	It depends on the arrival times of the input SET pulses and the Boolean function of the examining gate.

- For the example circuit:



Probabilistic SET Propagation: Reconvergence

probabilities annotation does not consider signal correlations due to reconvergence

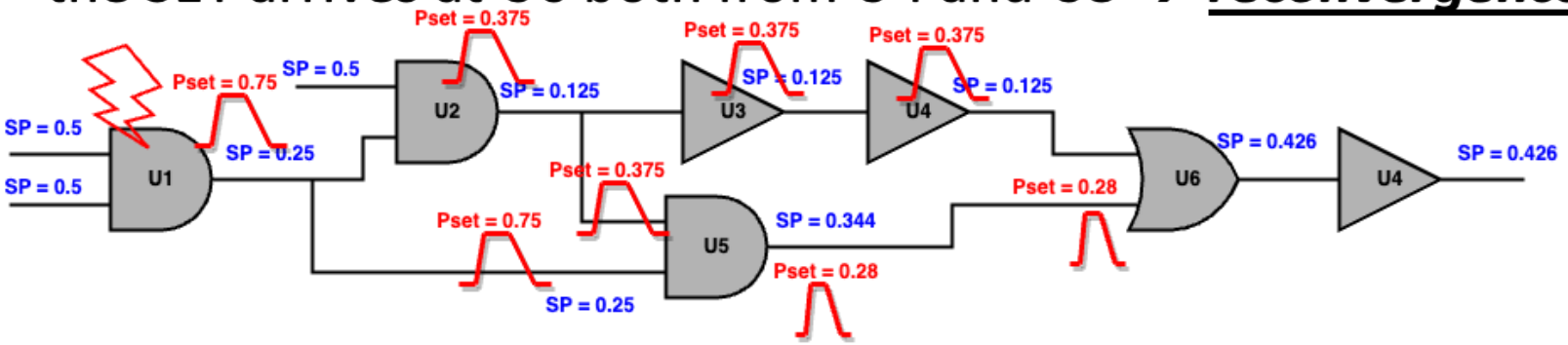
	Example	Probability
		
Intersection of Input Pulses		
U		
Prop / Other masked		

If side-inputs exist → these equation are expanded with the product with the probability of the side input combinations generating the pulse to the output (similar to "Vanilla" mode)

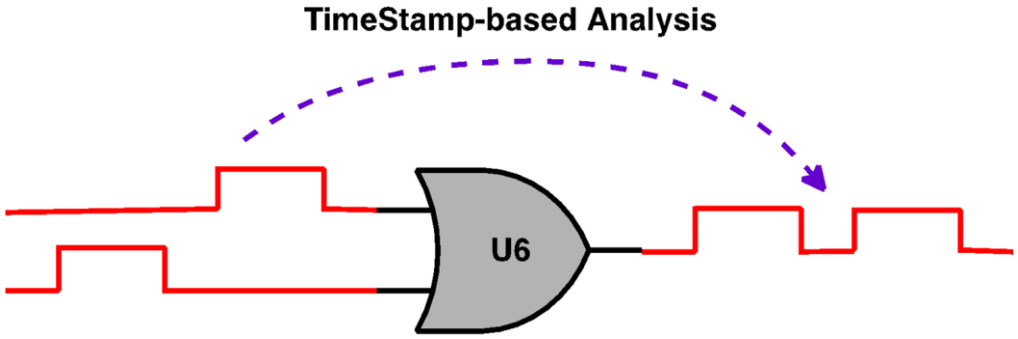
$$P_{SET}(out) = P_{SET}(a) \times \sum_{m \in M(a)} P_{side}(m)$$

Probabilistic SET Propagation: Reconvergence

- Continuing by propagating the SET pulse with the TimeStamp-based STA mode:
  - the SET arrives at U6 both from U4 and U5 → ***reconvergence***



  - The TimeStamp-based analysis will produce the following SET pulse train:
    - $P_{SET}(U6) = \max\{P_{SET}(U6|A), P_{SET}(U6|B)\} = 0.375$



UPSET *VS* SPICE

Comparative Study *VS* SPICE

Benchmark	PW @ endpoints (ns)		Runtime (s)	
	SPICE	UPSET	SPICE	UPSET
c17 single logic cone	0.344	0.389	3.230	<0.001
	0.393	0.464	3.230	<0.001
	0.429	0.514	3.220	<0.001
gate chain	0.505	0.613	3.320	<0.001
	0.556	0.594	2.500	<0.001
	0.587	0.605	3.690	<0.001
buffer chain x300 stages	5.180	4.765	632.000	0.050
	5.230	4.739	625.000	0.050
	5.264	7.752	616.000	0.050
SET filter	0.000	0.000	2.270	<0.001
	0.000	0.000	2.520	<0.001
	0.000	0.000	2.540	<0.001

significant source of error in STA engines

Significant source of error → extrapolations in the LUTs of the technology library during the delay annotation of the fall SET edge

~4.56% error

X25,222 times FASTER

Georgakidis, Christos, et al. "Towards a Comprehensive SET Analysis Flow for VLSI Circuits using Static Timing Analysis." *2023 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*. IEEE, 2023.

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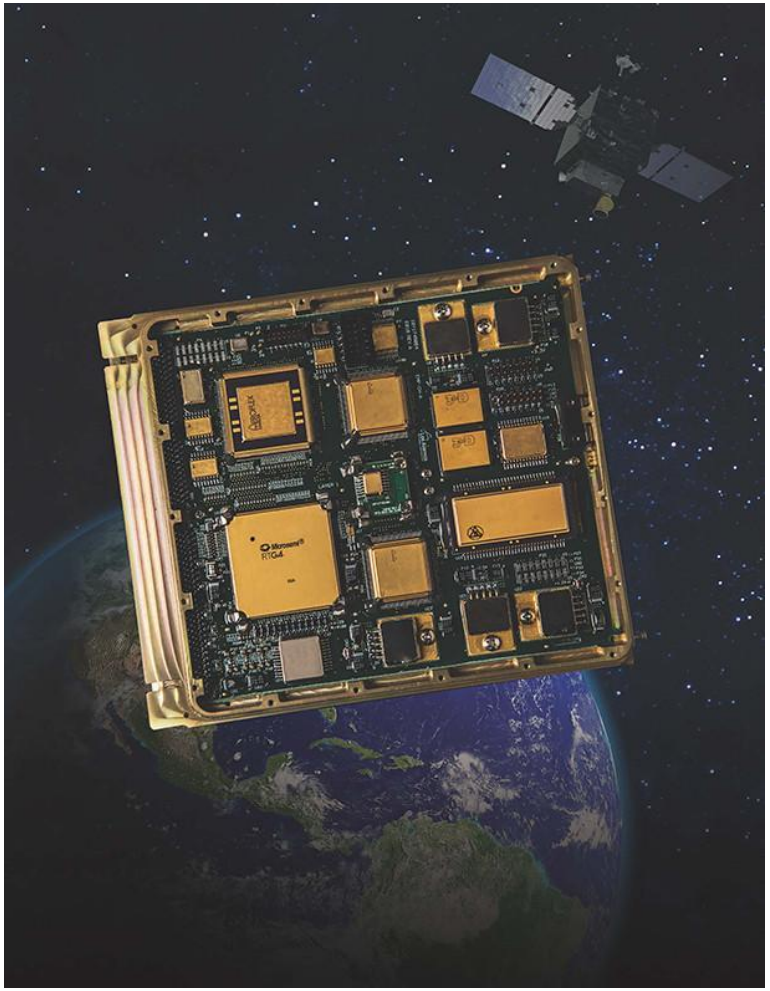

Circuit Sensitivity Metrics

- **Accumulated SETs ($ASET$)**
  - the number of SETs reaching and getting latched by each circuit endpoint
- **Accumulated Pulse Width (APW)**
  - the accumulation of the pulse widths of all the SET pulses reaching the circuit endpoints

Component Sensitivity Metrics

- **Impact Ratio (IR)**
  - the ratio of affected endpoint by a SET that produced at the output of a gate over the reachable endpoints
- **Maximum Pulse Width (MPW)**
  - the maximum pulse width of all SET pulses
- **Broadening Factor (BF)**
  - the ratio of the output to input pulse width for each SET pulse passing through a gate
- **SET Generation Probability (P_{gen})**
  - the probability of each gate being able to generate a SET pulse

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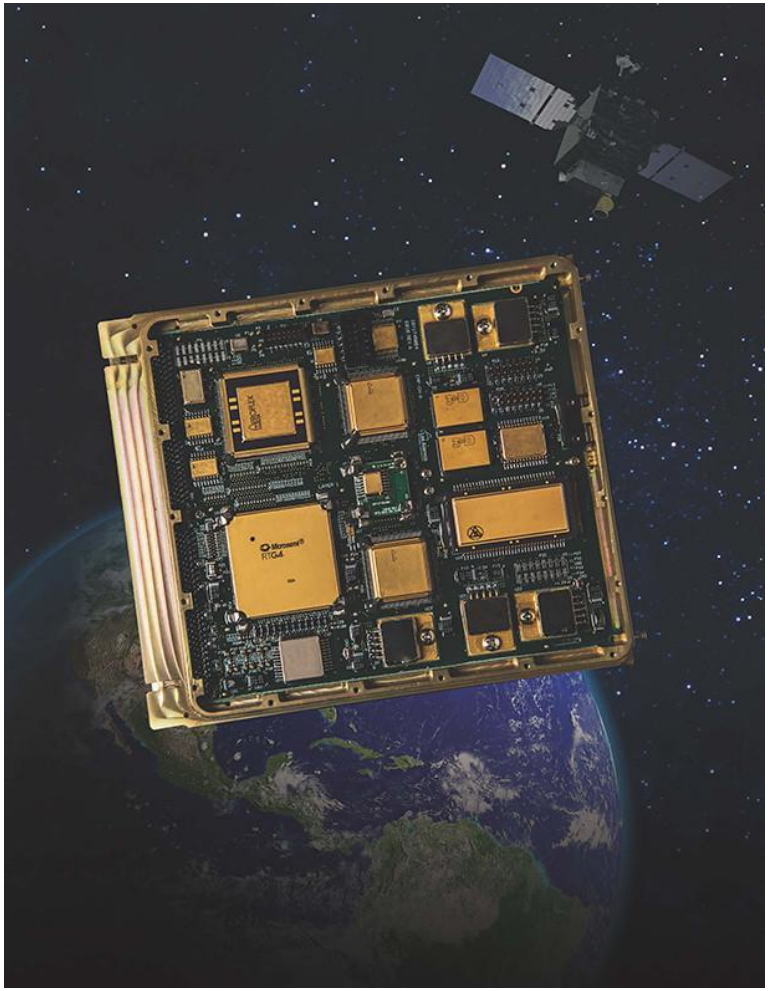
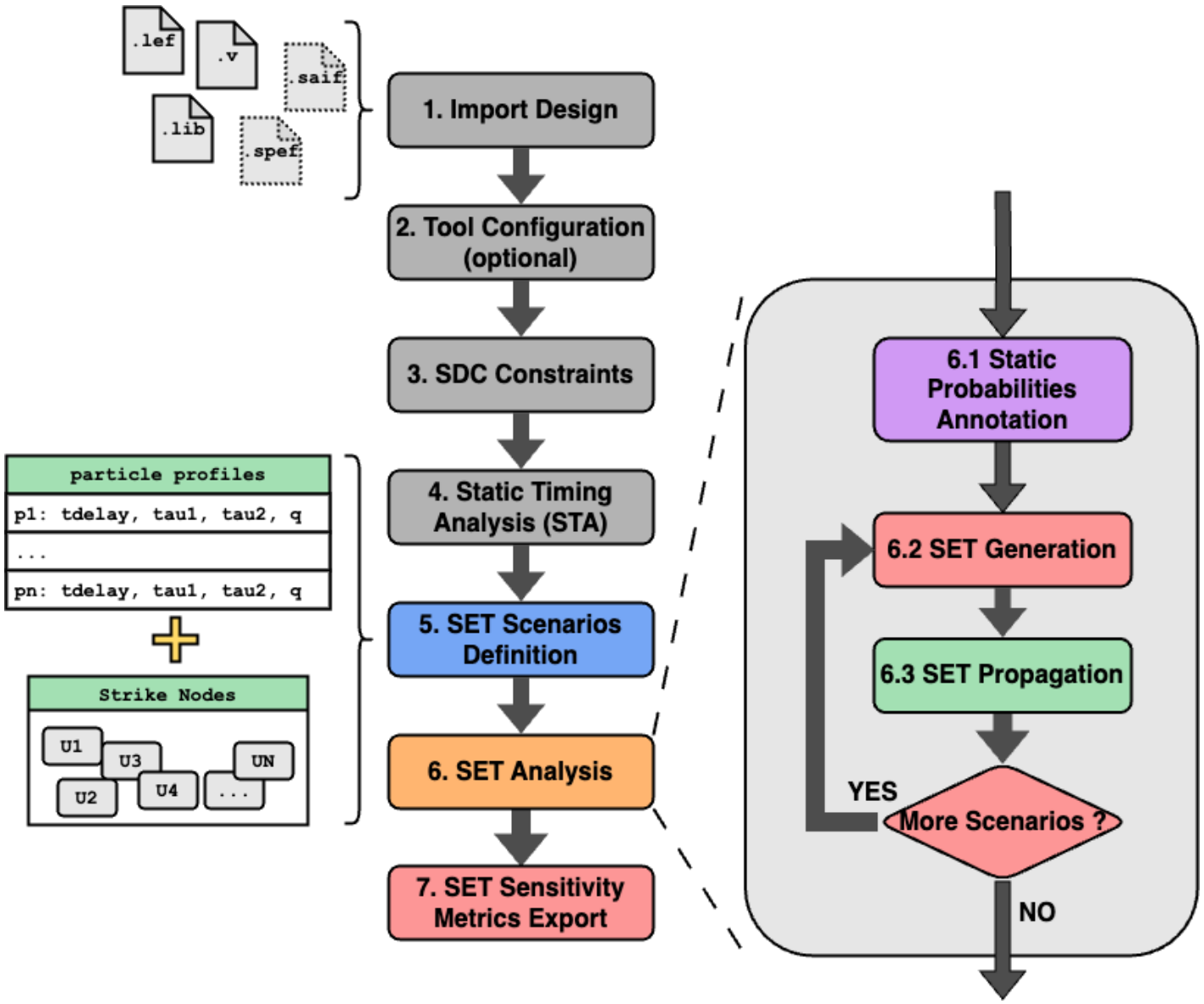
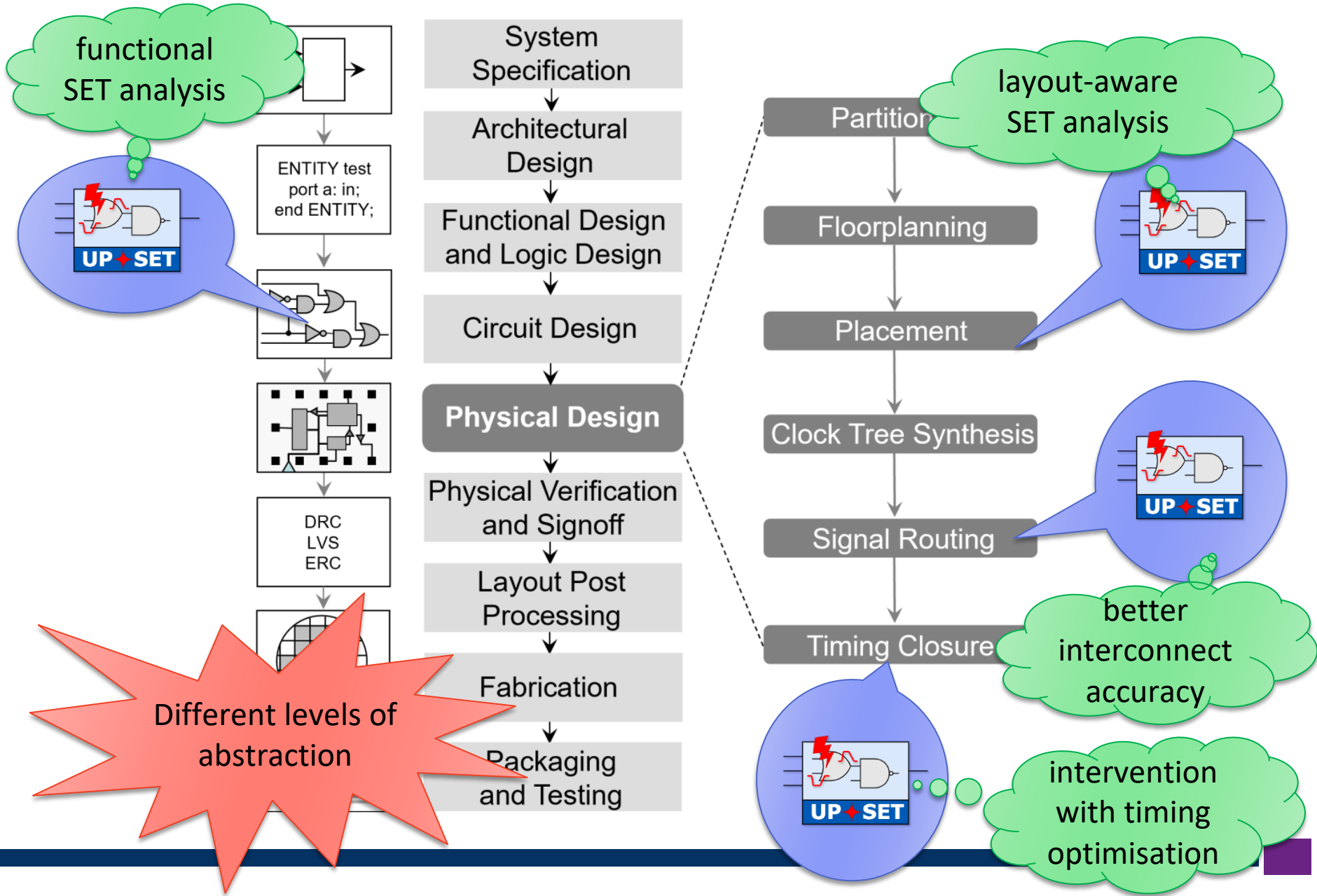


UPSET Top-Level Flow



UPSET Integration into the RTL-to-GDSII Flow



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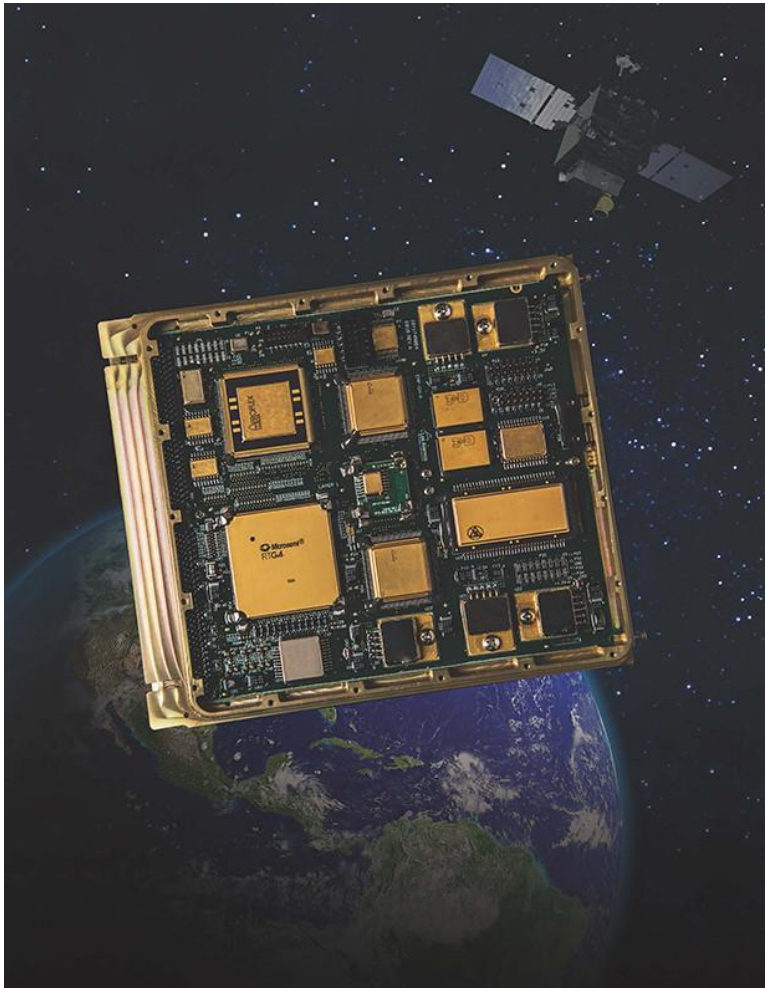
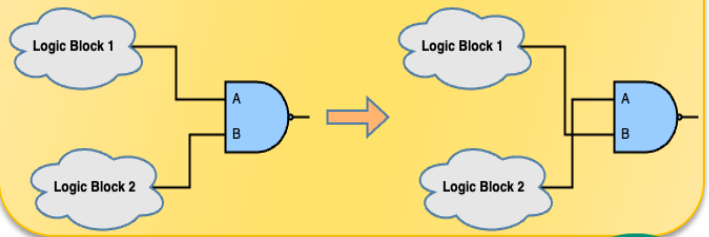
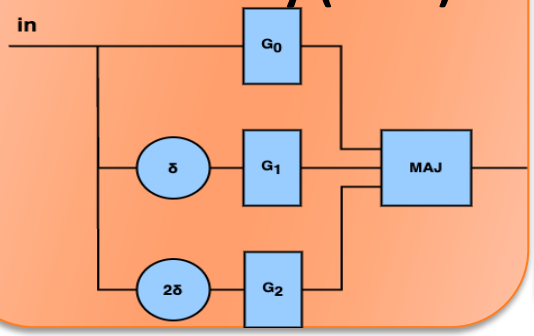


Common Gate-level SET Mitigation Techniques

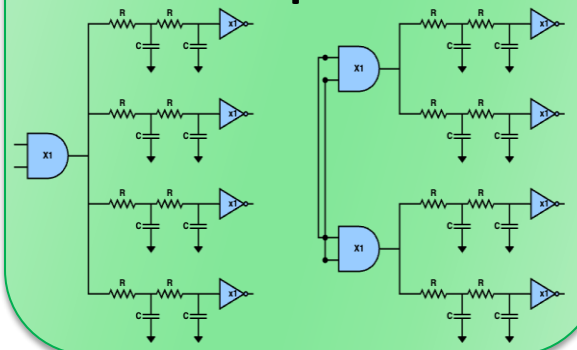
Pin Assignment / Rewiring



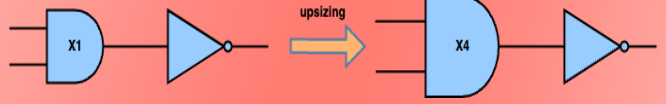
Triple Modular Redundancy (TMR)



Fan-out Decomposition

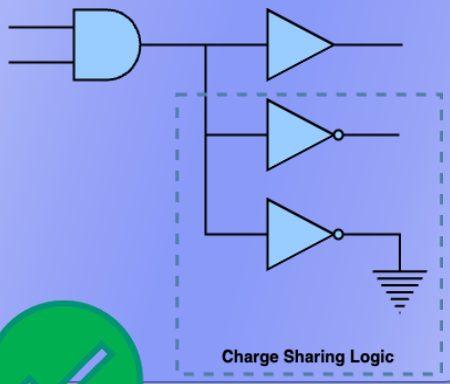


Gate Resizing

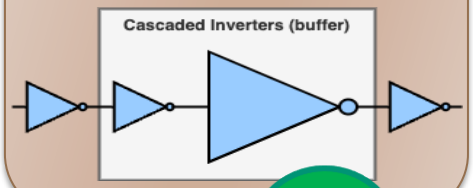


SET-driven Placement

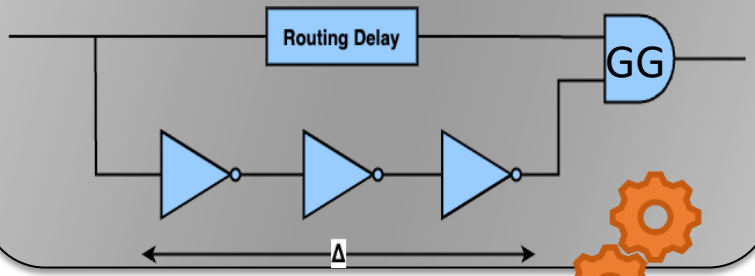
Charge-Sharing Logic



Cascaded Inverters



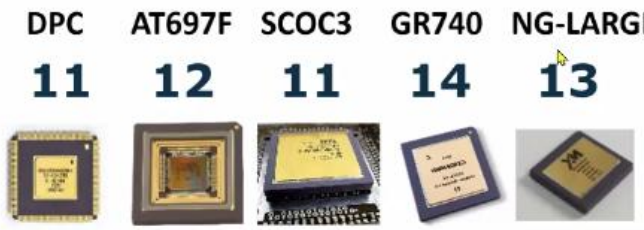
SET Filter Insertion



SET In-Place Optimisations: *Where is the catch?*

TOTAL number of mitigation techniques (on-chip) used per device

DPC	AT697F	SCOC3	GR740	NG-LARGE
11	12	11	14	13

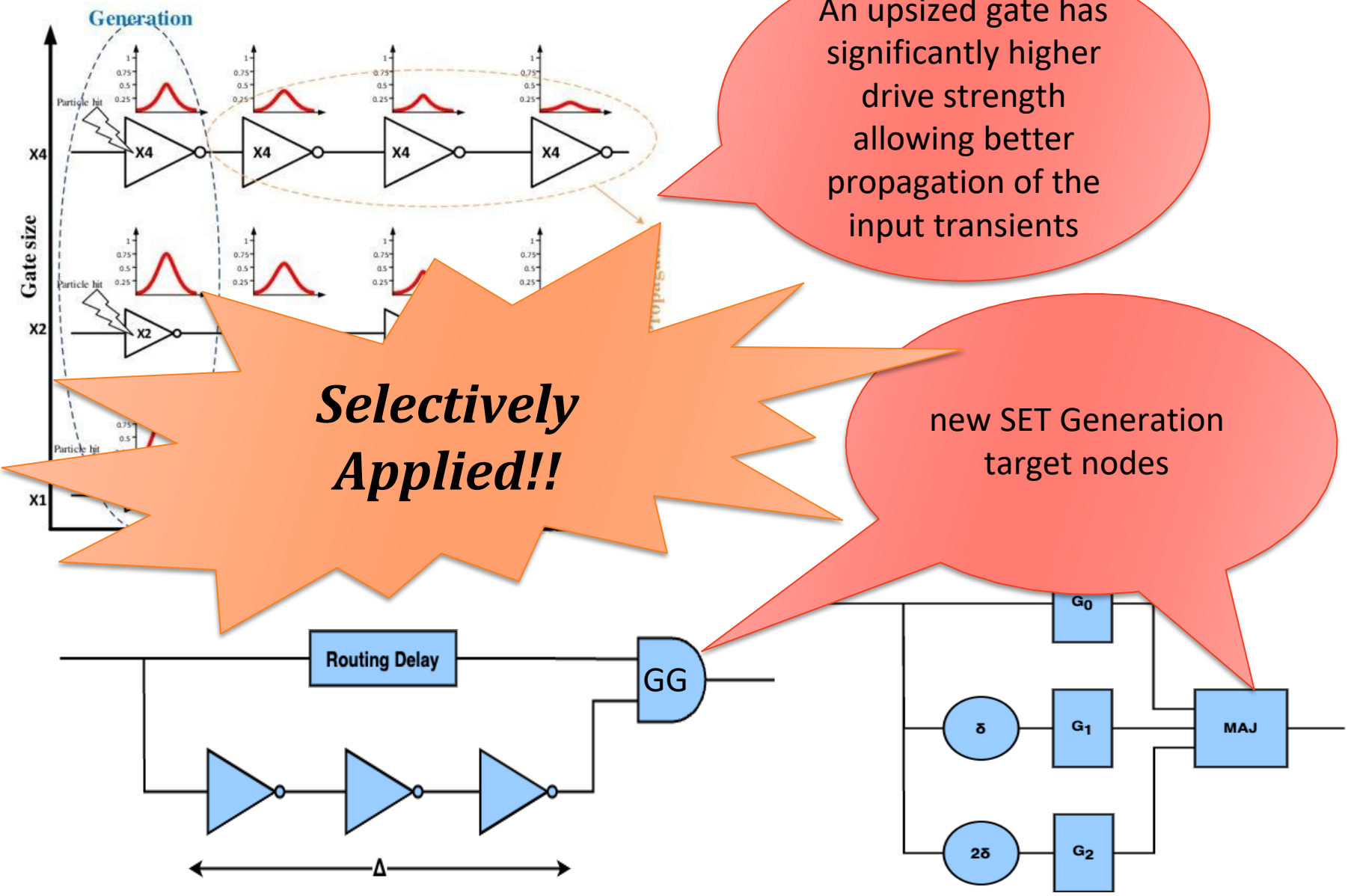


no universal recipe nor cookbook to guide you to decide which mitigation cocktail is best for your circuit

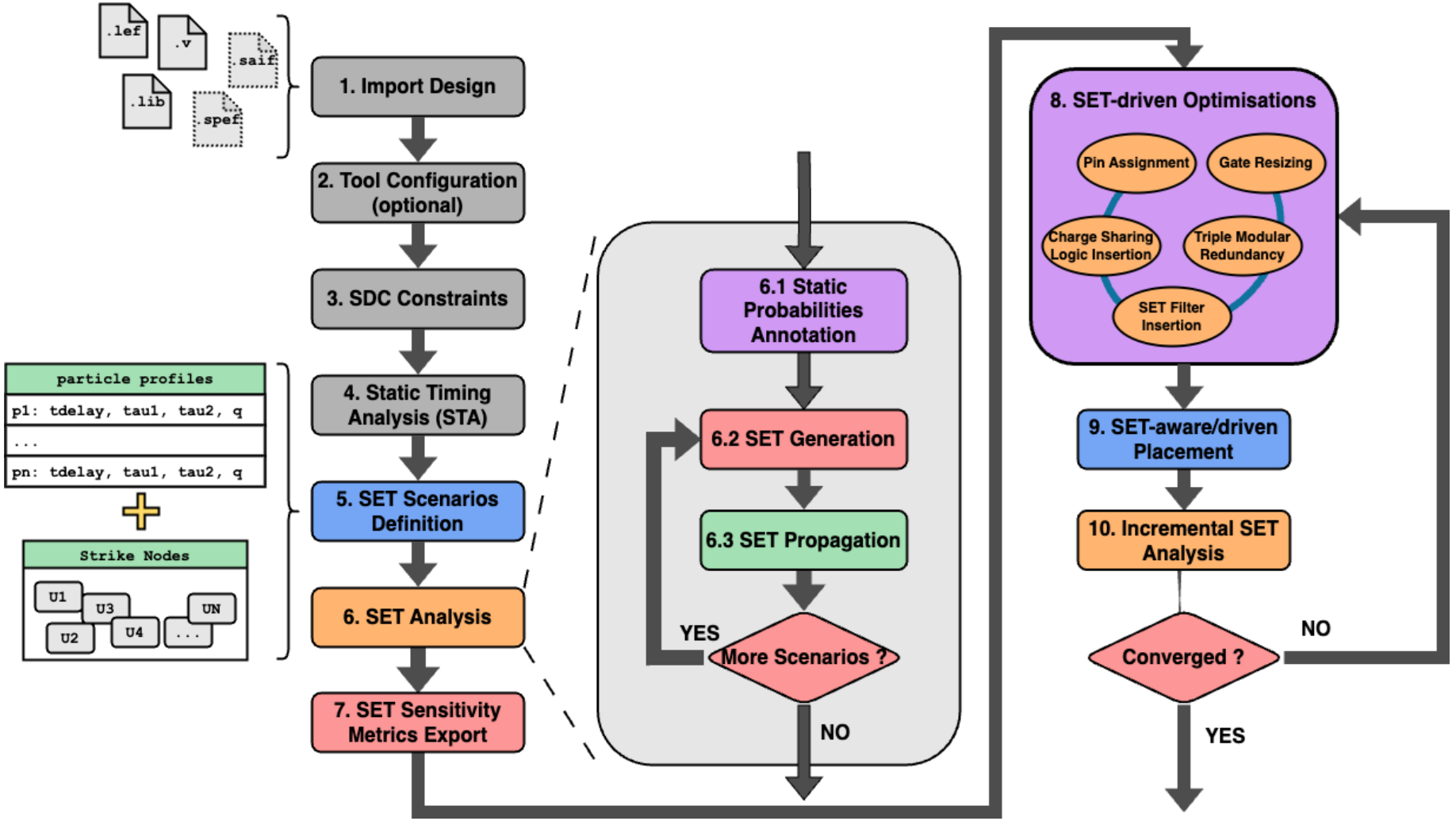
sometimes LESS can be BETTER: too many overlapping techniques may introduce additional or new unwanted radiation effects

source: ESA

SET In-Place Optimisations: *Where the catch?*



UPSET's 1st Closed-Optimisation Loop



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- Integration into EDA Flows
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- DEMO
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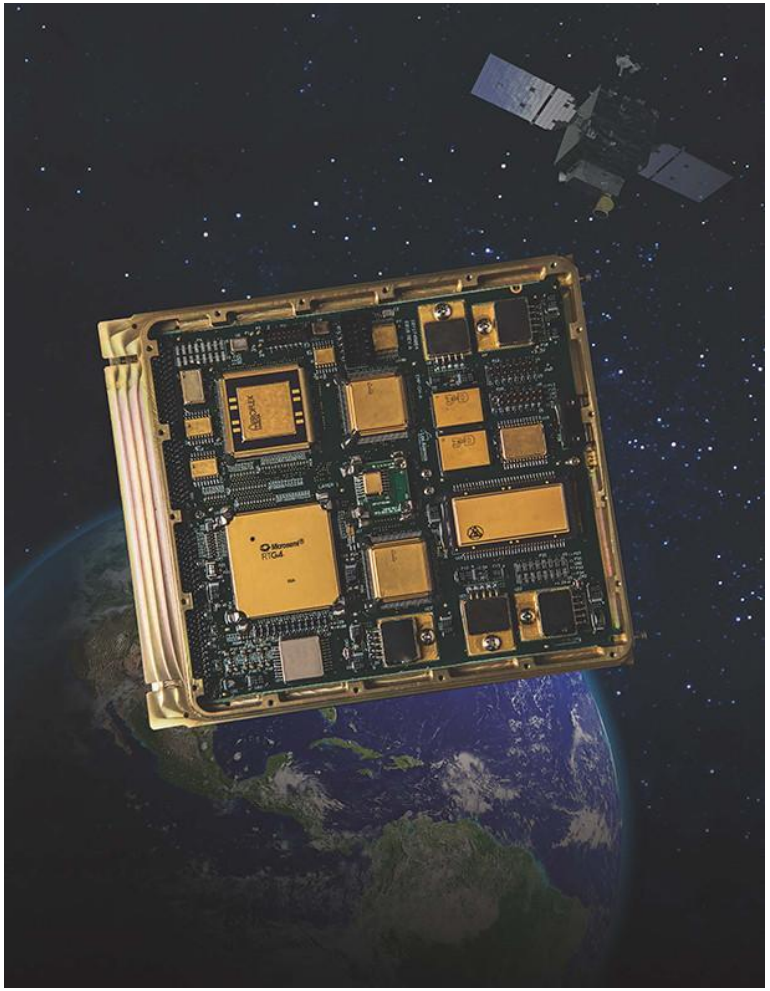
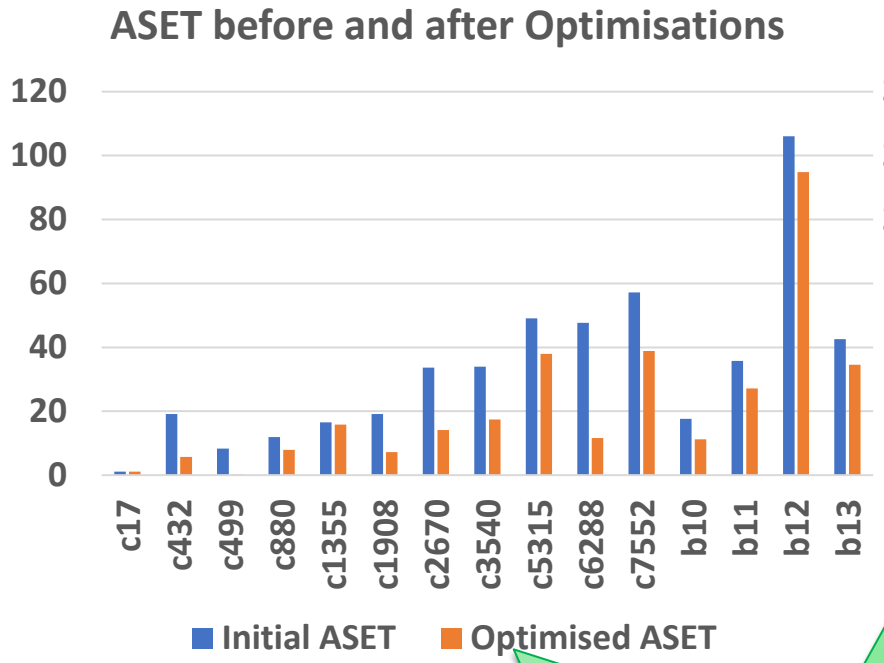
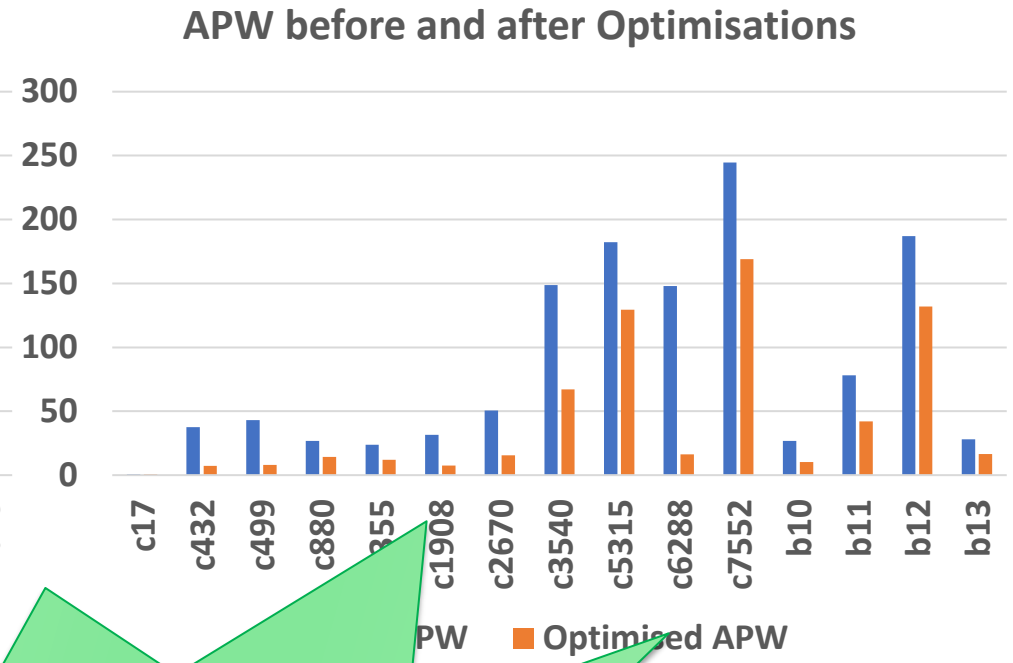


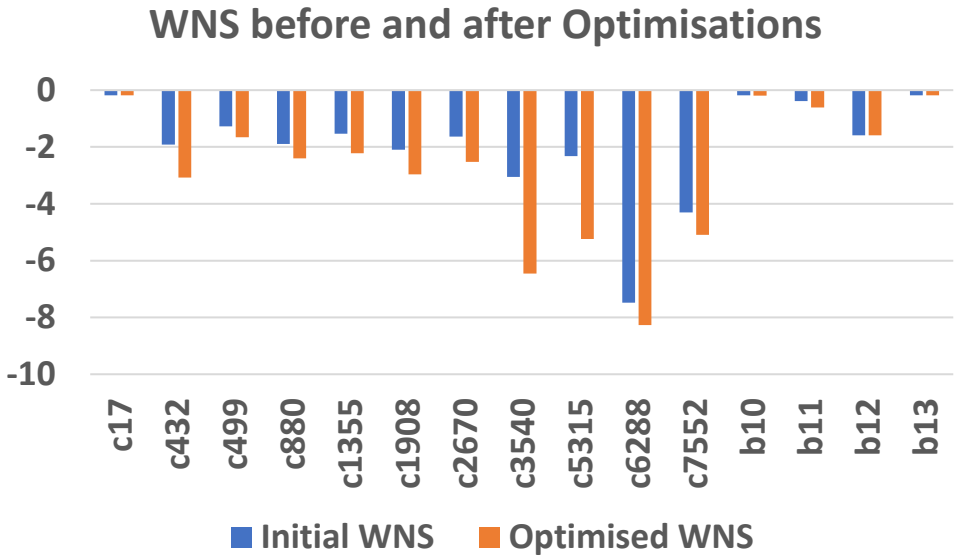
Post-P&R UPSET Optimisation Results: *ASET & APW*

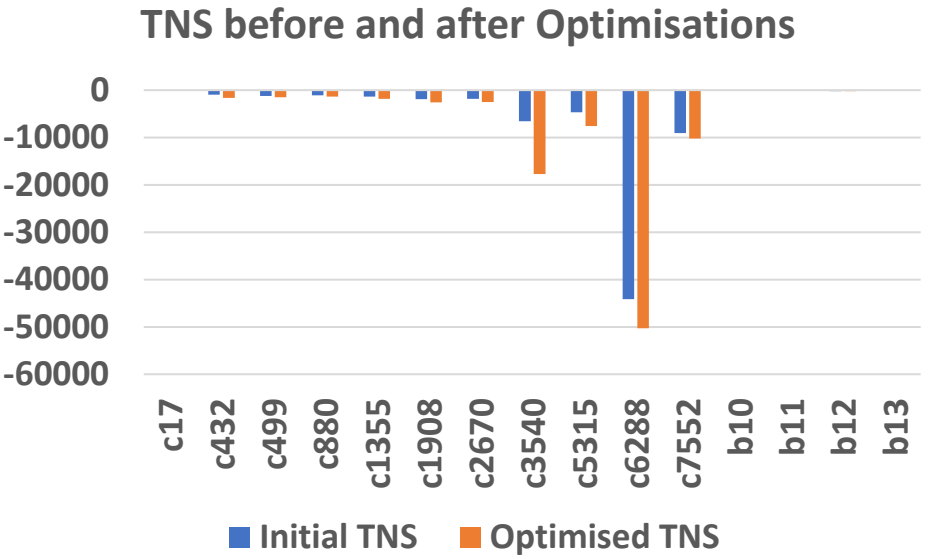


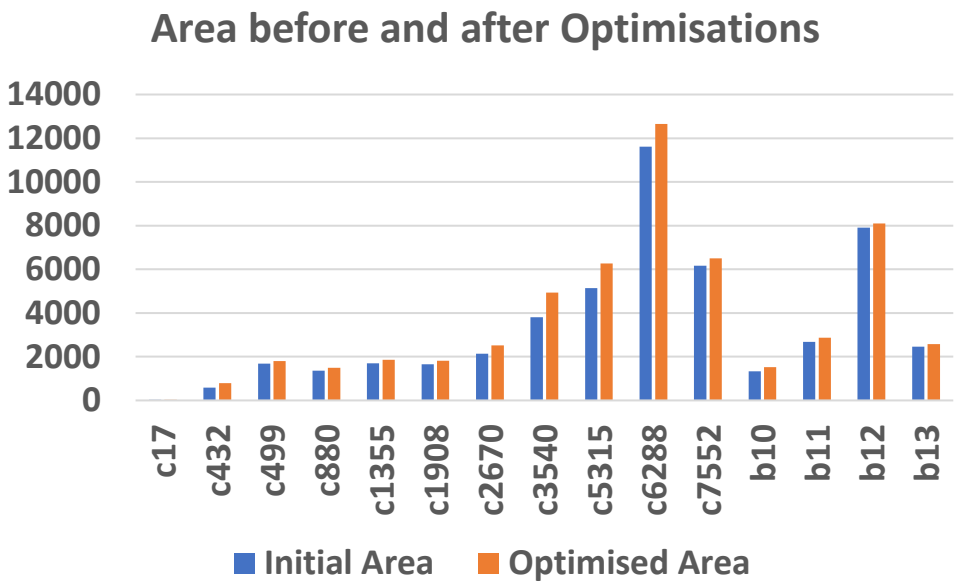


On Average:
ASET: 41% Improvement
APW: 53% Improvement

Post-P&R UPSET Optimisation Results: *Overheads*







On Average:

Total Area: 12% worsening

Worst Negative Slack: 39% worsening

Total Negative Slack: 40% worsening

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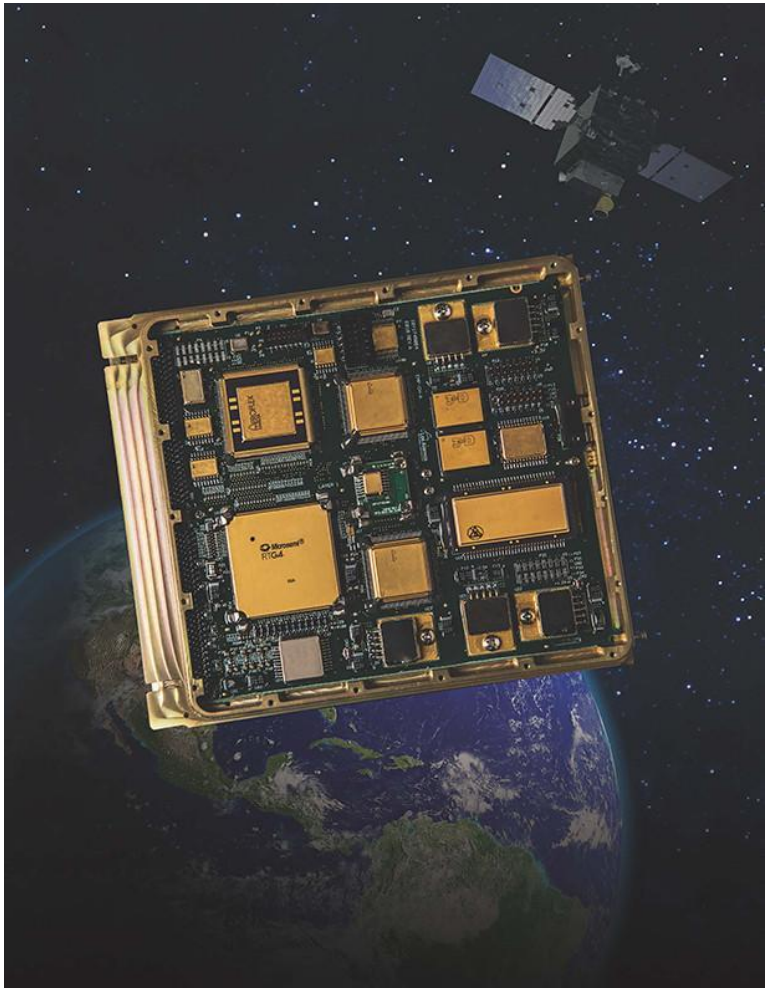

Future Directions

New Features

Incorporate more SET mitigation techniques into the closed-loop

Accurate Models

Using precise SET analysis models can enhance reliability prediction

Power, Performance, Area Consideration

Balancing power, performance, and area is crucial for optimal design

Trade-offs Exploration

Understanding trade-offs can lead to better reliability-performance balance

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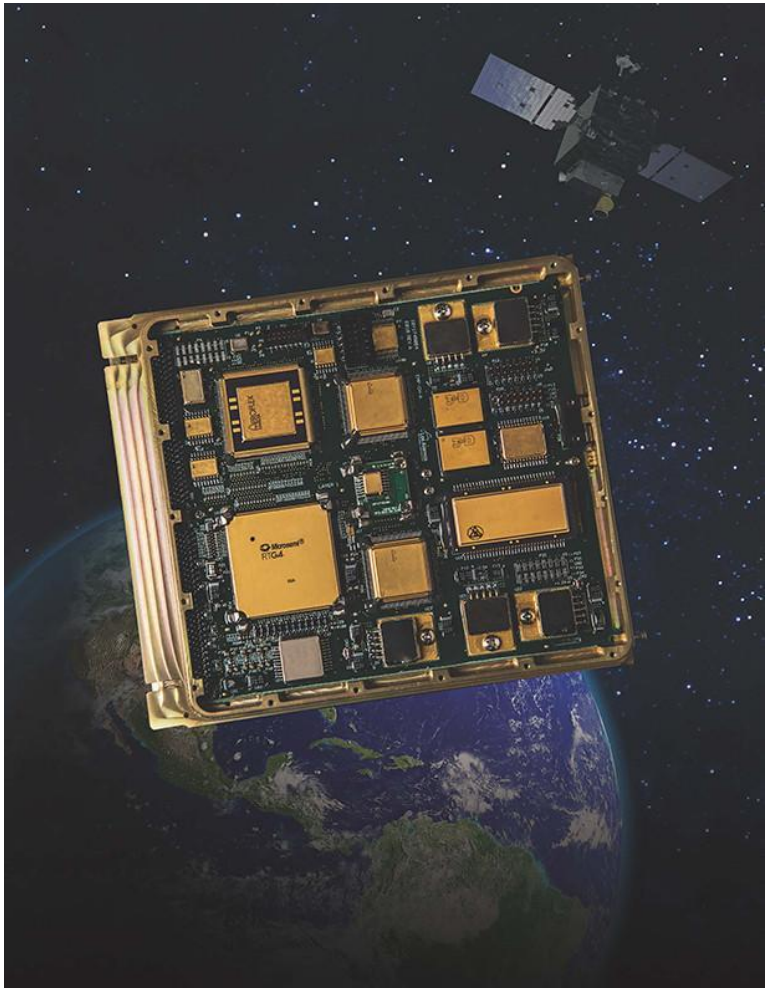

DEMO

Tuesday, 22 July 2025

09:00 - 09:45	**Algorithm/Technology Co-Optimization Unleashed: The Art of Designing AI Chips for Brain-Inspired Edge Computing** Prof. Hussam Amrouch, Technical University of Munich (TUM)
09:45 - 10:30	**Efficient Representations of Digital Circuits in EDA-Applications** Prof. Rene Krenz-Baath, University (UAS) TH-Wildau
10:30 - 10:50	**Coffee Break**
10:50 - 11:35	**Silicon Lifecycle Management Based on Cross-Layer Sensing** Dr. Fabian Luis Vargas, IHP - Leibniz Institute for High Performance Microelectronics
11:35 - 12:20	**Characterization and Modeling of SET Effects in Standard Combinational Cells** Dr. Marko Andjelkovic, IHP - Leibniz Institute for High Performance Microelectronics
12:20 - 13:20	**Demo Session 1** **UPSET** Nikolaos Chatzivangelis, University of Thessaly **EMBER** Alessandro Veronesi, IHP - Leibniz Institute for High Performance Microelectronics
13:20 - 14:20	**Lunch Break**
14:20 - 15:20	**Demo Session 2** **PredicSEE** Prof. Frederic Wrobel, University of Montpelier **ECORCE** Dr. Alain Michez, University of Montpelier
15:20 - 16:05	**Addressing Soft Errors in Asynchronous Bundled Data Design** Dr. Felipe Kuentzer, IHP - Leibniz Institute for High Performance Microelectronics

Tomorrow at 12:20 by Nikolaos Chatzivangelis

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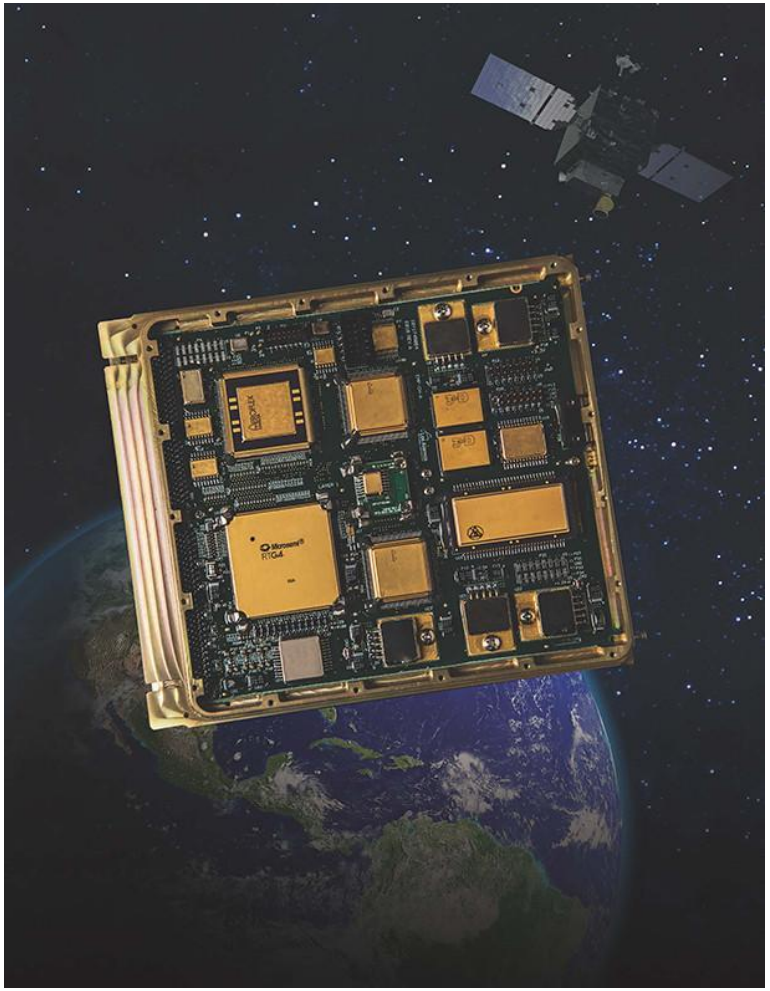

Conclusions

- UPSET: A tool for probabilistic SET analysis and optimisations for large-scale circuits
- Integrated criticality metrics and SET-driven optimisations into the EDA P&R flow
- SET-driven Closed Optimisation loop
  - Gate Resizing, Charge-Sharing Logic Insertion, Cascaded Inverters Insertion, …
- 1st version of Optimisation Loop:
  - improves ASET and APW by 41% and 53% respectively
  - worsens Total Area by 12%, and
  - worsens WNS and TNS by around 40%

UPSET In GitHub

- https://github.com/Circuits-and-Systems-Lab-CASlab/UPSET

Circuits-and-Systems-Lab-CASlab/**UPSET**

UPSET is an automated framework for performing SET Analysis and Optimisation for VLSI circuits utilising Static Timing Analysis principles

3	0	2	0
Contributors	Issues	Stars	Forks

TWINRELECT
TWINNING FOR EXCELLENCE IN RELIABLE ELECTRONICS

Thank you!!

UK Research and Innovation

Funded by the European Union

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Funded by the European Union (Grant Agreement № 101160314). Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union. Neither the European Union nor the granting authority can be held responsible for them.