3MLR: An Investigation of Moment-Matched Mutual Ladder-based Reduction for VLSI Static Timing Analysis

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UK Research and Innovation

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PEX Networks Are Becoming a Signoff Bottleneck

01

ECO Iterations Multiply Cost

Signoff timing closure requires repeated Engineering Change Orders, each triggering a fresh parasitic extraction pass.

02

Interconnect Dominates Delay

Shrinking wire width raises resistance; denser routing raises coupling capacitance at advanced nodes.

03

SPEF Files Grow With Design Size

Billions of transistors and detailed extraction models push RC networks to sizes that strain memory and storage.

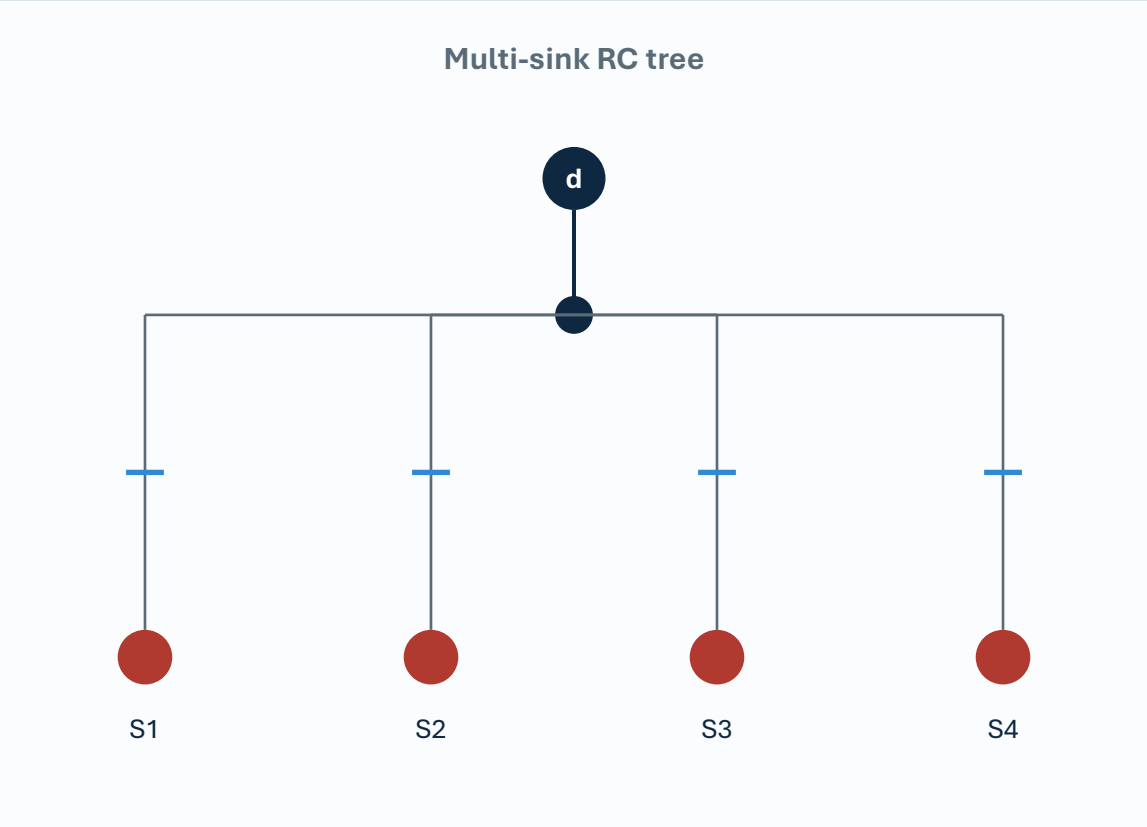
Goal: *compress RC networks substantially while keeping per-sink delay and arrival-time error within signoff tolerance.*

Two Established Families of RC Reduction

Method	Approach	Limitation
TICER	Topology-preserving node elimination; preserves Elmore delay via ladder segments.	No canonical output topology; doesn't optimize per-sink arrival time.
O'Brien & Savarino	Moment-matching at the driving point; accurate π-model at the source.	Collapses all sinks into two lumped capacitors — no per-sink arrival times.
Ang et al.	Extraction-time delay tolerance; 75% SPEF size reduction within 5 ps.	Relies on the extractor's engine, not a standalone analytical method.

- **3MLR combines both strengths**
  - Moment-matched accuracy with an explicit per-sink ladder topology, gated by a structural complexity score.

RC Trees, Elmore Delay, and Reduction Targets



- **Reduction target**
  - Find a reduced tree $\hat{T}$ with $|\hat{V}| \ll |V|$ such that the first-moment error at every sink stays below tolerance δ:

$$| \hat{m}_1(s_i) - m_1(s_i) | / m_1(s_i) \leq \delta$$

  - Subject to $R, C \geq 0$ and total capacitance conservation $\Sigma C_v \hat{=} C\_tot$

3MLR: Reduction Pipeline & Adaptive Sink Clustering

Moment Computation
Bottom-up C + two pre-order passes for m_1, m_2

→

Adaptive Clustering
Group sinks by timing similarity into stages

→

Ladder Formulation
Closed-form node capacitances via linear solve

1 Feature vector per sink

$f(s) = (m_1, m_2, R\_path)$

2 Initial grouping by observed net range

10% agreement rule

3 Until target stage count n is reached

Merge by centroid distance

4 Fixes final ladder stage order

Sort by R_path

Gating
A structural complexity score Φ identifies nets unsuitable for ladder reduction and passes them through unreduced (only multi-sink nets are processed).

Scope: *applies to multi-sink nets only — single-sink and clock nets bypass the pipeline entirely.*

Structural Complexity Score Φ

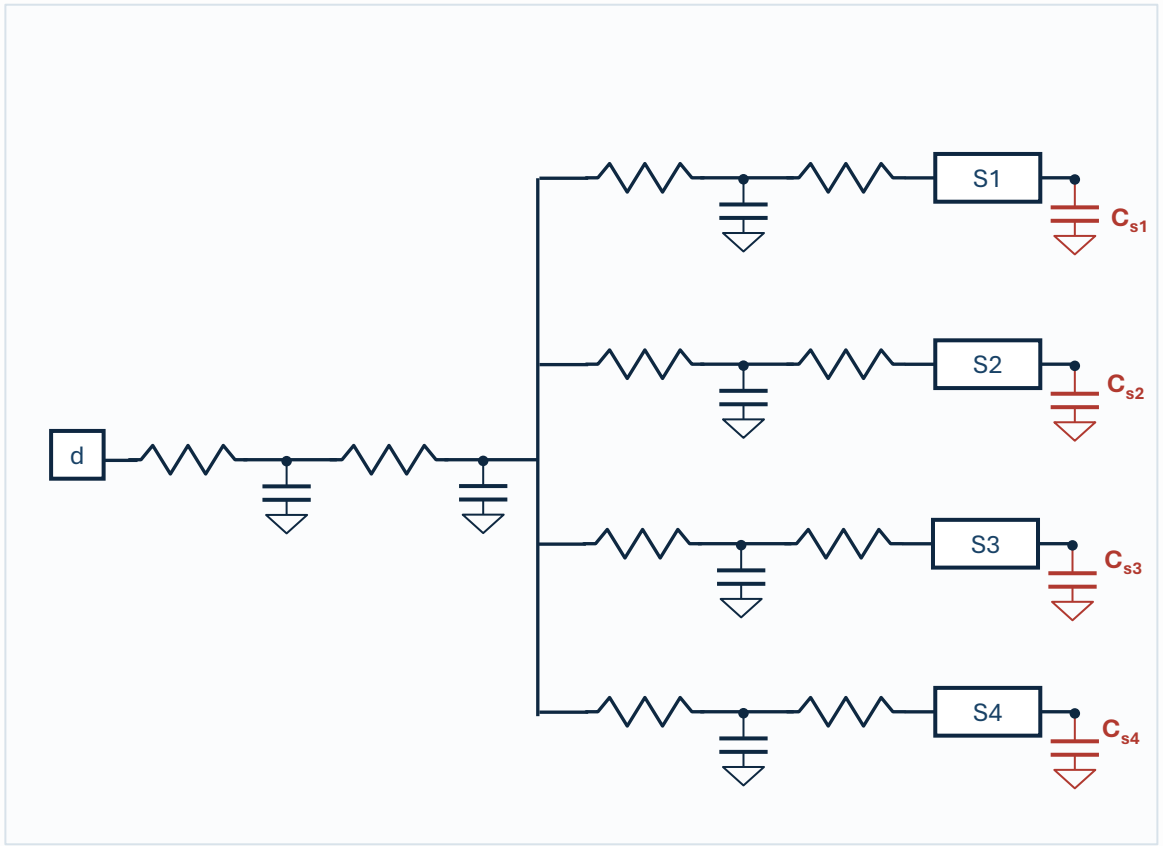
- Five sub-scores, each scaled to [0,1], measure how far a net's structure deviates from the ladder topology's assumptions
- Their equal-weighted average gives the composite score Φ
- Nets are gated at Φ = 0.35, a threshold derived empirically

S_LCA	S_res	S_cap	S_out	S_fan
Early branching	Branch-dominated resistance	Capacitive imbalance	Outlier branch length	Fanout risk (3–5)

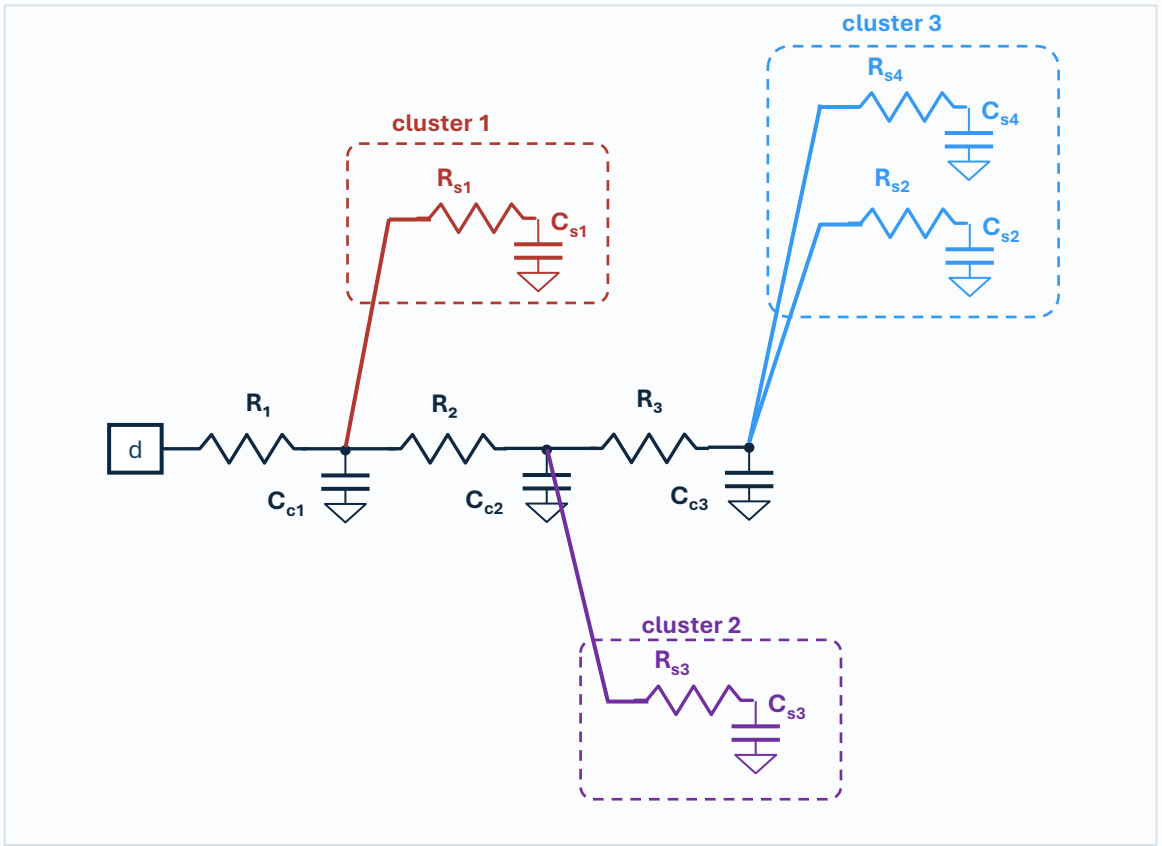
- Fanout risk best separates failing from passing nets (2.25×), ahead of capacitive imbalance (1.67×) and branch-dominated resistance (1.34×)

3MLR Reduction: Original Tree vs. Reduced Ladder

Node capacitances solved exactly via **A·c = b** — a symmetric positive-definite linear system matching first moments at every cluster.



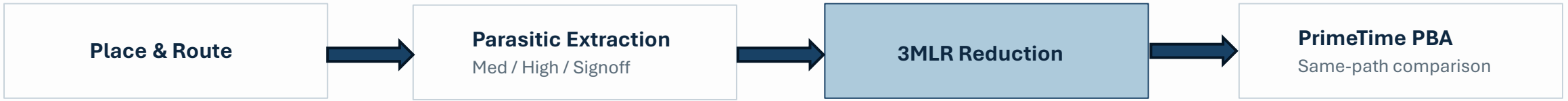
(a) Original RC tree with driver **d** and sinks S_1–S_4, multiple RC segments per branch.



(b) 3MLR reduced structure — clusters attach to shared ladder nodes via residual R_{si} and local C_{si}.

Fig. 1 — 3MLR reduction: sinks S_1–S_4 grouped into clusters C_1–C_3, each attached to the shared ladder via trunk resistances R_1–R_3 and node capacitances C_{ci}.

Six OpenCores Designs, Three PEX Effort Levels



Design	Cells	Pins	Nets	Util. (%)	Max FO
aes	4,393	18,096	4,784	65	76
aes_cipher_top	11,630	41,225	12,021	71	71
des3	2,180	8,465	2,486	73	65
mc_top	5,410	19,568	5,681	63	62
pci_bridge32	12,091	47,159	12,465	64	75
nvdla	167,833	683,388	169,076	60	76

ASAP7 7 nm PDK • PrimeTime with CCSN + full waveform propagation • nvdla sign-off SPEF unavailable

SPEF Compression Under Φ-Restricted 3MLR

Design	Node Count Reduction (%)	File Size Reduction (%)
aes	16.3	9.4
aes_cipher_top	19.6	11.8
des3	20.9	12.3
mc_top	22.4	12.8
nvdla	19.4	9.8
pci_bridge32	**23.5**	**13.2**

23.5%

peak node-count reduction (pci_bridge32, high effort)

13.2%

peak file-size reduction (pci_bridge32, high effort)

Signoff-Effort Arrival-Time Accuracy

Design	<1% AT Error	1–3% AT Error	≥3% AT Error
aes	100.0	0.0	0.0
aes_cipher_top	90.6	9.4	0.0
des3	100.0	0.0	0.0
mc_top	100.0	0.0	0.0
pci_bridge32	98.9	0.2	0.9

98.3%

average paths across designs with <3% arrival error (10k paths/design, signoff)

Thank you!

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