Radiation Detection Integrated Read out Front Ends - Design and methodology Challenges

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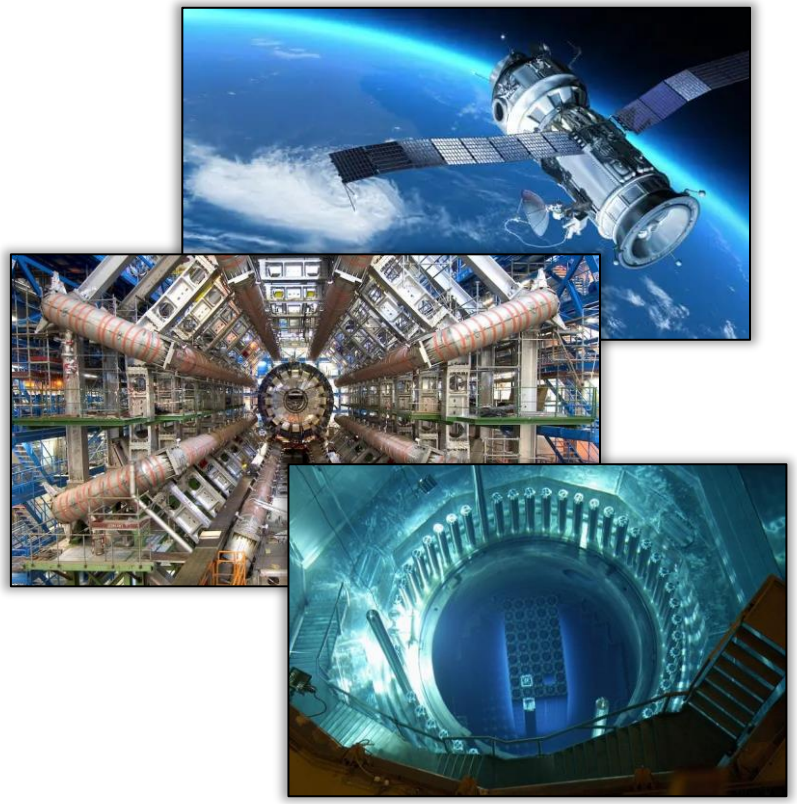
Radiation Hardened Electronics

•Radiation-hardened ICs are crucial for **mission-critical systems** in:

- **Space exploration**
- **High-energy physics** experiments
- **Nuclear reactor** control systems



Emerging Challenges

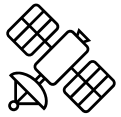
•Next-gen applications (e.g., Space 2.0, LHC upgrades) demand:

- **High resilience** under intense radiation
- **Improved performance** and reliability

Success depends on **advanced radiation-hardened electronics** and **innovative design approaches**

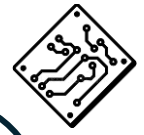
Radiation Hardened Electronics

Space-rated electronics



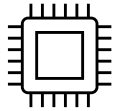
- ✓ High Technology Readiness Levels (TRLs)
- ✓ Lower design costs
- × Radiation resistance can be limited
- × Fewer available parts and vendors.

Radiation-resistant COTs



- ✓ Use inherently radiation-tolerant components
- ✓ Cost-effective solution
- × Require extensive testing
- × May lead to larger physical footprints (i.e., bulky products)

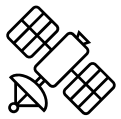
Radiation hardened ASICs



- ✓ Most robust for radiation-heavy environments
- ✓ Uses RHBD and RHBP techniques
- ✓ Works with legacy nodes
- ✓ Optimized MOSFET layouts (ELT, DGA, H-Gate)

Radiation Hardened Electronics

Space-rated electronics



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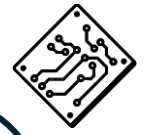
Radiation-resistant COTs



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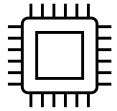

- ✓ Most robust for radiation-heavy environments
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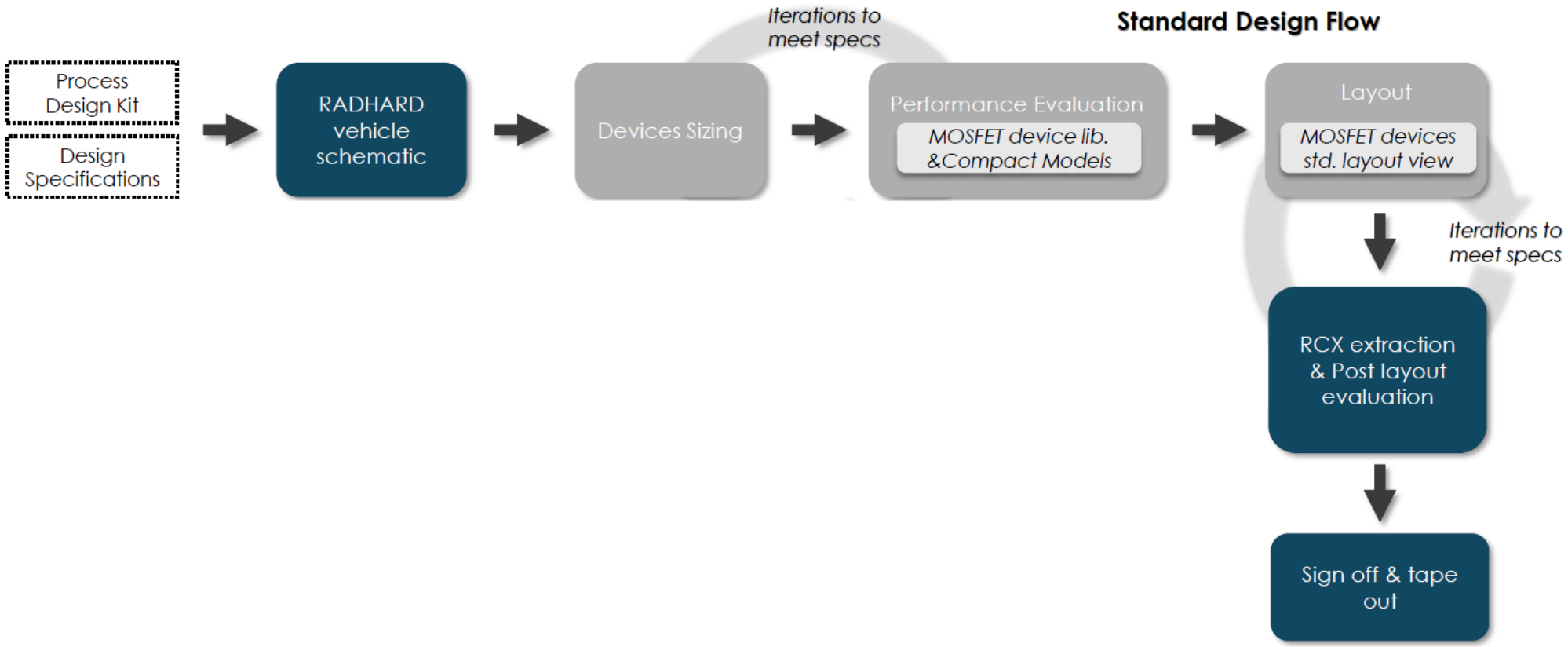
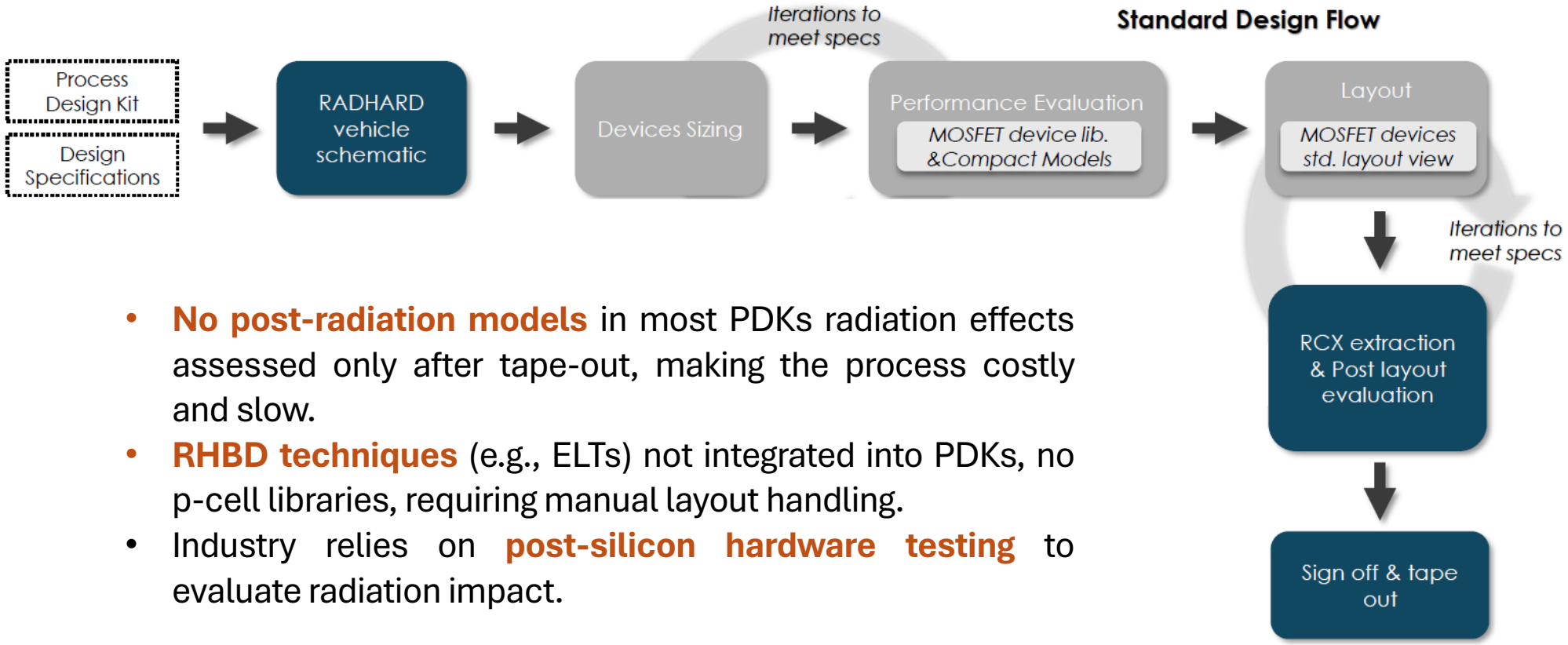
No standard design methodology available!

Standard IC design methodology

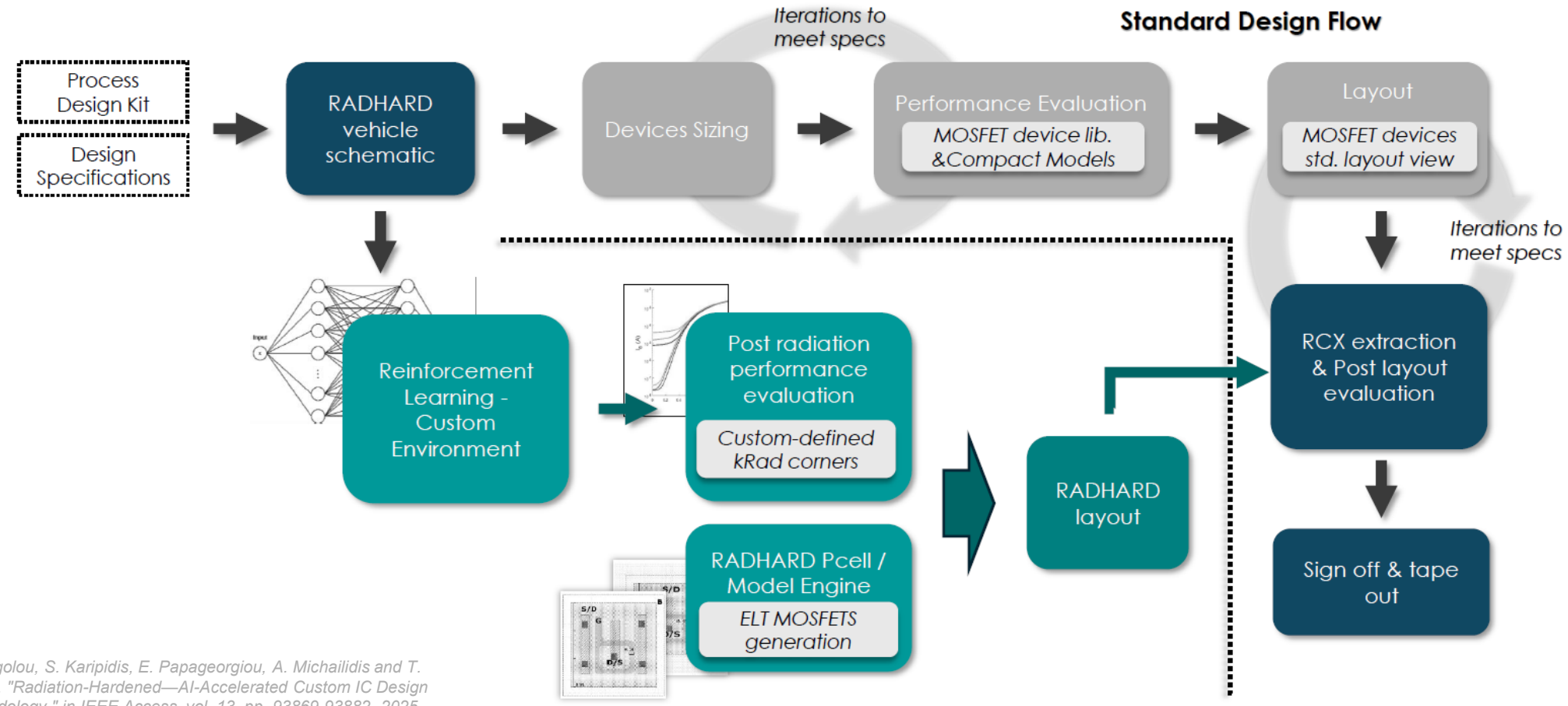


Standard IC design methodology



- **No post-radiation models** in most PDKs radiation effects assessed only after tape-out, making the process costly and slow.
- **RHBD techniques** (e.g., ELTs) not integrated into PDKs, no p-cell libraries, requiring manual layout handling.
- Industry relies on **post-silicon hardware testing** to evaluate radiation impact.

AI-accelerated Rad-Hard design methodology



V. Gogolou, S. Karipidis, E. Papageorgiou, A. Michailidis and T. Noulis, "Radiation-Hardened—AI-Accelerated Custom IC Design Methodology," in IEEE Access, vol. 13, pp. 93869-93882, 2025, doi: 10.1109/ACCESS.2025.3574058.

Product vehicle: Charge Sensitive Amplifier

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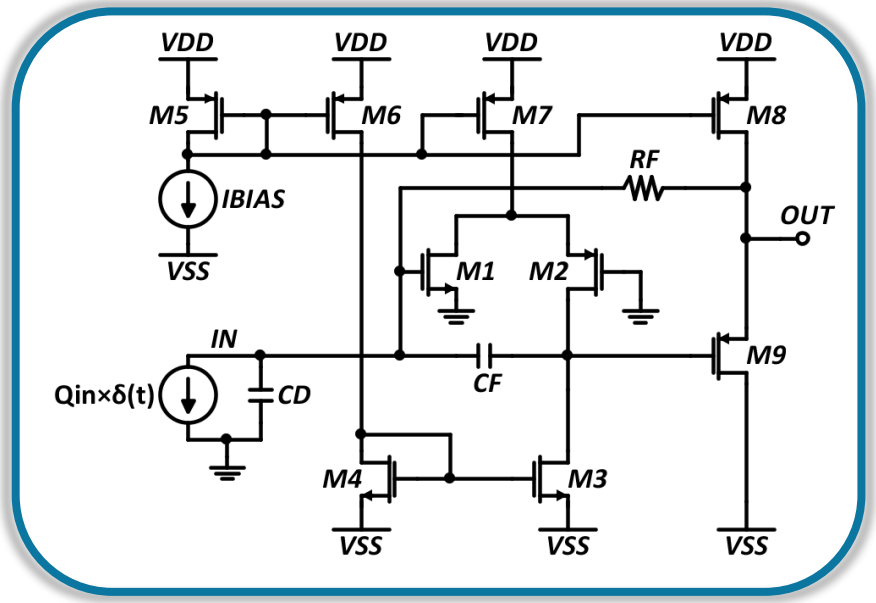
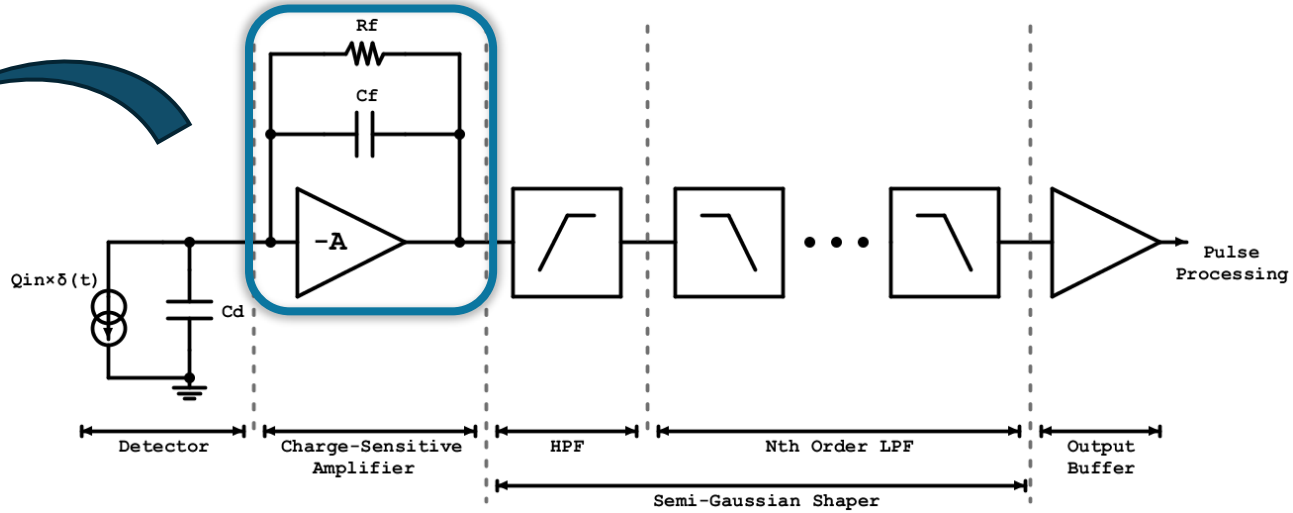
Folded-cascode architecture





Design parameters	Symbol	Step Size	Range
M3-4 W/L	w_l_bot_mrr	0.1	[0.2-2]
M5-8 W/L [1]	w_l_top_mrr	0.2	[0.4-4]
M9 W/L	w_l_nmos_out	17.5	[35-285]
M8 W/L multiplier	m4	2	[2-20]
Feedback capacitance (fF)	Cf		
Reset resistor (kΩ)	Rf		
M1 W/L (222 x num of.fingers) [2]	nf		
M2 W/L (114 x num of.fingers)	nf		

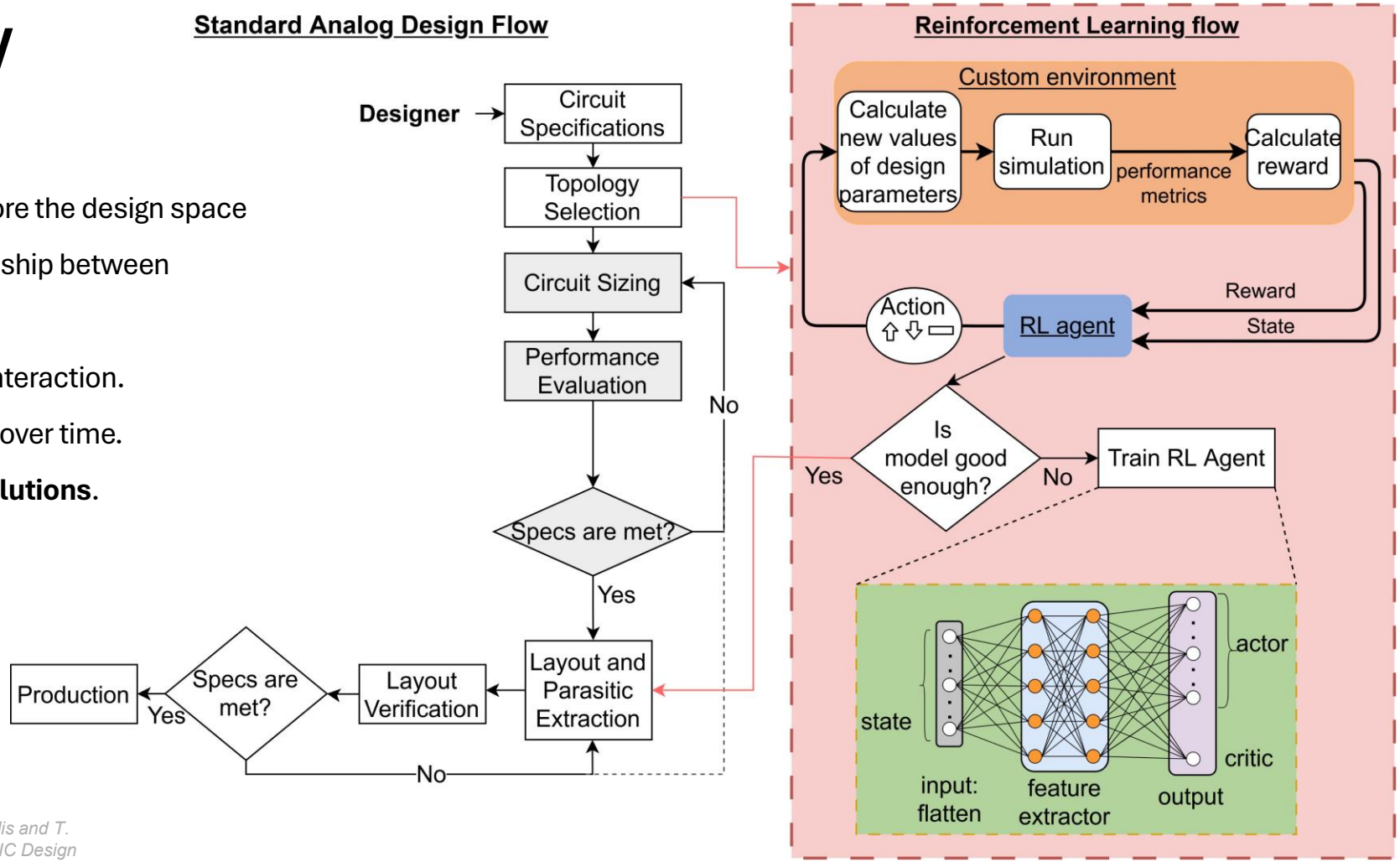
Set design parameters

Set performance metrics

Performance metrics	Category	Threshold
Power (mW)	Constrain (min)	1
Voltage gain (dB)	Constrain (max)	80
Transimpedance gain (dB)	Constrain (max)	120
Bandwidth (MHz)	Constrain (max)	1
Peaking time (us)	Constrain (min)	2
RMS noise (uV)	Objective (min)	1e-3

RL assisted analog design flow

- **Reinforcement Learning** to explore the design space without prior knowledge of relationship between design parameters and metrics
- Mimics human learning through interaction.
- Learns from feedback to improve over time.
- Discovery of **multiple optimal solutions**.



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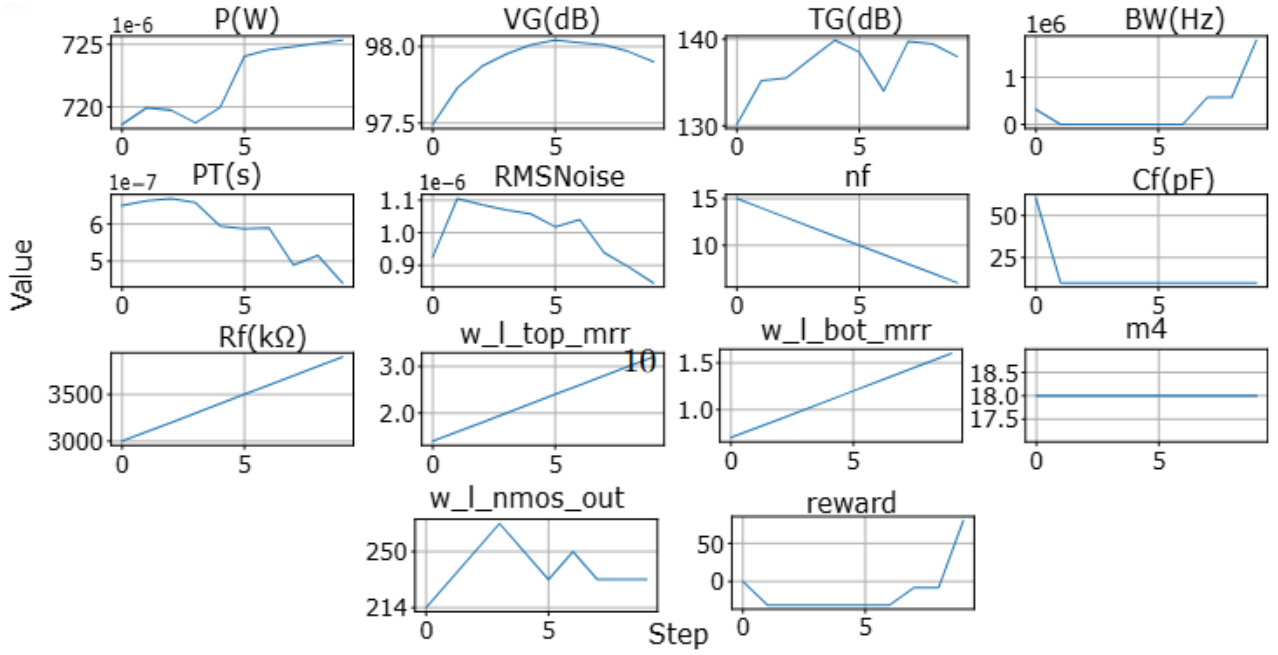
Experiments and results

- After training, 100 episodes are run to validate the RL agent's performance.
- Each episode starts from a random point in the design space to ensure converge in feasible solutions across the entire space.



Snapshot of single episode completed in **9 steps**

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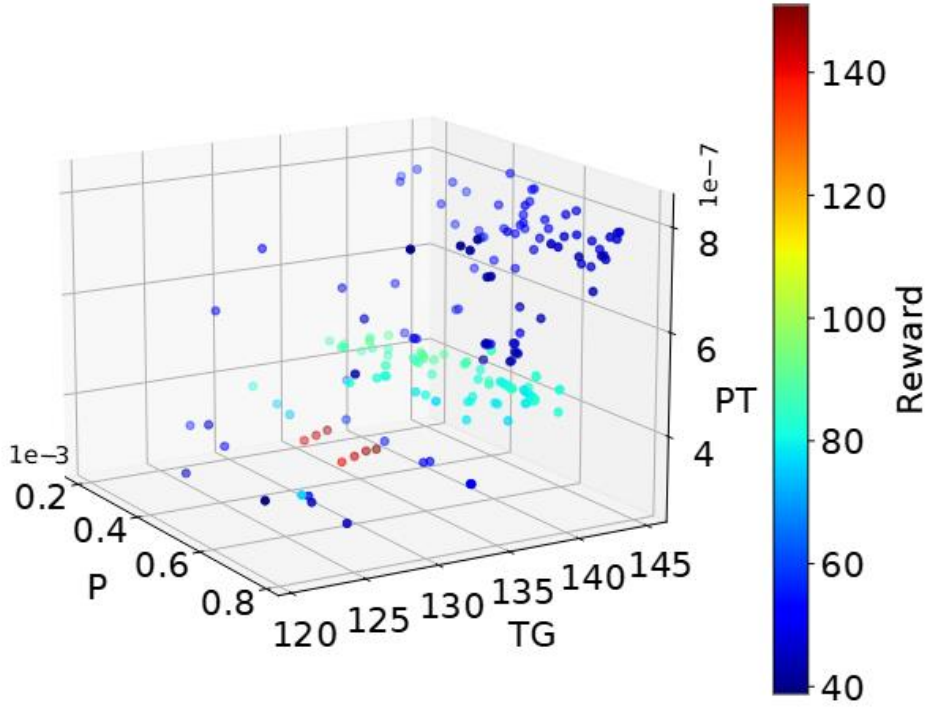
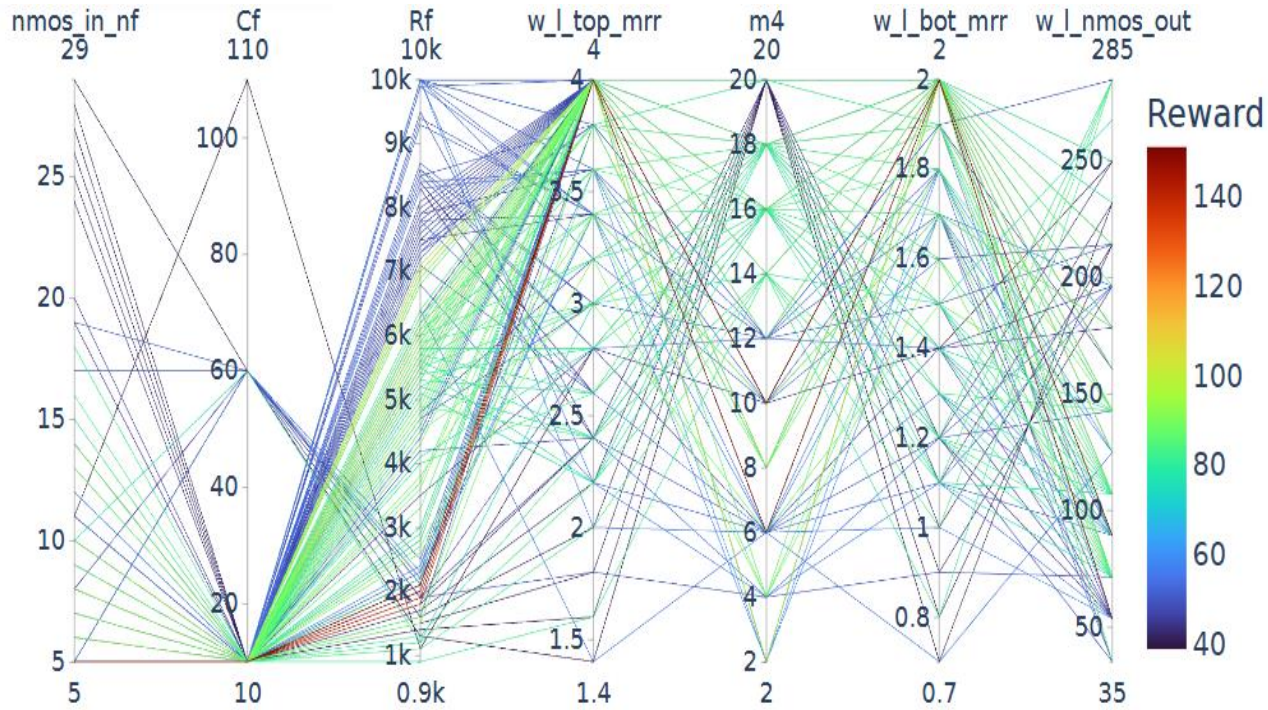


3D heated scatter plot of the feasible solutions



Parallel coordinates plot of the design parameter for the feasible solutions

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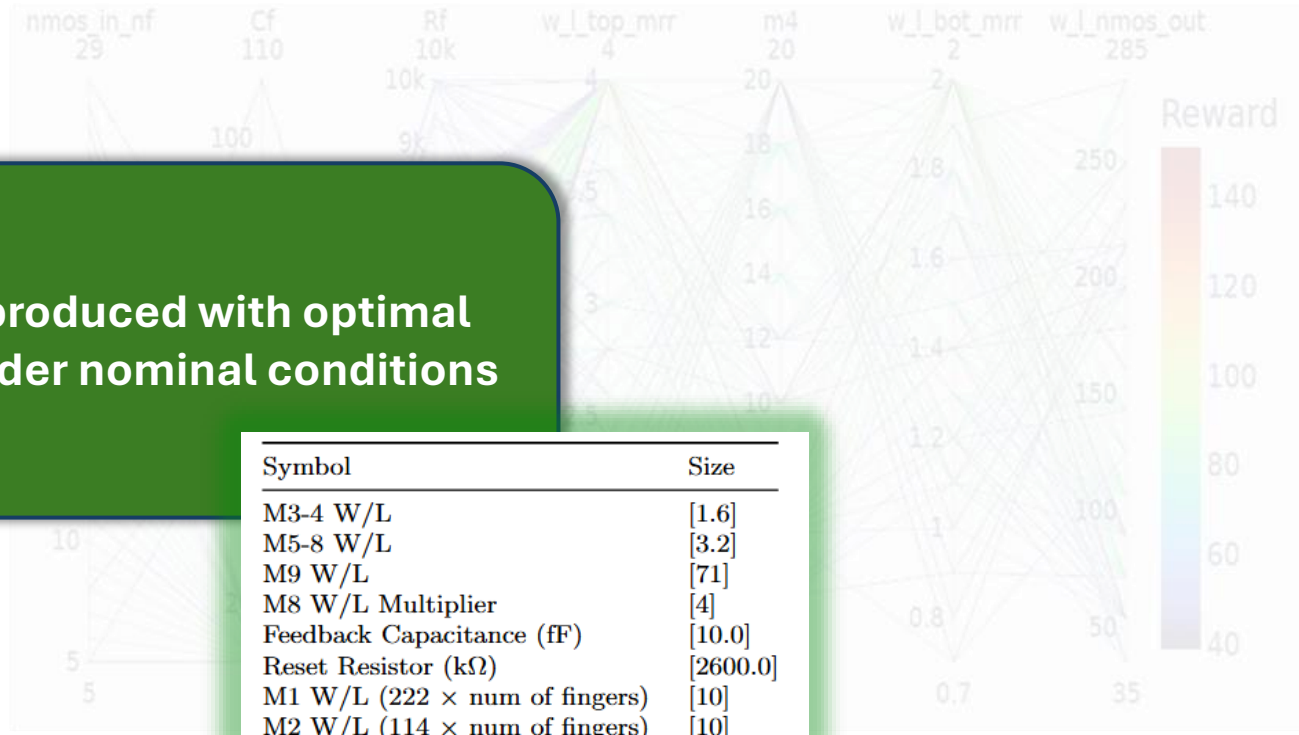
CSA design is produced with optimal performance under nominal conditions

Symbol	Size
M3-4 W/L	[1.6]
M5-8 W/L	[3.2]
M9 W/L	[71]
M8 W/L Multiplier	[4]
Feedback Capacitance (fF)	[10.0]
Reset Resistor (kΩ)	[2600.0]
M1 W/L (222 × num of fingers)	[10]
M2 W/L (114 × num of fingers)	[10]



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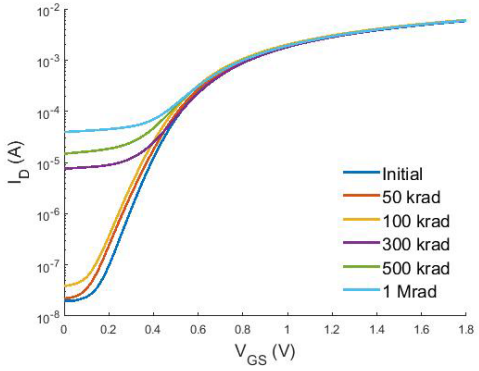
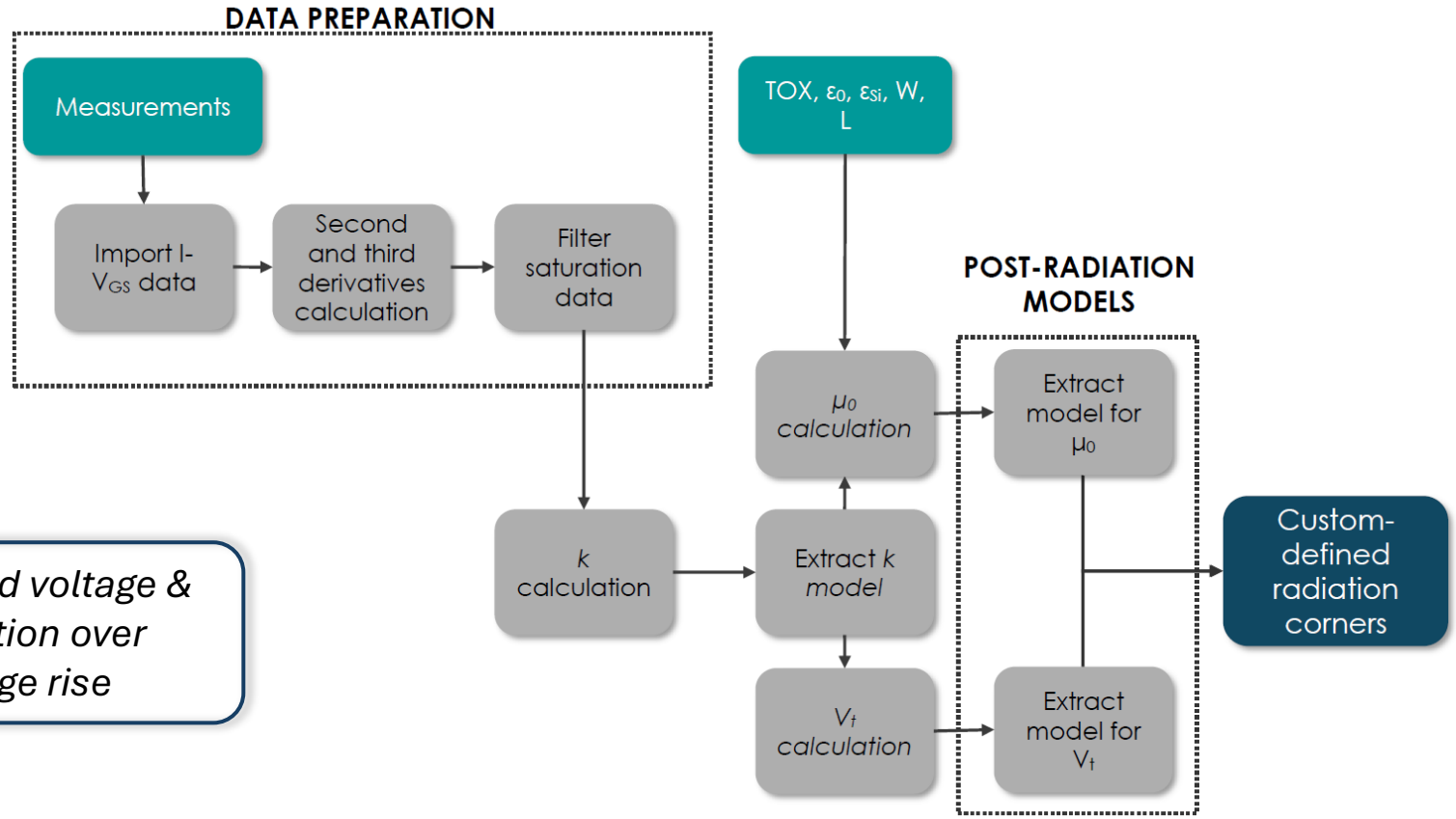
Parallel coordinates plot of the design parameter for the feasible solutions

Post-radiation modeling





MOSFET's threshold voltage & mobility calculation over radiation dosage rise

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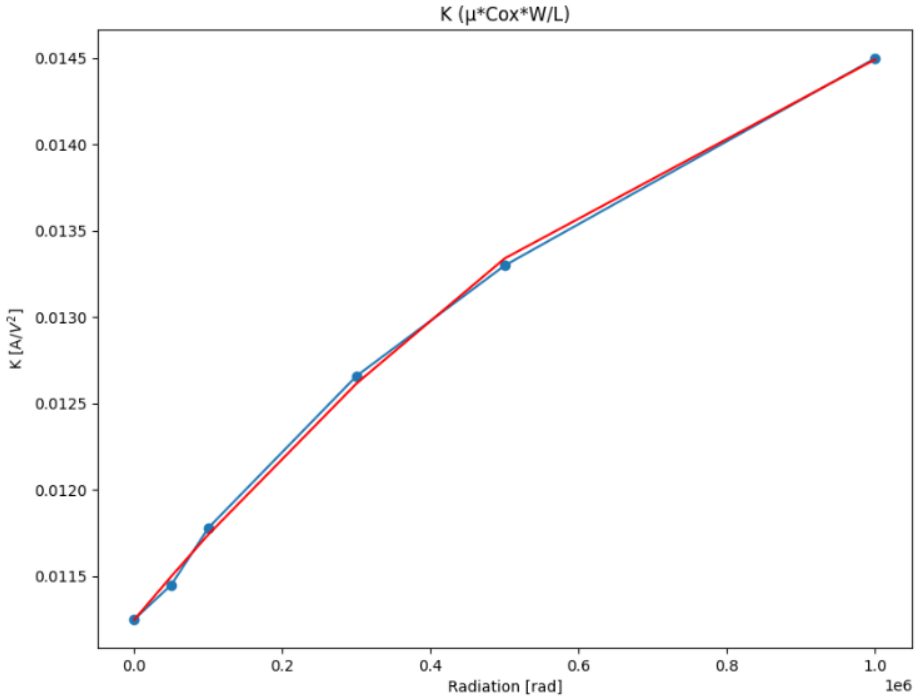
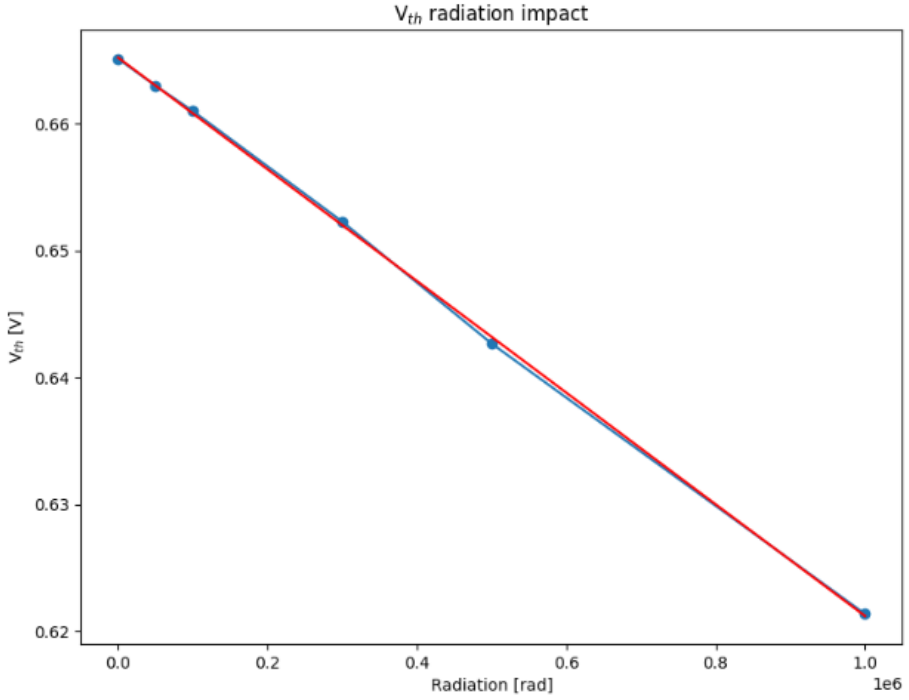


k as a function of radiation level along with the second order polynomial fit in *red*.



Vt as a function of radiation level along with the linear fit in *red*.

Post-radiation modeling

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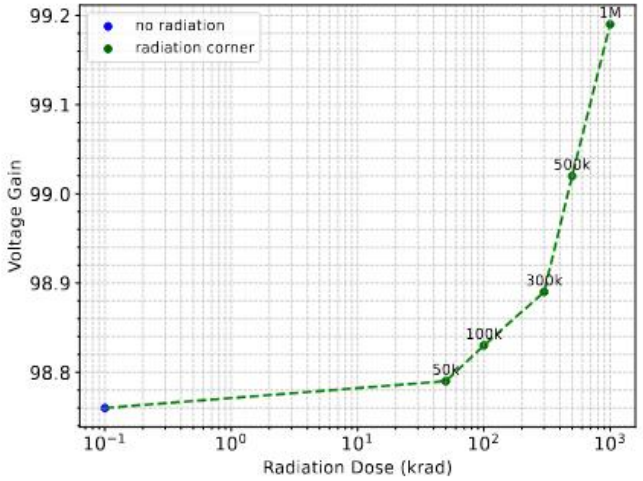

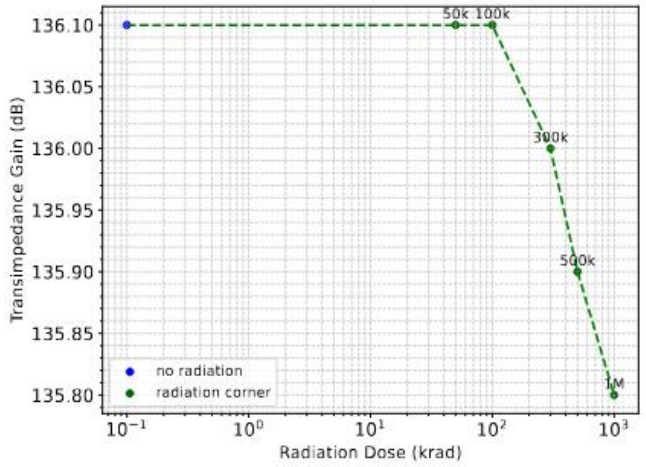

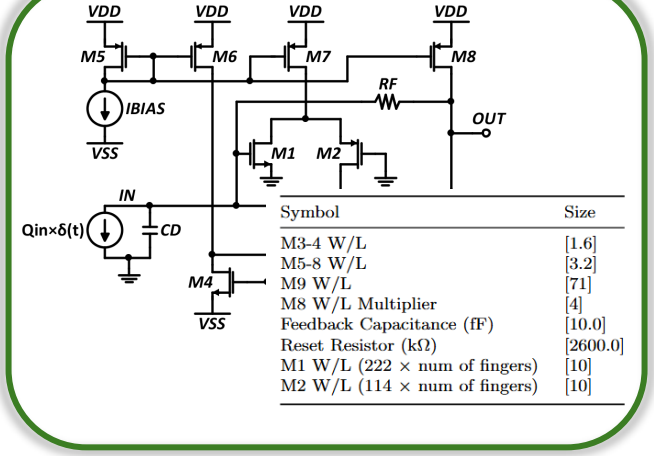

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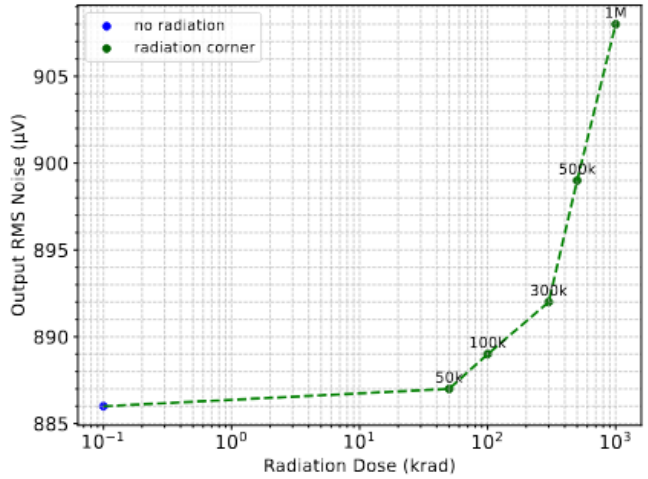
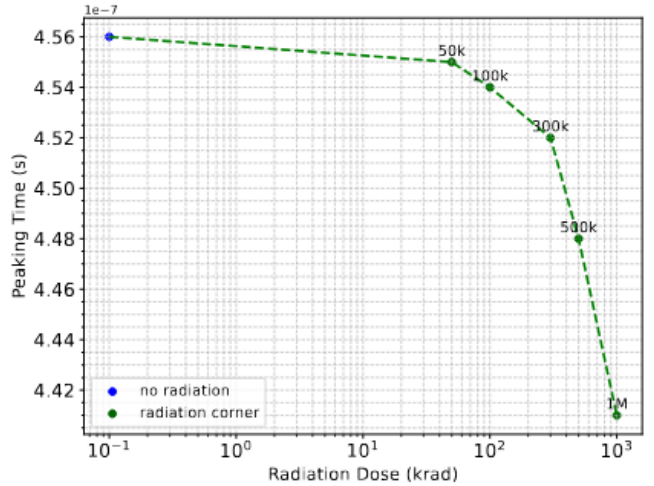
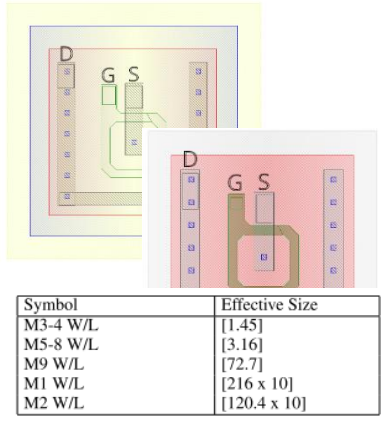
Radiation induced performance variation on the RL-generated CSA vehicle





Rad-hard pCell generator

Radhard cells exploitation in analog design



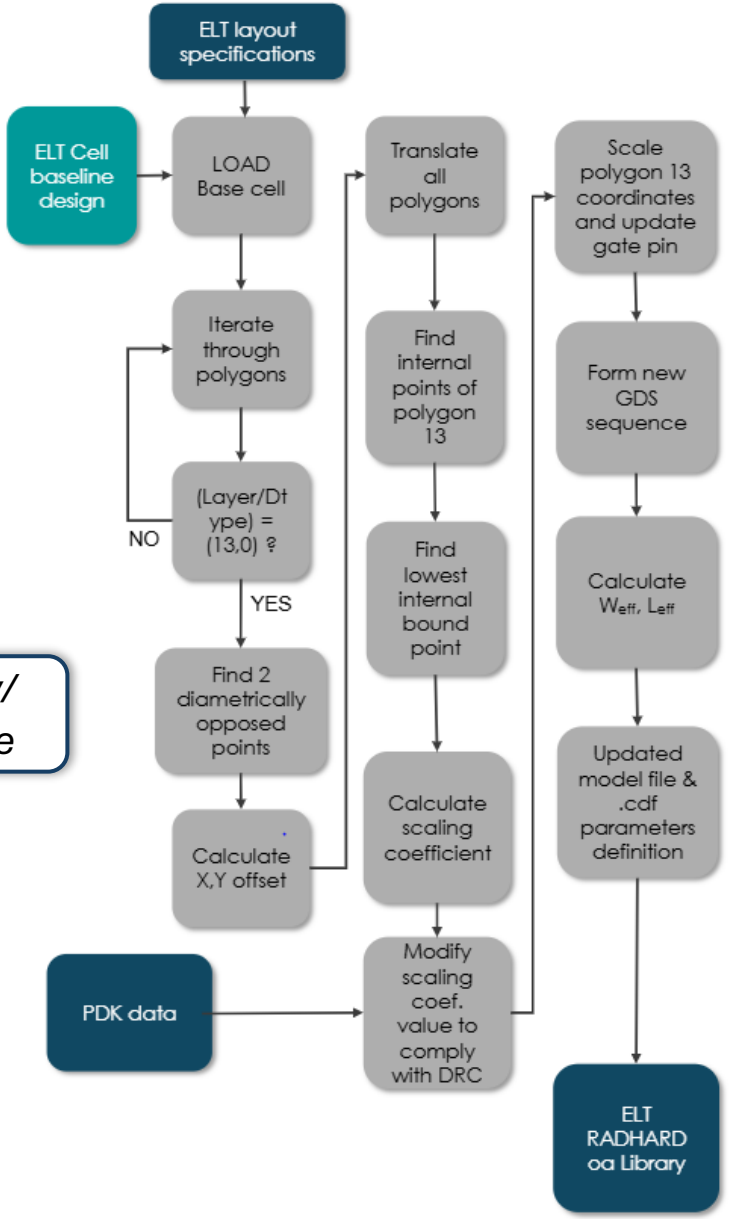
Symbol	Effective Size
M3-4 W/L	[1.45]
M5-8 W/L	[3.16]
M9 W/L	[72.7]
M1 W/L	[216 x 10]
M2 W/L	[120.4 x 10]

$$\left(\frac{W}{L}\right)_{eff} = 4\frac{2\alpha}{\ln\frac{d'}{d'-2\alpha L}} + 2K\frac{1-\alpha}{\frac{1}{2}\sqrt{\alpha^2+2\alpha+5}\cdot\ln\frac{1}{\alpha}} + 3\frac{\frac{d-d'}{2}}{L}$$

Algorithm 2 pCell Sizing Algorithm

```
poly13 ← ""
for polygon ← cell_polygons do
    if polygon.layer = 13 and polygon.datatype = 0 then
        poly13 ← polygon
        break
    end if
end for
point1, point2 ← diametrically opposed borderpoint coordinates
offsetX ← point1.x − (point1.x − point2.x)/2
offsetY ← point1.y − (point1.y − point2.y)/2
for p in cell_polygons do
    translate(p, −offsetX, −offsetY)
end for
intern_points ← internal_filter(poly13.points)
low_intern_bound ← min(intern_points)
coef ← (low_intern_bound + ratio · base_l)/(low_intern_bound + base_l)
if coef > drc_upper_limit then
    coef = drc_
end if
if coef < drc_
    coef = drc_
end if
update_Gate_Pin()
for coordinate in poly13.coordinates do
    if coordinate not in intern_points then
        poly13.coordinate ← poly13.coordinate · coef
    end if
end for
update_GDS_cell()
WtoLeff ← EffectiveChannelCalc (W, L)
new_model_params ← update_Model(WtoLeff)
return GDS_cell, new_model_params
```

Python script w/ GDSPY package



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Rad-hard pCell generator

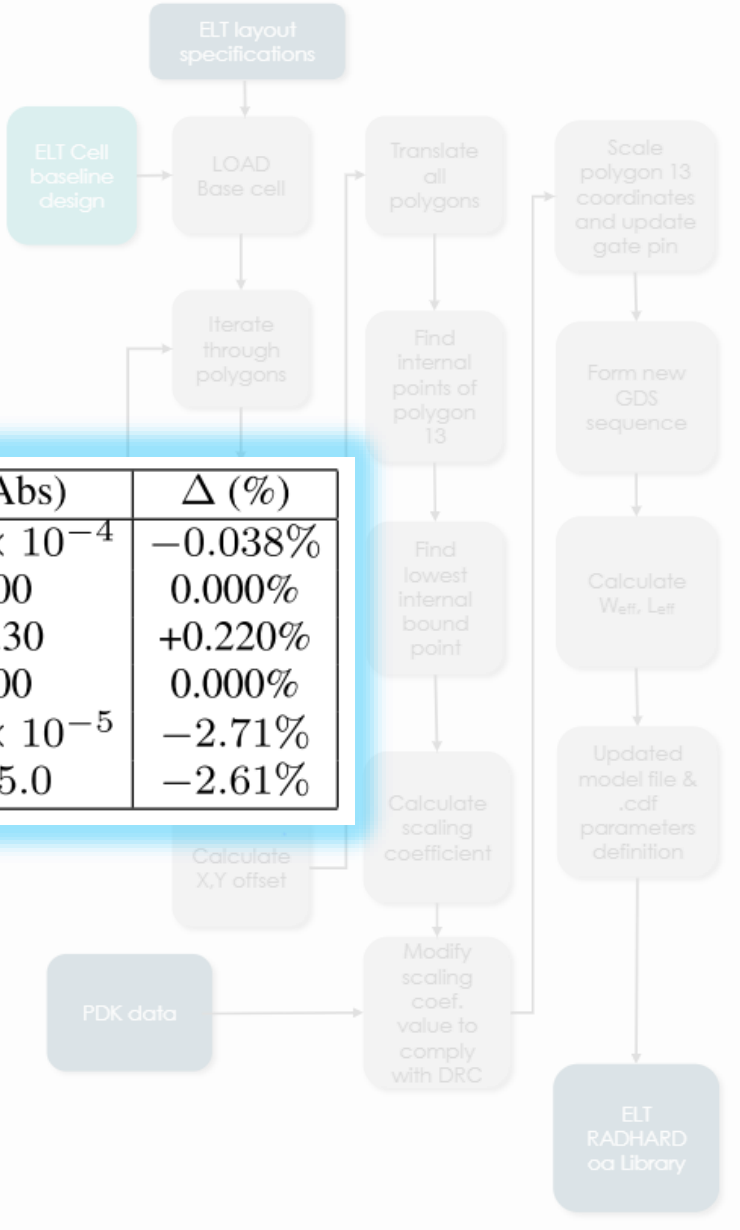
Radhard cells exploitation in analog design

Metric	Conventional	ELT	Δ (Abs)	Δ (%)
Power Dissipation (mW)	2.609×10^{-1}	2.608×10^{-1}	-1.0×10^{-4}	−0.038%
Voltage Gain (dB)	98.76	98.76	0.00	0.000%
Transimpedance (dB)	136.10	136.40	+0.30	+0.220%
Peaking Time (μs)	456.0	456.0	0.00	0.000%
RMS Noise (V)	8.859×10^{-4}	8.619×10^{-4}	-2.4×10^{-5}	−2.71%
Bandwidth (MHz)	1341.0	1306.0	−35.0	−2.61%

Algorithm 2 pCell Sizing Algorithm

```
poly13 ← ""
for polygon ← cell_polygons do
    if polygon.layer = 13 and polygon.datatype = 0 then
        poly13 ← polygon
        break
    end if
end for
point1, point2 ← diametrically_opposed_borderpoint coordinates
...
poly13.coordinate ← poly13.coordinate - coef
    end if
end for
update_GDS_cell()
WtoLeff ← EffectiveChannelCalc (W, L)
new_model_params ← update_Model(WtoLeff)
return GDS_cell, new_model_params
```

$$\left(\frac{W}{L}\right)_{eff} = 4\frac{2\alpha}{\ln\frac{d'}{d'-2\alpha L}} + 2K\frac{1-\alpha}{\frac{1}{2}\sqrt{\alpha^2+2\alpha+5}\cdot\ln\frac{1}{\alpha}} + 3\frac{\frac{d-d'}{2}}{L}$$



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State-of-the-Art assessment

V. Gogolou, S. Karipidis, E. Papageorgiou, A. Michailidis and T. Noulis, "Radiation-Hardened—AI-Accelerated Custom IC Design Methodology," in IEEE Access, vol. 13, pp. 93869-93882, 2025, doi: 10.1109/ACCESS.2025.3574058.

Ref.	Circuit/Device Level	Target Vehicle	Design Cycle Speedup	Post-Rad Model	Rad-Hard Design	Pre-signoff Evaluation	Standard Flow Compatible
[28]	Digital	Ring-Osc	✗	✓	✗	✓	✓
[29]	Device	MOSFET	✗	✓	✗	✗	✗
[31]	Digital	Ring-Osc	✗	✗	✓	✗	✓
[33]	Digital	Flip-Flop	✗	✓	✓	✗	✓
[34]	Digital	Std. Cell Gates	✗	✓	✗	✓	✗
This work	Analog	CSA	✓	✓	✓	✓	✓

- ✓ Targets **analog circuits**, which are more complex and underrepresented in radiation-hardened design flows.
- ✓ Introduces **AI-assisted design acceleration**, significantly reducing time to post-radiation evaluation and RHBD design.
- ✓ Provides a **complete two-step flow**: baseline radiation modeling followed by ELT-based hardening.
- ✓ **Eliminates need for fabrication**, enabling early validation through simulation.
- ✓ Fully **compatible with standard EDA flows**, ensuring practical integration in real-world design environments.

Conclusions

V. Gogolou, S. Karipidis, E. Papageorgiou, A. Michailidis and T. Noulis, "Radiation-Hardened—AI-Accelerated Custom IC Design Methodology," in IEEE Access, vol. 13, pp. 93869-93882, 2025, doi: 10.1109/ACCESS.2025.3574058.

- A holistic AI-assisted methodology is proposed for designing radiation-hardened analog circuits, essential for front-end radiation detection systems.
- The methodology uses a **Reinforcement Learning (RL) framework** to:
  - Seamlessly design an analog product vehicle
  - Generate the necessary component values for the CSA.
- Provides post-radiation assessments without requiring tape-out and physical measurements
- Enables **automated radiation hardening** by exploiting a pcell generator for **RHBD** cells to enhance radiation immunity.
- **Accelerates workflow** while maintaining or improving performance metrics.
- Offers a **highly efficient and reliable solution** for radiation-hardened analog circuit design.

Thank You!

Any Questions?