Closing the gap between Reliability Physics, EDA and Circuit Design

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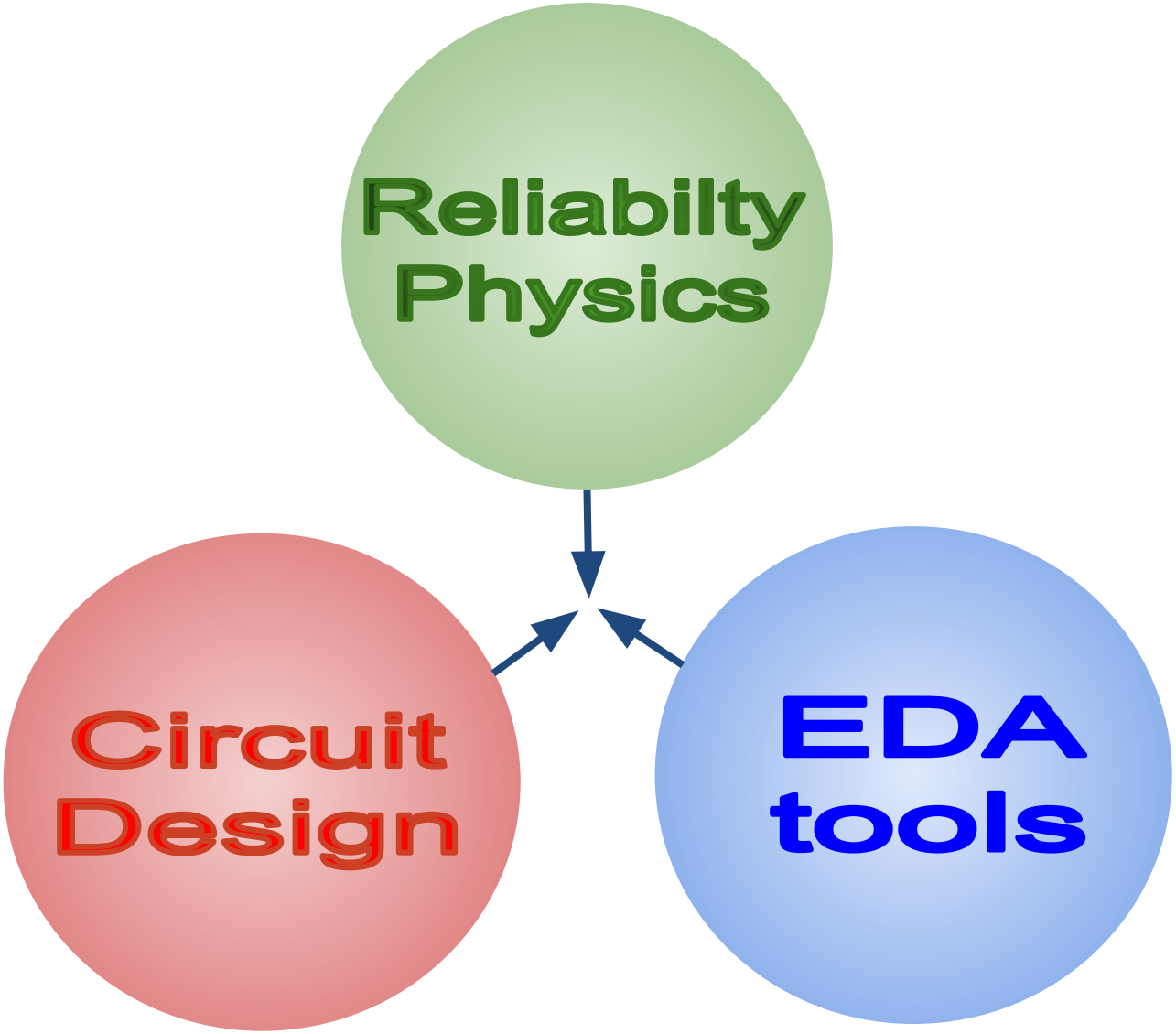
Purpose



Outline

- Introduction
- Main Reliability Degradation Mechanisms
  - Voltage, Temperature, Activity dependencies
- Impact on Circuits and Products
  - Reliability Circuit Analysis & optimization
  - Aging monitors
  - Adaptive techniques
  - HTOL Best practices
- EDA requirements
- Conclusions

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Introduction

- Accurate Circuit Reliability analysis is a must
  - Reduce design margins and time to market
  - Maximize product performance and reliability.
- Reliability specifications are typically based on DC measurements and certain Voltage, Temp
- Reliability analysis is very challenging due Voltage, Temperature and workload activity variations over the lifetime of the product
- Need very close cooperation amongst Reliability Physics, Circuit and EDA Experts

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Main Reliability Degradation Mechanisms

- **NBTI** Negative Bias Temperature Instability
- **PBTI** Positive Bias Temperature Instability
- **RTN** Random Telegraphic noise
- **HCI** Hot Carrier Injection
- **TDDB** Time Dependent Dielectric Breakdown
- **EM** Electromigration
- **SER** Soft Error Rate

Failure Mechanisms main Characteristics

- **NBTI** Vt increase, mobility decrease, PMOS -> speed degradation
- **PBTI** Vt increase, mobility decrease, NMOS -> speed degradation
- **RTN** Increases Vmin in SRAMs -> power impact
- **HCI** Hot Carrier Injection -> mobility decrease, NMOS-> speed degradation
- **TDDB** Gate oxide leakage-> affects functionality and can cause stuck at failures
- **EM** Can cause metal opens -> functionality failures
- **SER** Can cause wrong data storage

Reliability Mechanism Dependencies

	parameter	Temperature	Voltage	Recovery
NBTI	|VTH|	exp(-Ea/kT)	exp((VGS-VTH)/Tox)	partial
PBTI	|VTH|	exp(-Ea/kT)	exp((VGS-VTH)/Tox)	partial
RTN	|VTH|	exp(-Ea/kT)	exp((VGS-VTH)/Tox)	partial
HCI	Idlin	weak	exp(VDS) for Id>0	no
TDDB	MTTF (T63.2%)	exp(-Ea/kT)	exp(|VGS|)	no
EM	MTTF (T50%)	exp(-Ea/kT)	~V	partial
SER	SER	~T	~1/V	yes

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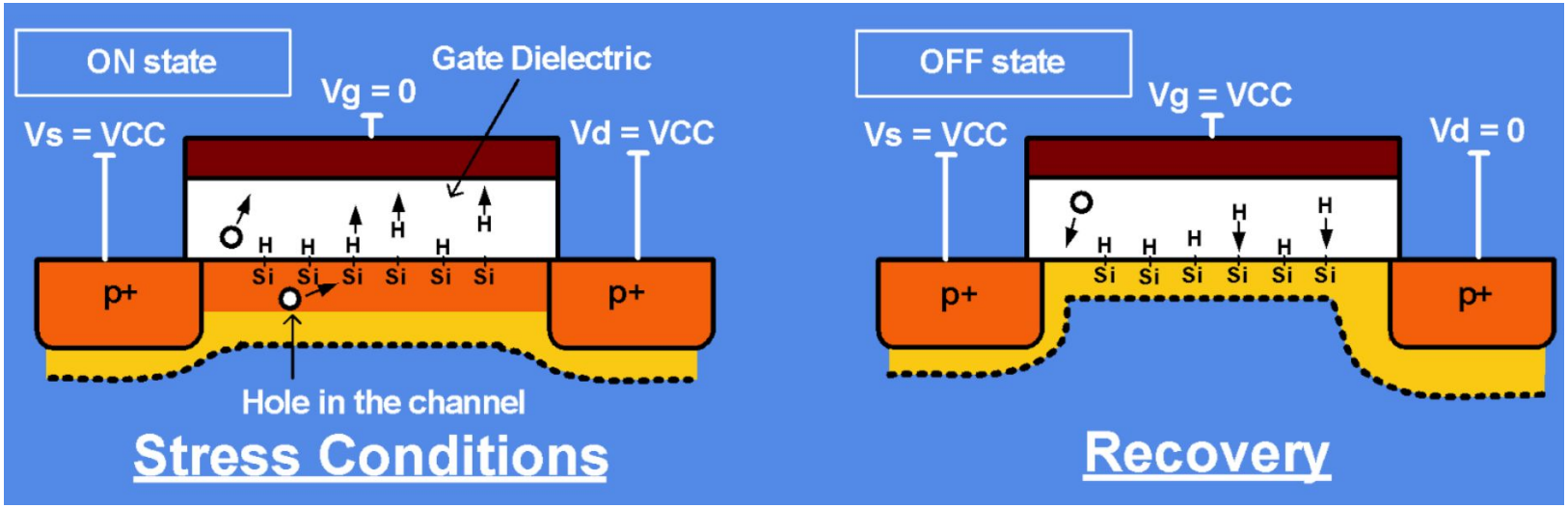
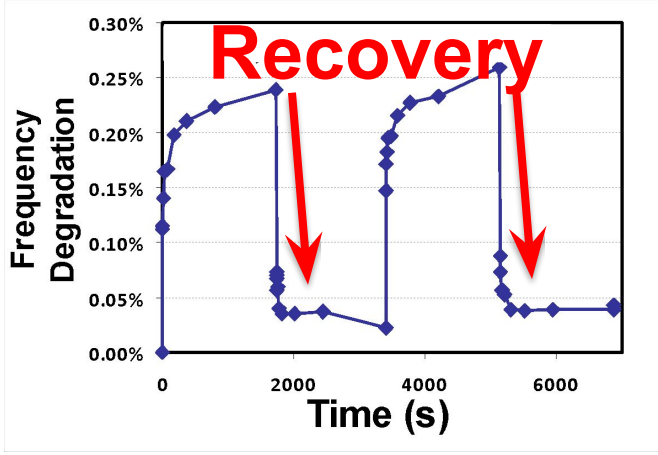
Introduction to NBTI



Keane, et al., VLSI Symp. 2009

- Channel holes interact with Si-H bonds at interface to create traps
- Increase in |Vth|
  - ~20-30% increase in 10 years
- Partial recovery occurs when PMOS is turned off



NBTI modeling

- Vth Degradation: Power Law Model

$$DV_{th}(t)=A*t^{n}$$

  - A: empirical constant. Depends on oxide thickness, electrical field, temperature
  - t: stress time
  - n: 0.13…0.25, process dependant

- Vth relaxation: Reaction-Diffusion/ Trapping-Detrapping model

$$DV_{th}(_{relaxation})/DV_{th}(_{stress})= 1-\exp(-(t_{relaxation}/C)^{b})$$

  - b = 0..1, typically 0.5
  - C: relaxation time constant that is process, voltage and Temperature dependent.

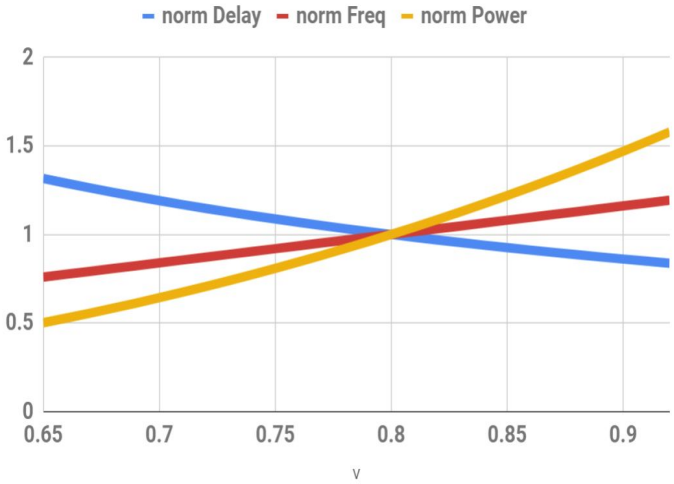
Tibor Grass et al IRPS 2007

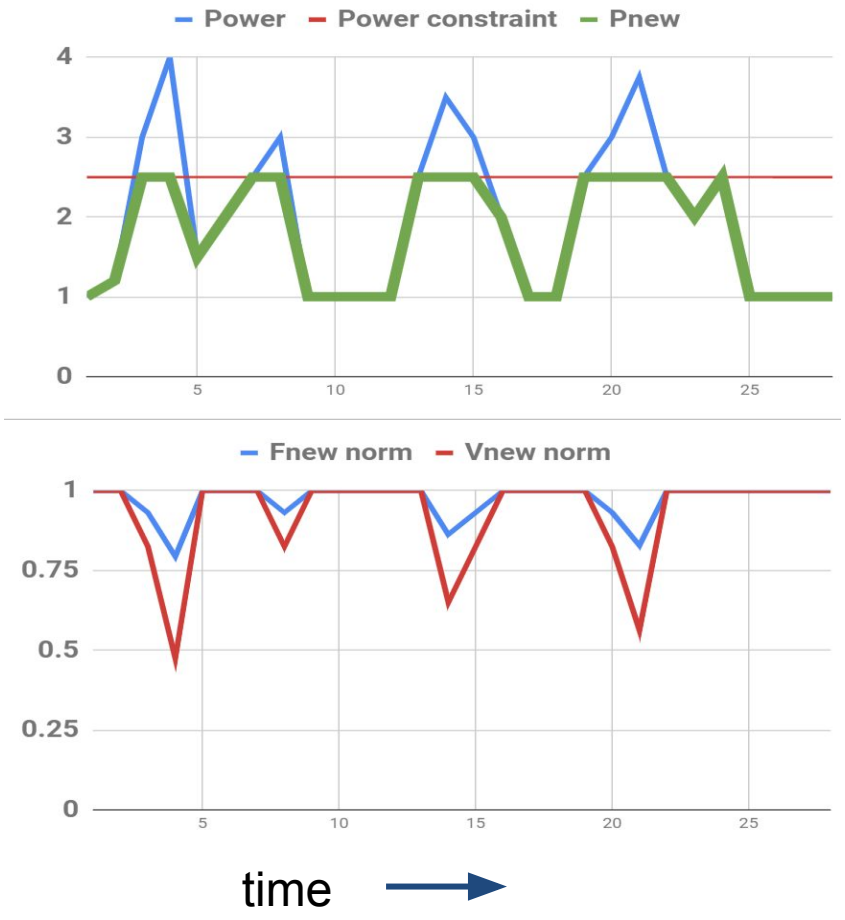
NBTI, PBTI - Workload Dependency

- Workload dependency (activity).
  - Need to account for Temp, Voltage, activity, time between activations
- Watch out for:
  - Nodes that are stuck for long time will have permanent stress with no chance for recovery
  - Clock network, clock gaters
  - SRAMs, RFs

NBTI, PBTI and DVFS

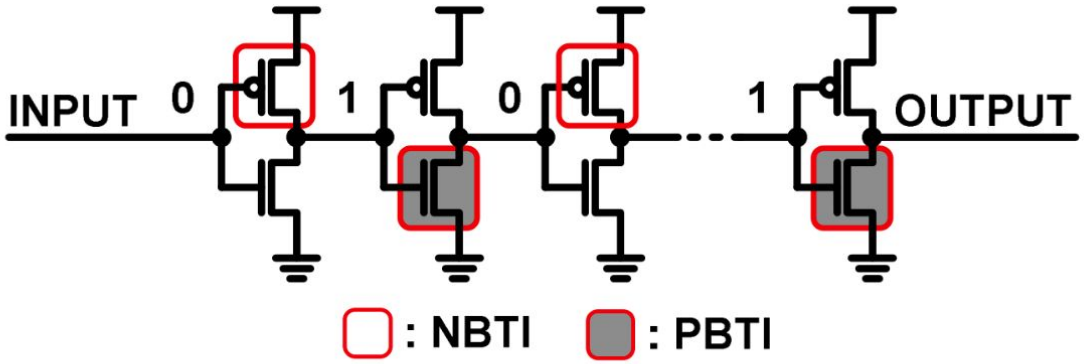
- Continuous Voltage, Frequency change

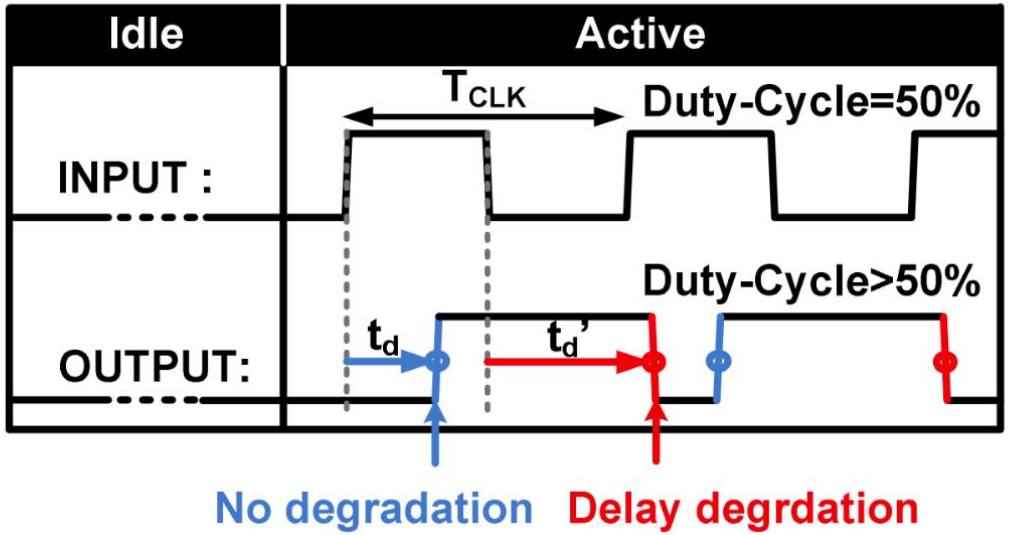




PBTI stress conditions
vary substantially over time

NBTI, PBTI - Asymmetric Stress





Wang et al, IRPS 2013

NBTI, PBTI - Asymmetric Stress

- Asymmetric stress in clock network during HTOL will create duty cycle distortion.
- Need to make sure clock is free running for balanced stress.
- Duty cycle distortion can create timing violations in double pumped SRAMs that use both the rising and falling edges of the clock

NBTI, PBTI- Impact on Timing analysis

- Effect on multi Vt optimization for timing paths
  - High vt paths need to have more slack due to larger sensitivity to low voltage
  - Need to account for mismatch between the various transistors and the different rate of variation due to NBTI
  - Need to account to the different behavior with Temp inversion
  - Vt optimization to reduce power need to account for different margin per transistor type and target voltage
  - Larger devices will have less variation (RSS) but will lead to higher power

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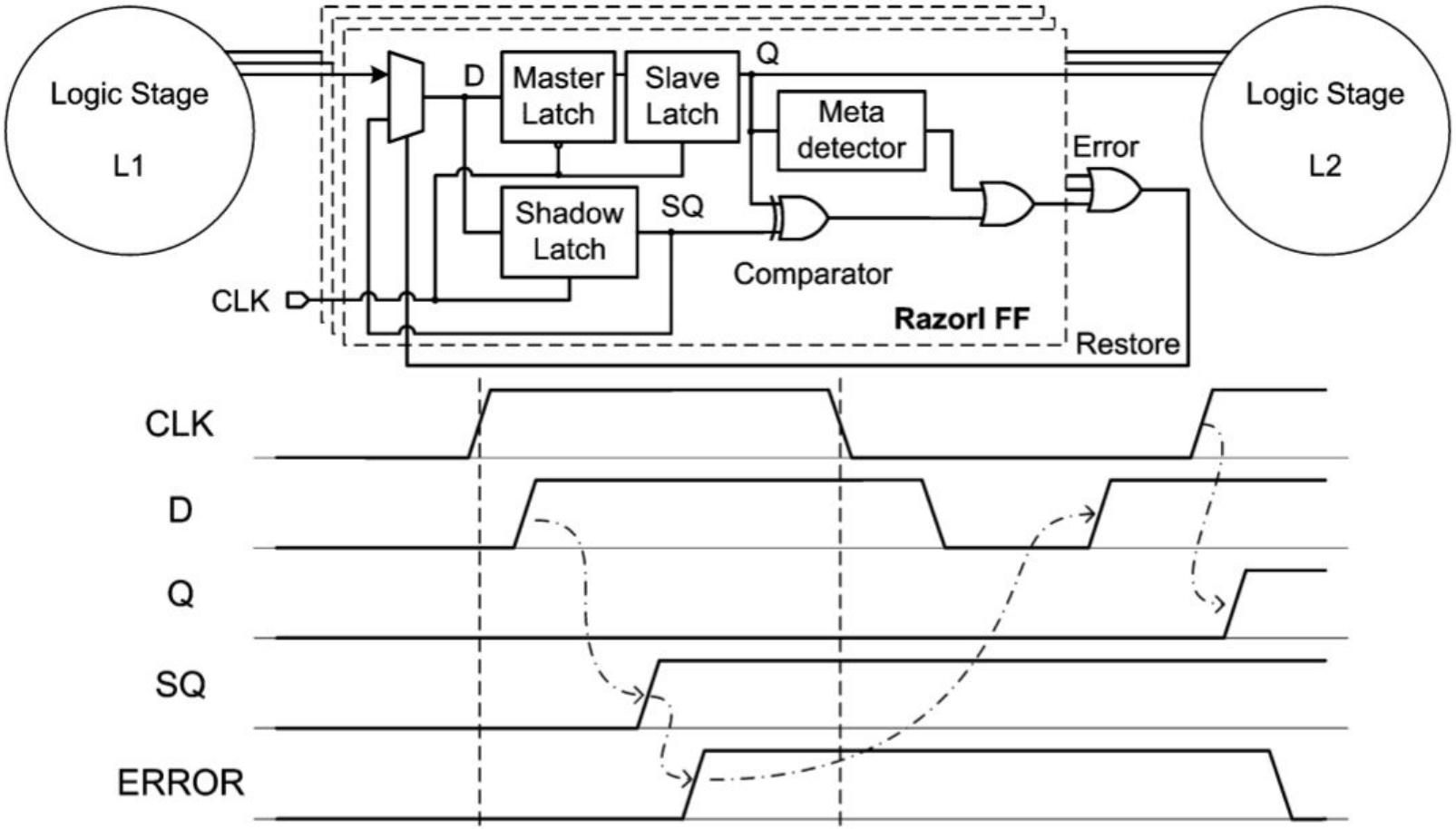
Razor I - Timing Margin Check



Das, et al, JSSC 2009

NBTI degradation detector and early warning system

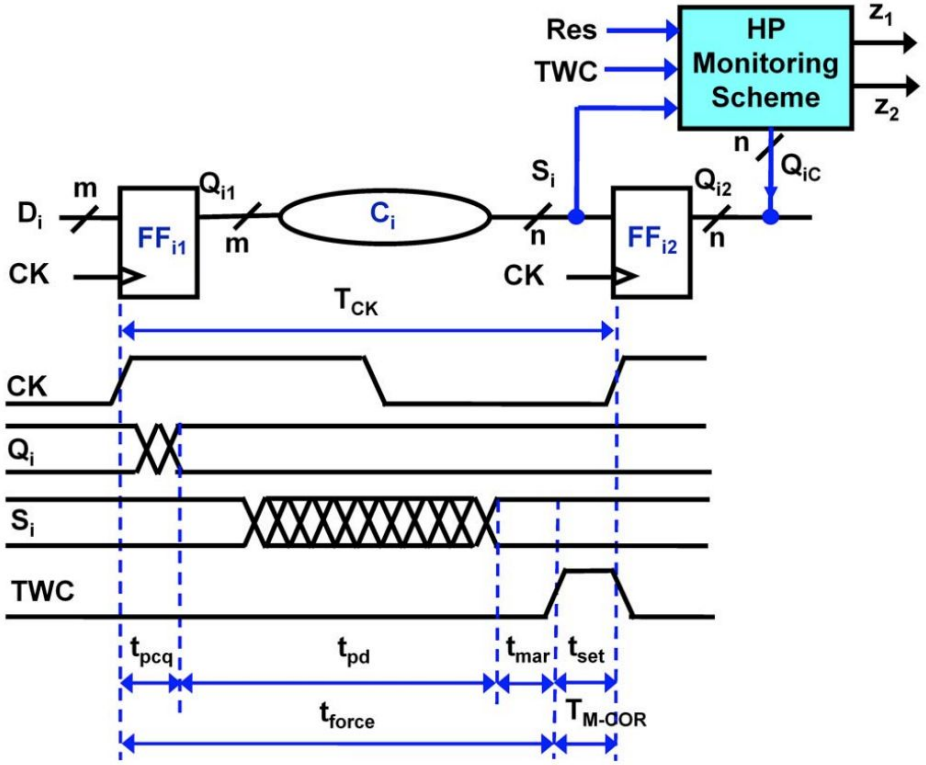


Fig. 11. HP monitoring scheme insertion within the considered critical data paths.

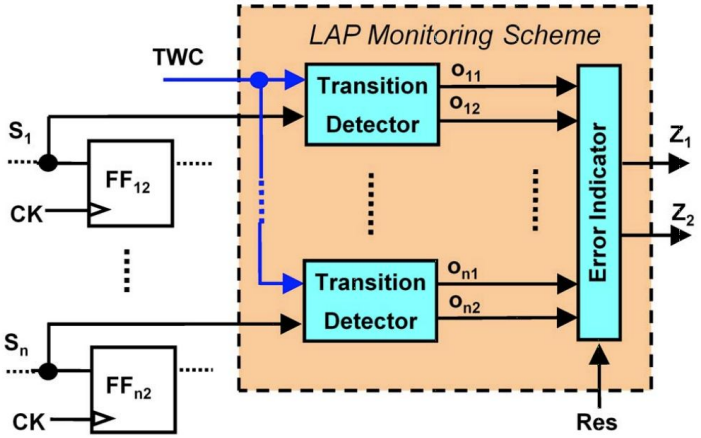
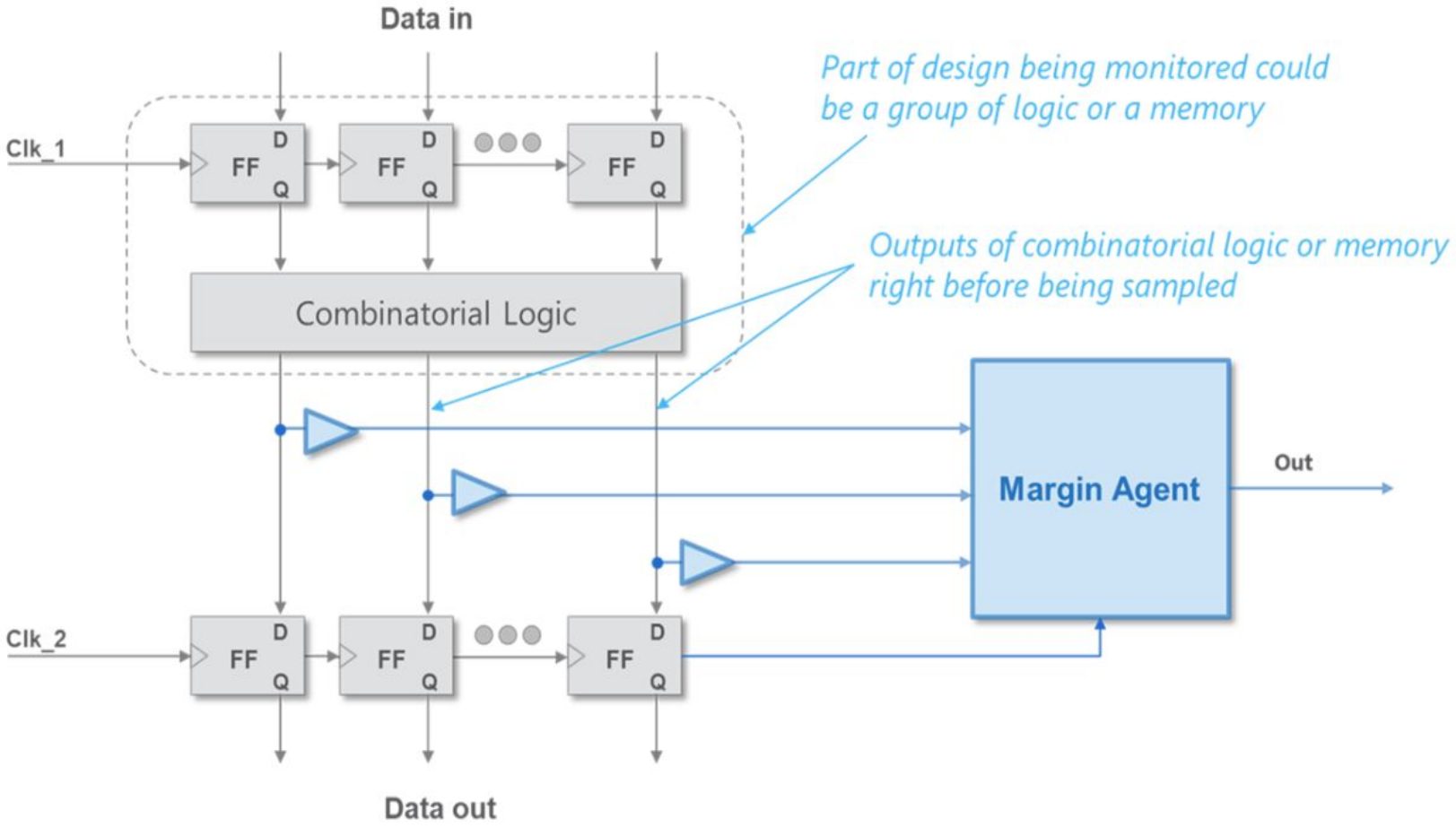


Fig. 3. LAP monitoring scheme internal block structure.

Omana et al, Trans. on Computers, 2013

Aging Monitors as IP



ProteanTecs, Landman et al, IRPS 2019

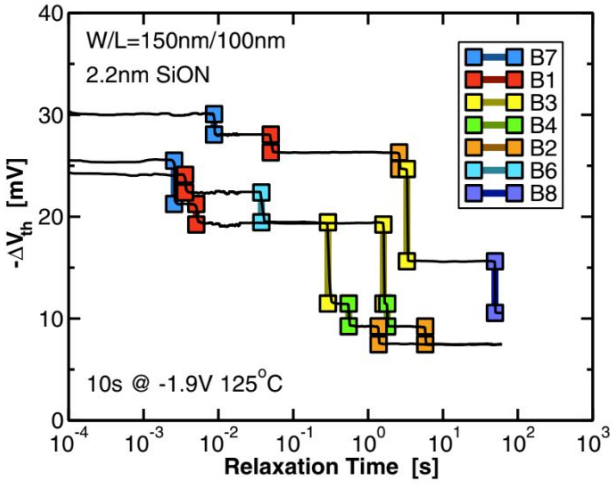
NBTI, PBTI - EDA Requirements

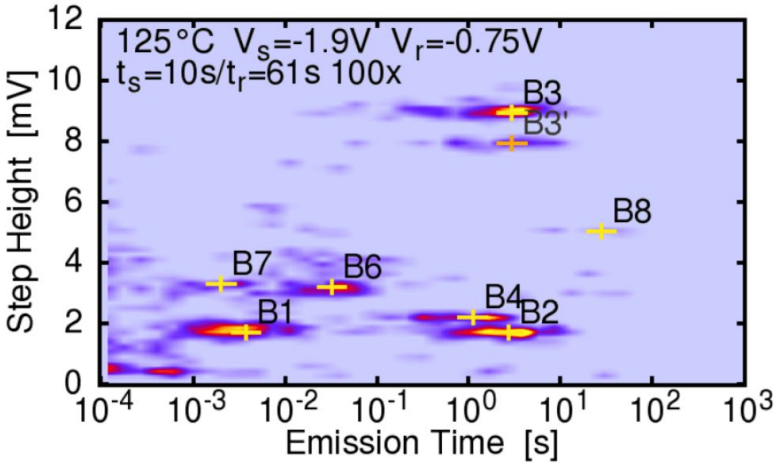
- EDA requirements, std lib char
- Library characterization pert VT type vs Voltage, Temp
- Thermal maps for various workloads
- Node activity
- Time spent at each bias condition
- Need macromodels for fast simulations based on pre-characterized std cell library
- Cannot rely on spice sims at large scale but only for the cell characterization

RTN basics

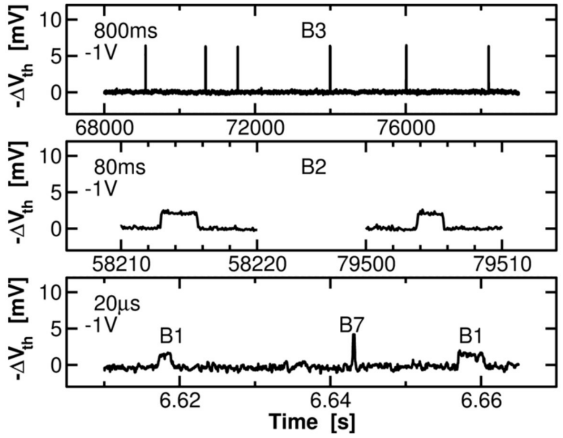
- Random Telegraphic Noise (RTN)
- “pop-corn” noise in audio devices
- Vt fluctuation over time due to defect charge trapping - detrapping at various time constants.
- Discrete events at small devices
- 1/f noise in larger devices

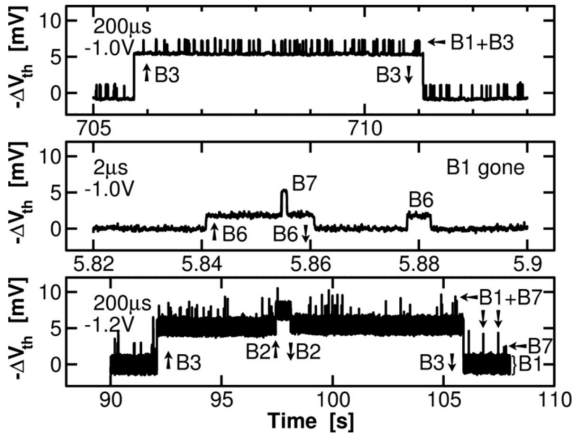
RTN, NBTI Unified perspective





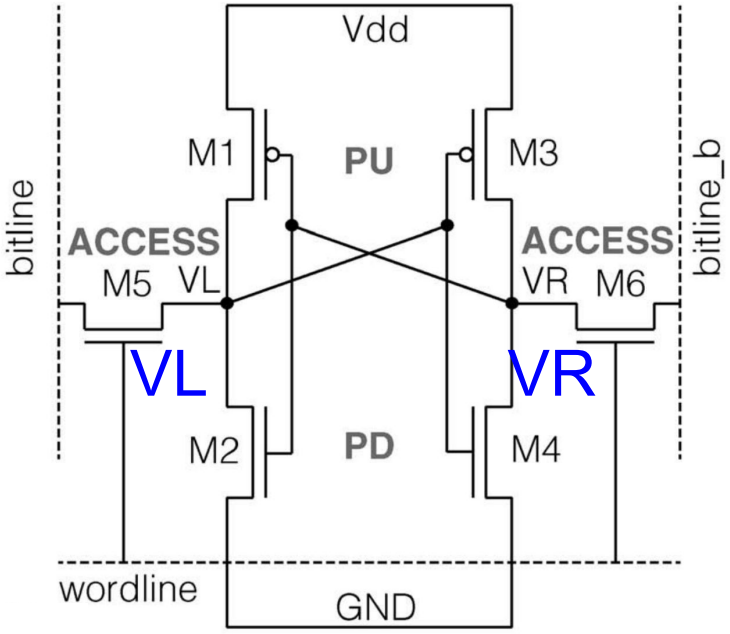
Grasser et al. IRPS 2010, 2014

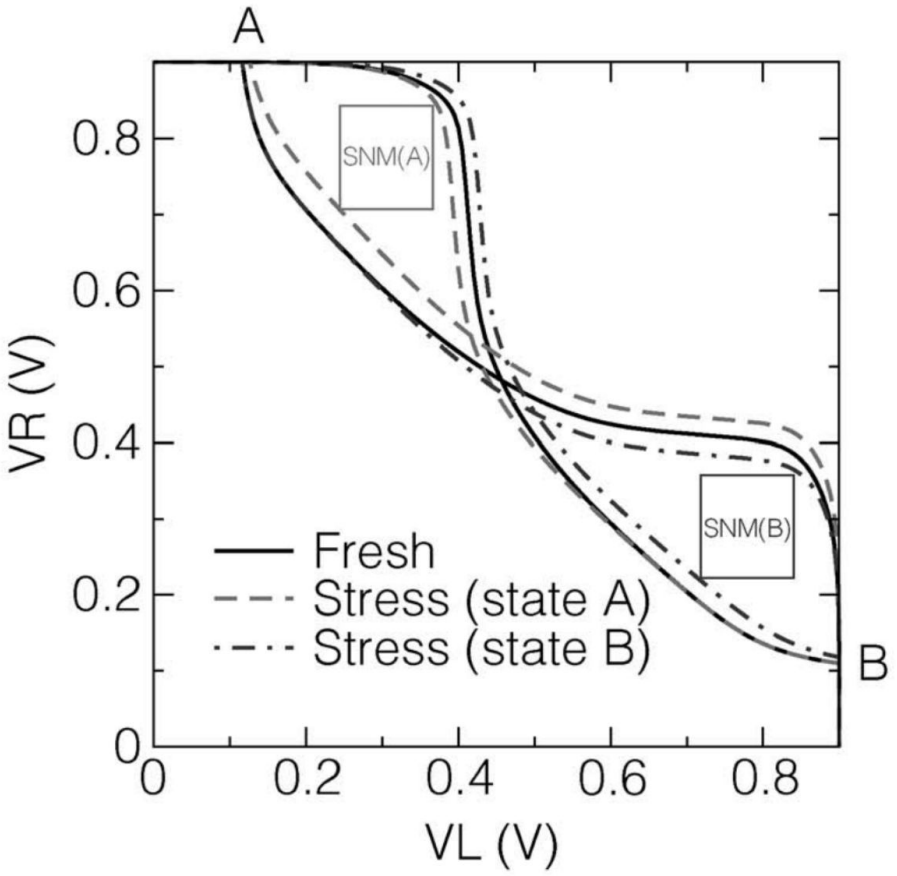




By using different sampling rates it can be shown that all defects identified during NBTI recovery also produce RTN..

NBTI, PBTI Impact on SNM





Wand et al, IEEE Design & Test 2013

NBTI & RTN Impact on SRAM Vmin

- Reduces the effectiveness of low power techniques by not allowing supply voltage reduction beyond a limit imposed by SRAMs
- SNM estimation in SRAMs calls for 6 sigma analysis
  - Results depend on the size of the Array
  - Bit repair capability through e-fuses
  - Cell size
    - Arrays built with larger cells have lower Vmin

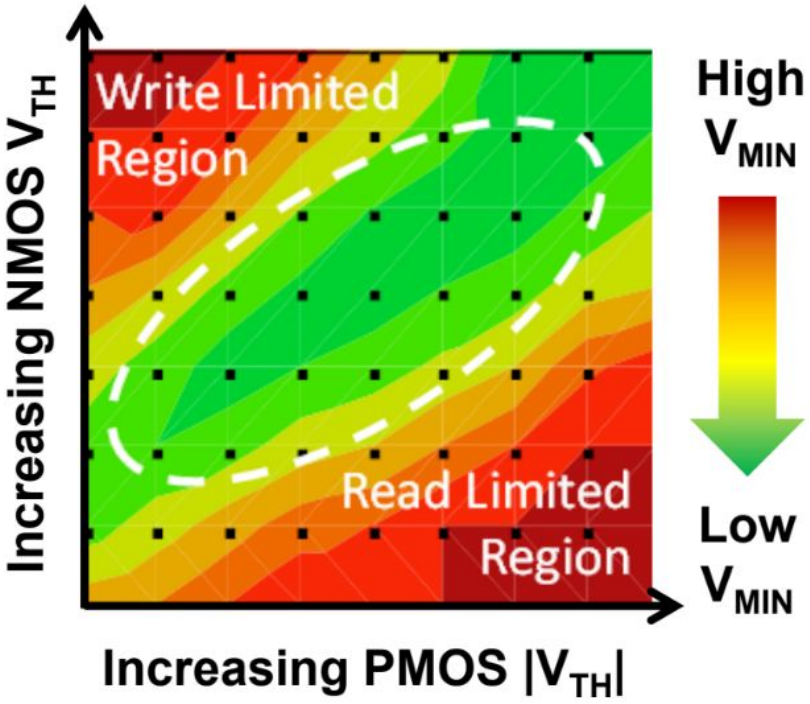
Vmin Mitigation Techniques

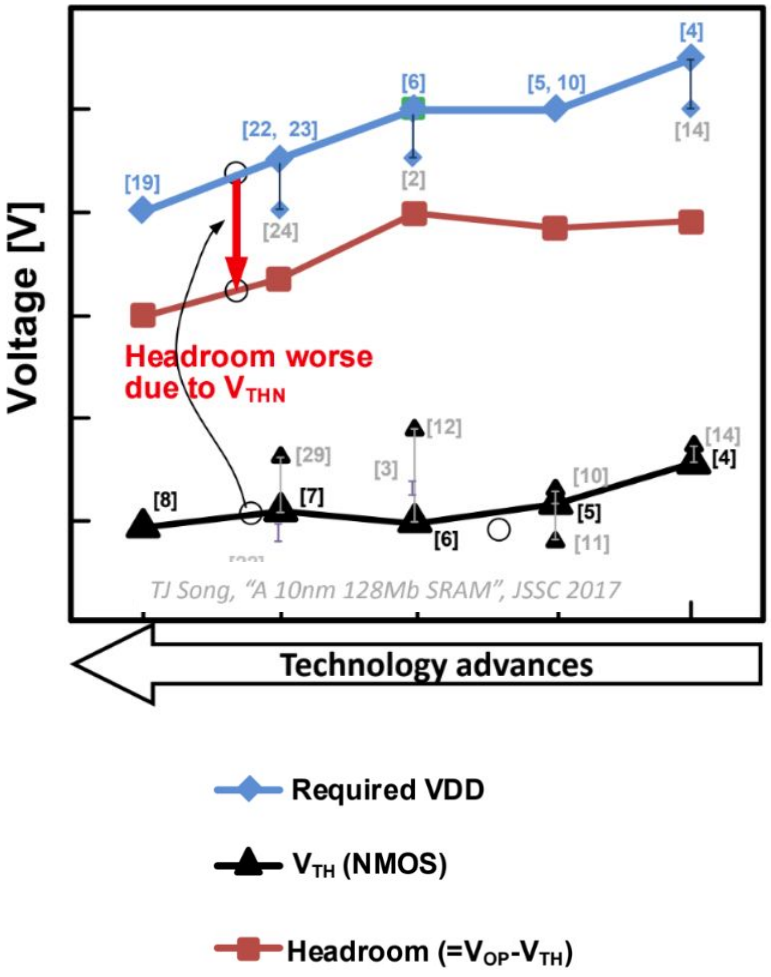
- Separate power supply for the SRAM bits
  - layout overhead, Power Grid integrity Degradation
- Weak bit repair
- Column/Row repair.
  - Overhead, degradation over time,test escapes,
- Line Retirement
  - Software controlled
  - Requires continuous monitoring

Vmin Mitigation Techniques (cont'd)

- ECC (Error Correction Code)
  - Area/circuitry overhead
  - Depending on implementation can provide single bit detection or single bit correction and double bit detection etc
- Write or read assist circuitry
  - Reduces Vmin by more than 100-200mV
  - Facilitates reads & writes by manipulating the transistor strength through dynamic voltage modulation
  - Comes with area overhead, circuit complexity

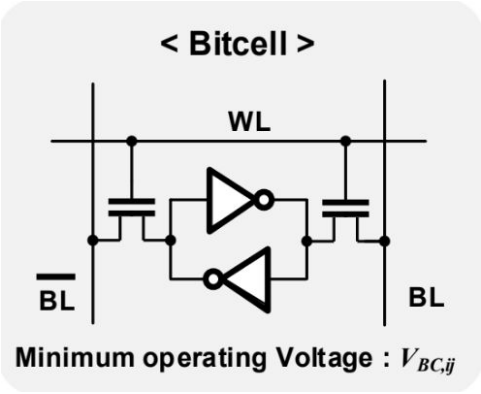
SRAM Write and Read Margins

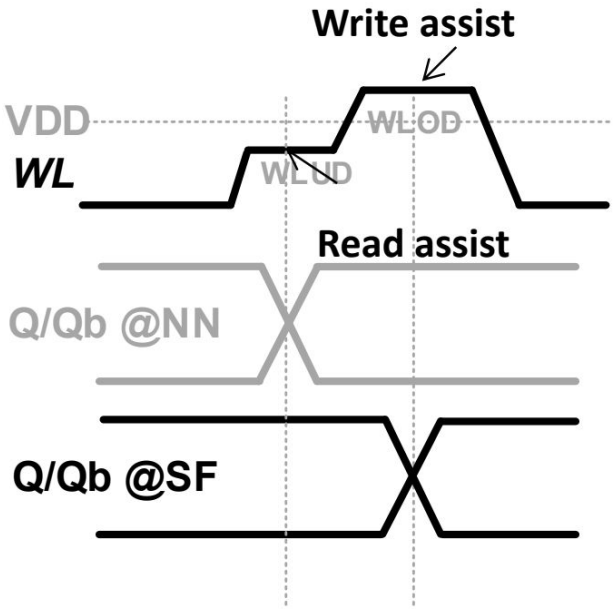




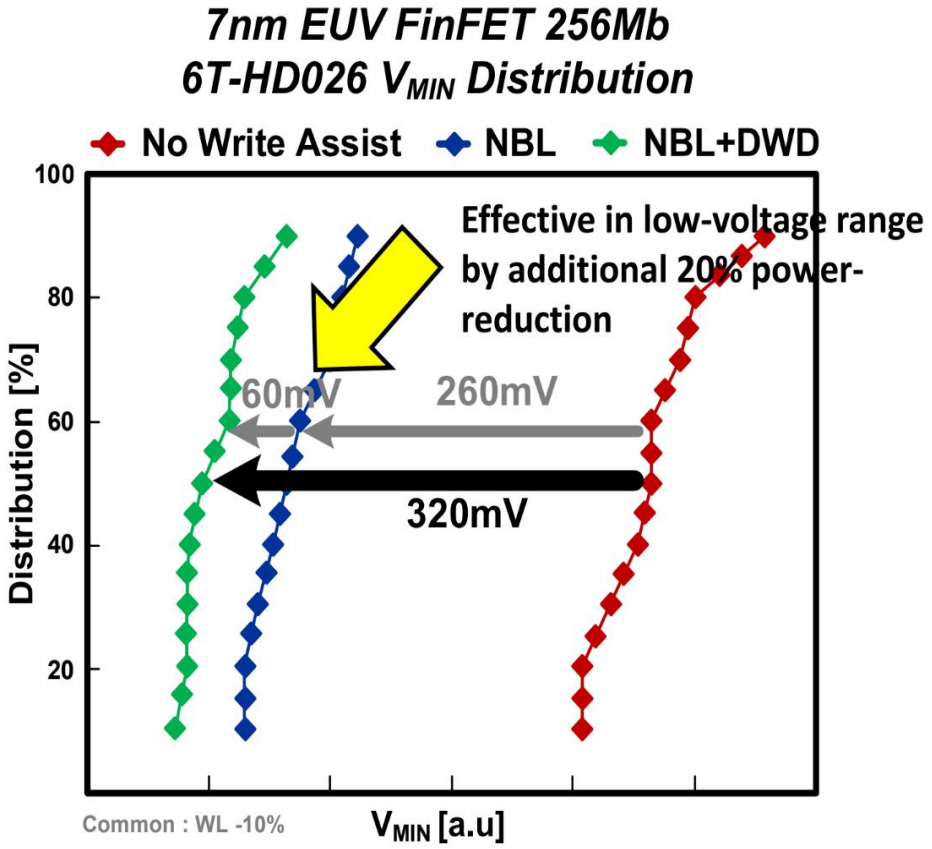
Guo et al, ISSCC 2018

Write and Read Assist



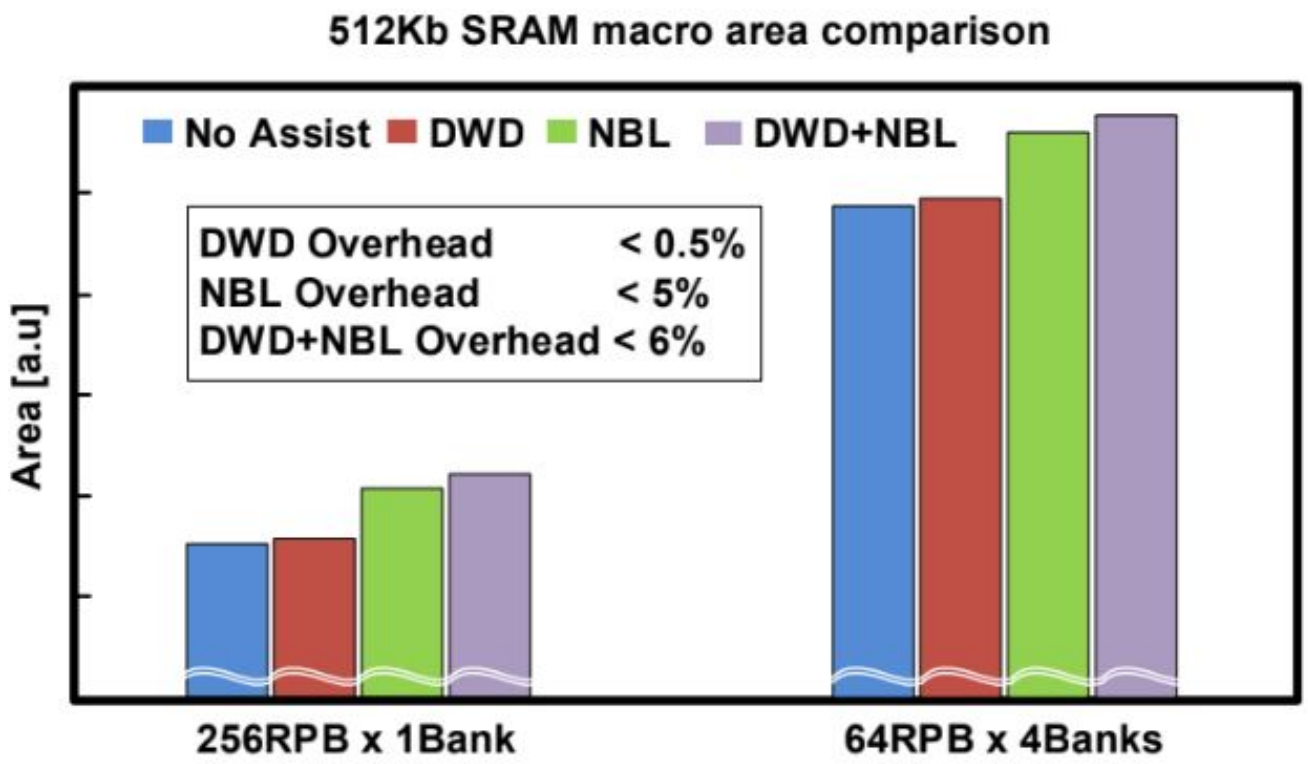


Song at al, ISSCC 2016



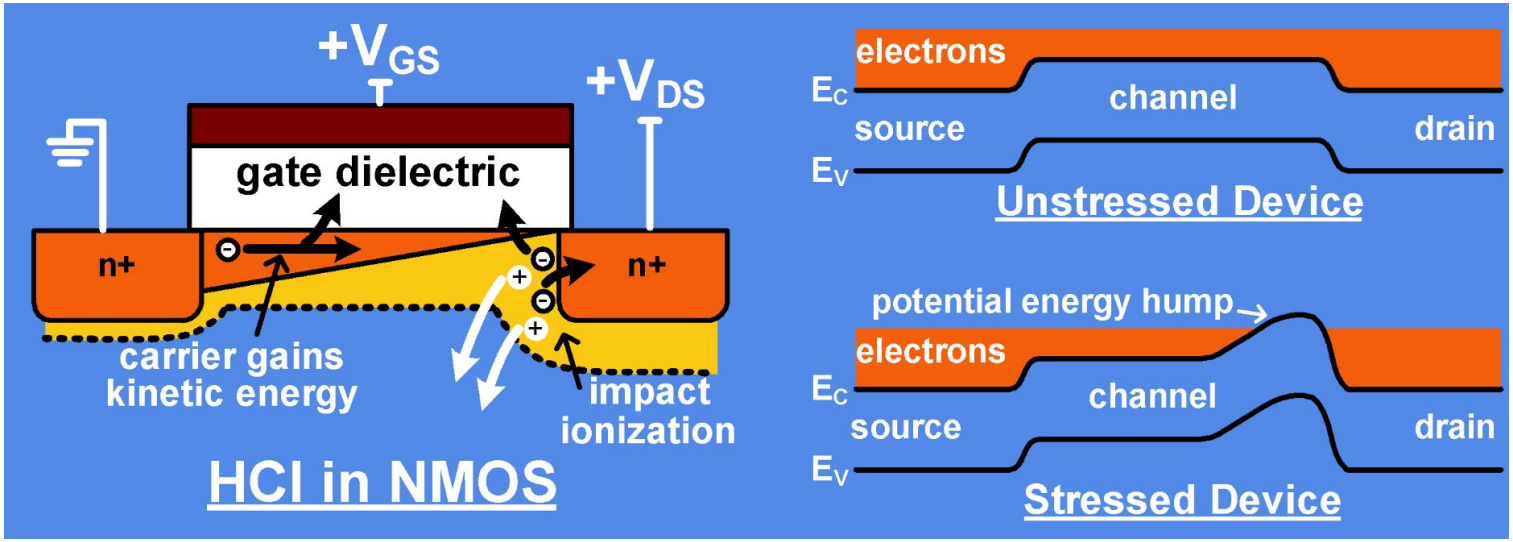
Song et al, ISSCC 2018

Assist Circuitry Overhead



Song at al, ISSCC 2016

HCI basics



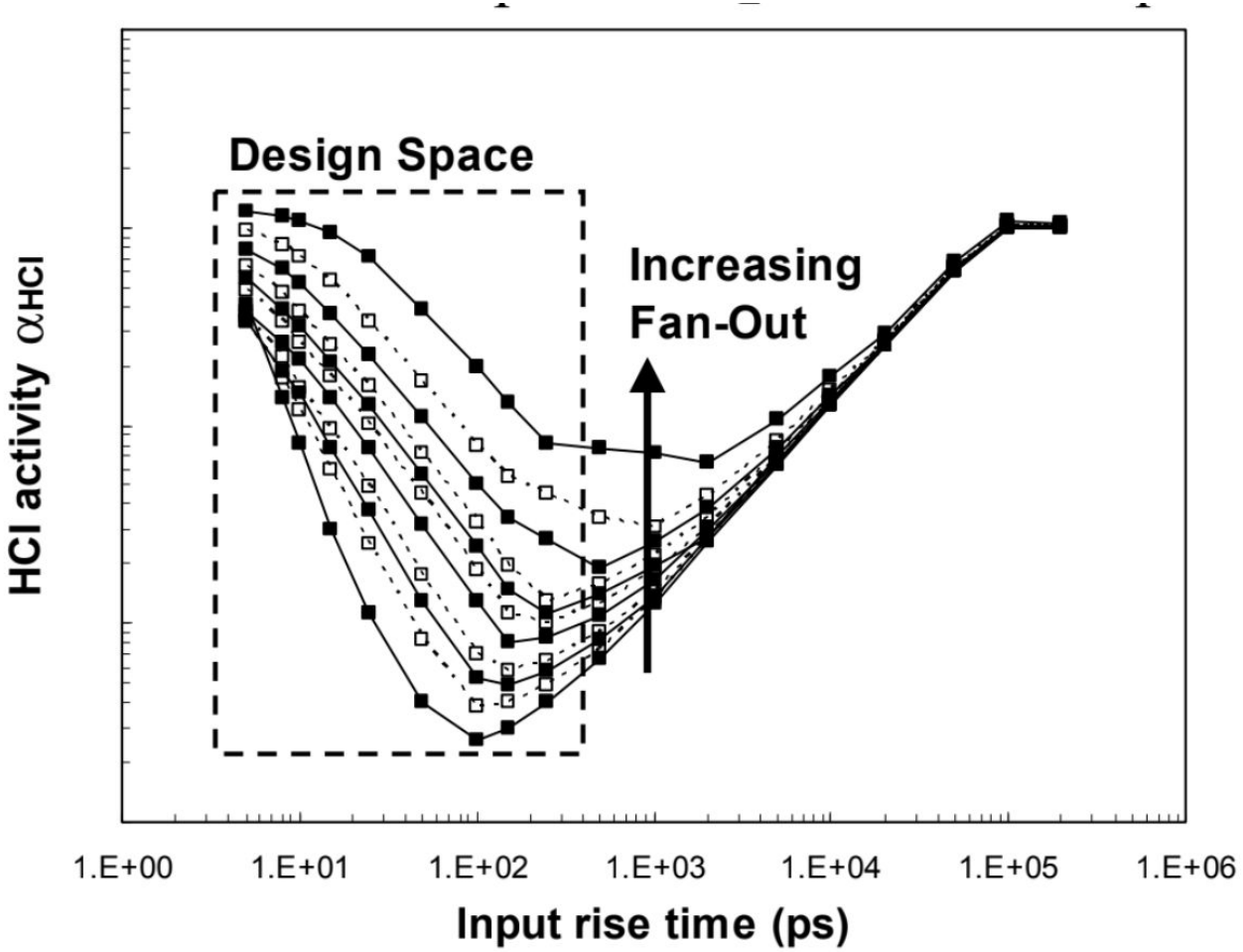
Keane, et al., VLSI Symp. 2009

- Causes degradation of gate dielectric Interfacial and oxide traps
- Negatively trapped charges create potential hump
- Degradation not reversible

HCI Impact on Circuits

- HCI is predominant in NMOS devices since electrons can be accelerated faster than holes and require lower energy to cause impact ionization.
- The degradation will be proportional to the VDS value over time and while there is drain current
- Large VDS and high current flow will exacerbate this effect.

HCI Dependency on Input Slew Rate and Fan-out (Load)



Huard et al, IEEE 2012

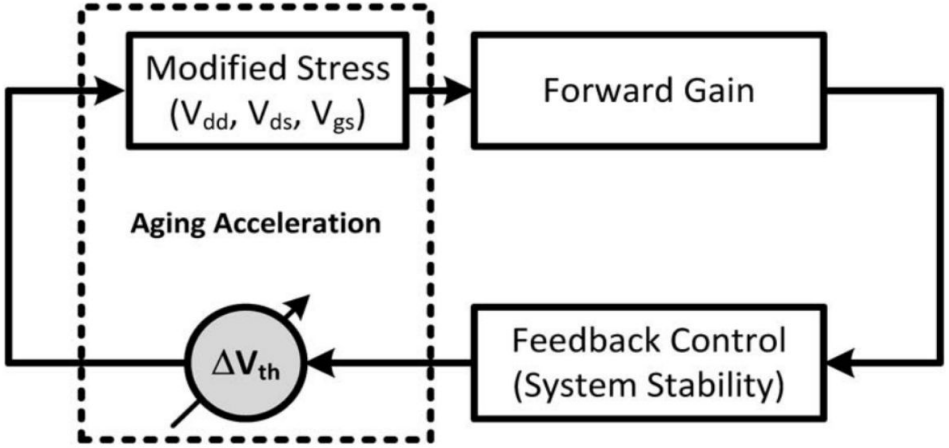
HCI EDA requirements

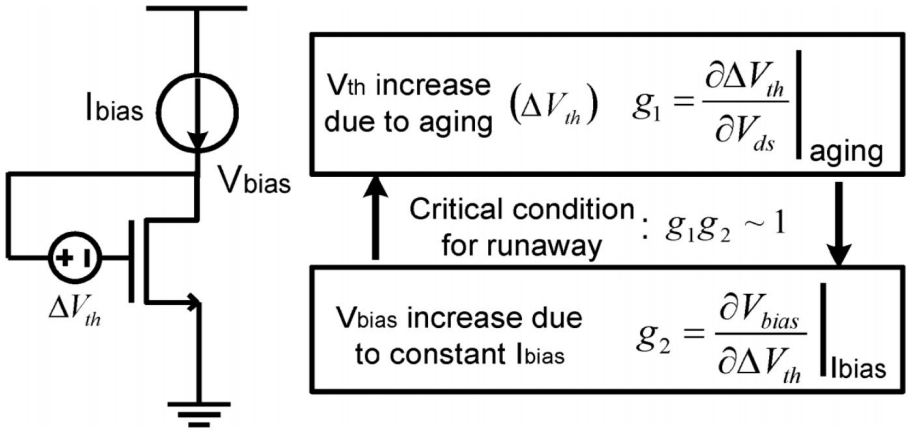
- Need information on the switching activity over time
  - Back annotation from gate level simulations for a wide range of workloads
- Need information on the magnitude and duration of the switching drain current
  - This is the same information used in the EM flow
  - Alternatively, knowing the slew rates at the output of each gate and the Ceff load one can easily calculate the switching current for a fast evaluation
    - Back annotation from STA analysis

Analog Circuits Reliability

- Potential run away in feedback control loops
  - Critical mission applications, medical, automotive
- Need symmetrical biasing in sense amplifiers to avoid offset
  - make sure symmetrical stress is applied in standby mode as well
- Amplifier degradation, CTLE offset
- Duty cycle distortion
- Serdes BER degradation
- PLL, DLL jitter degradation

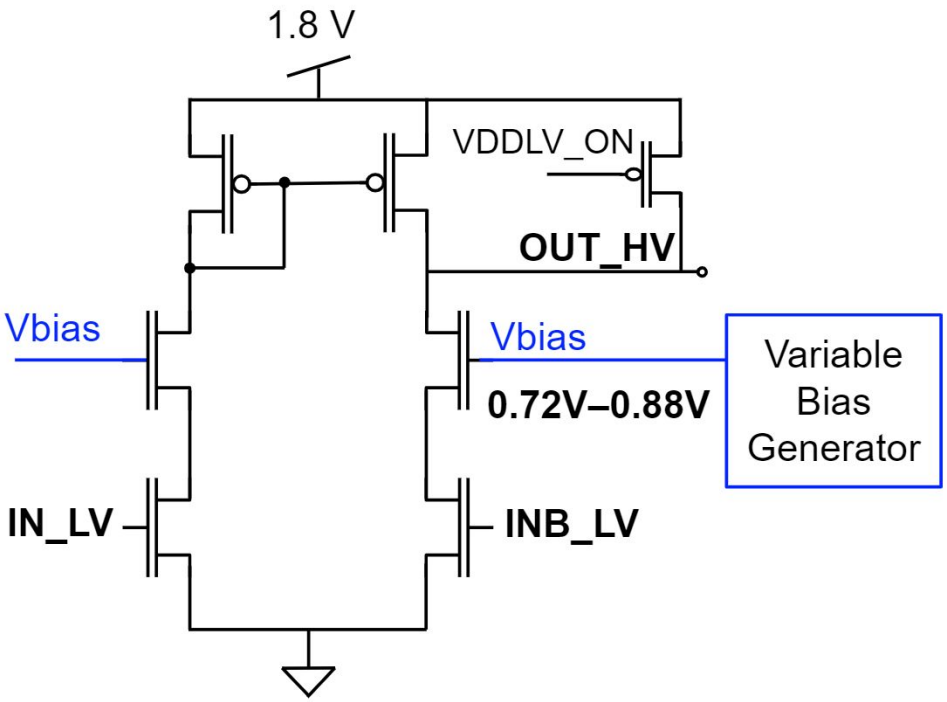
Run-Away in Feedback loops





Sutaria et al, IEEE Trans on Material and Devices, Sep 2015

Impact on 5Gbs LVDS

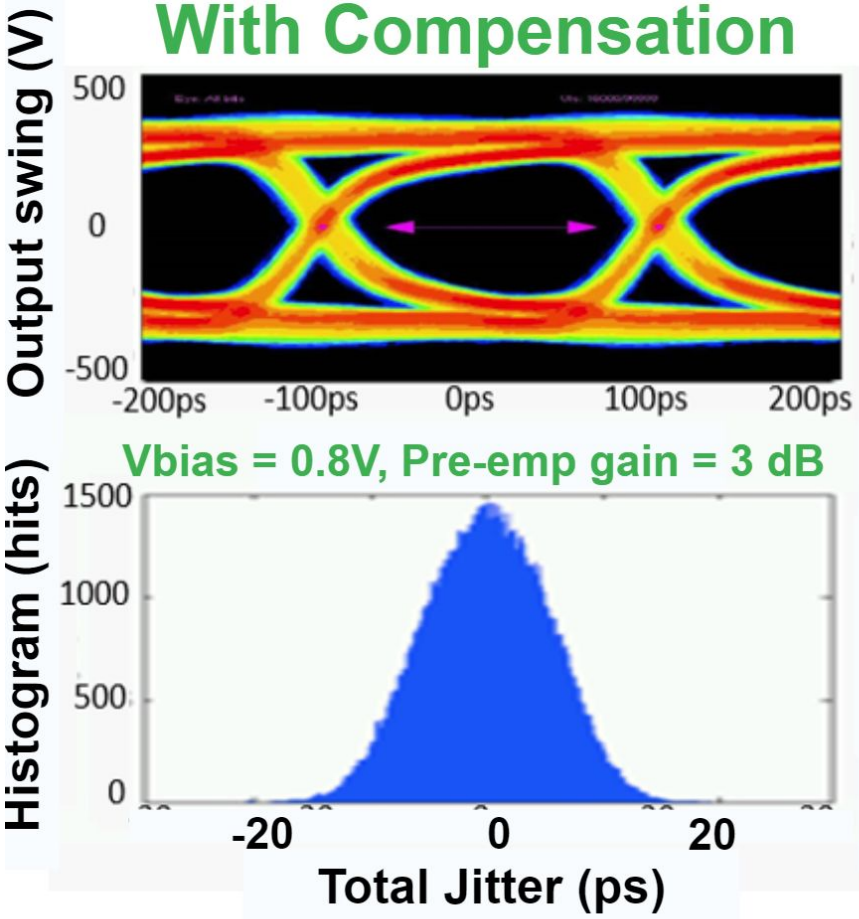


- **Constant Vbias replaced by variable DC bias**
- **Vbias can be selected to compensate for V_{TH} @ PVTs or aging degradation**
- **Duty cycle can be measured on-chip to and automatically adjust Vbias**
- **Without the compensation, the circuit failed after HTOL. The compensation scheme managed to restore functionality**

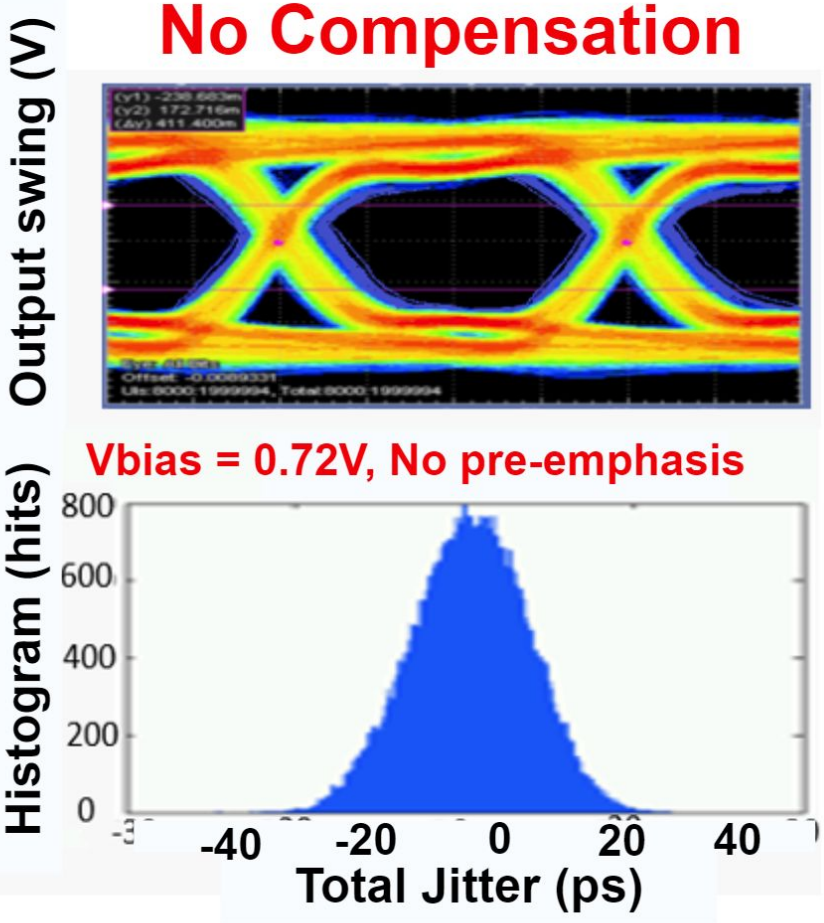
Jagannathan et al, IRPS 2018

Aged with/without Compensation

With Compensation



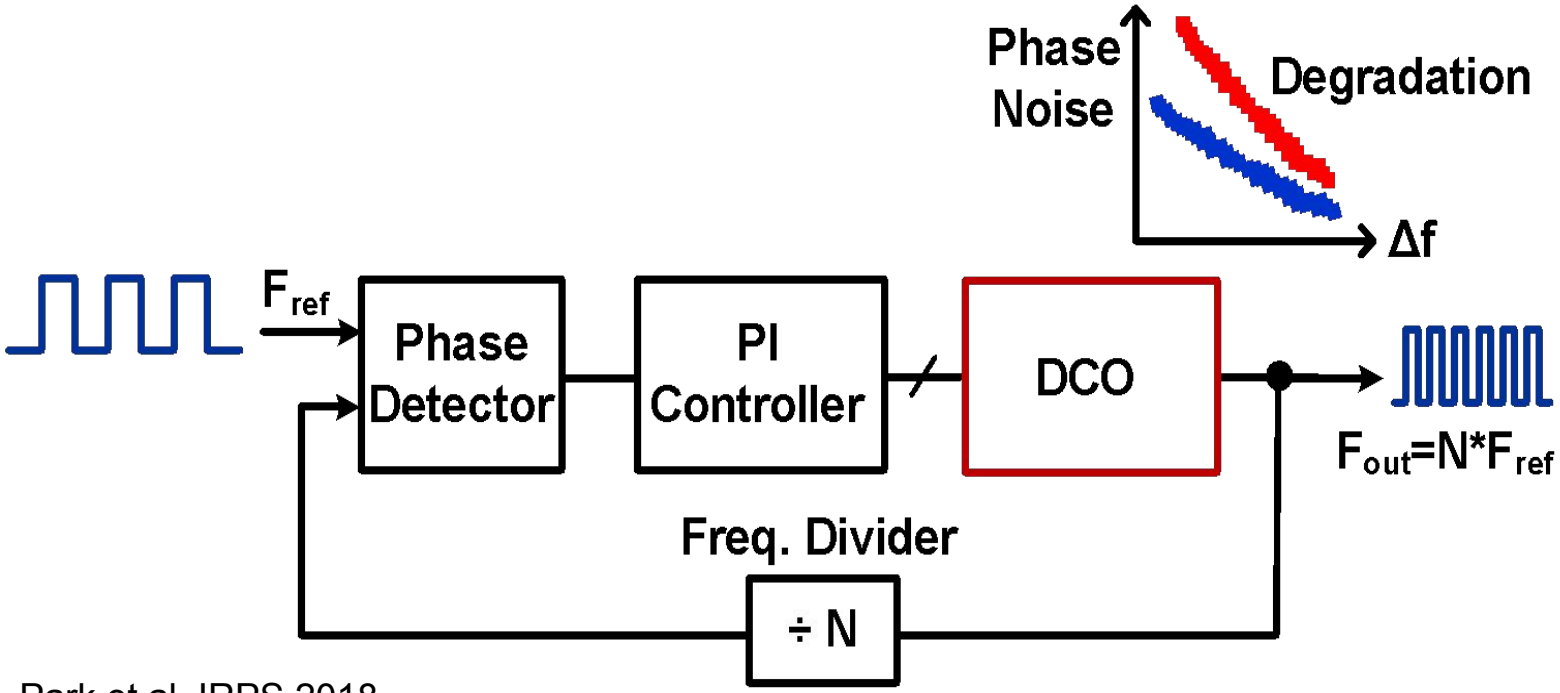
No Compensation



- **Vbias and pre-emphasis gain increased from 0.75V and 1dB to 0.8V and 3dB to compensate for aging induced degradation**
- **Able to achieve output swing, jitter & duty cycle well within specs**

Jagannathan et al, IRPS 2018,

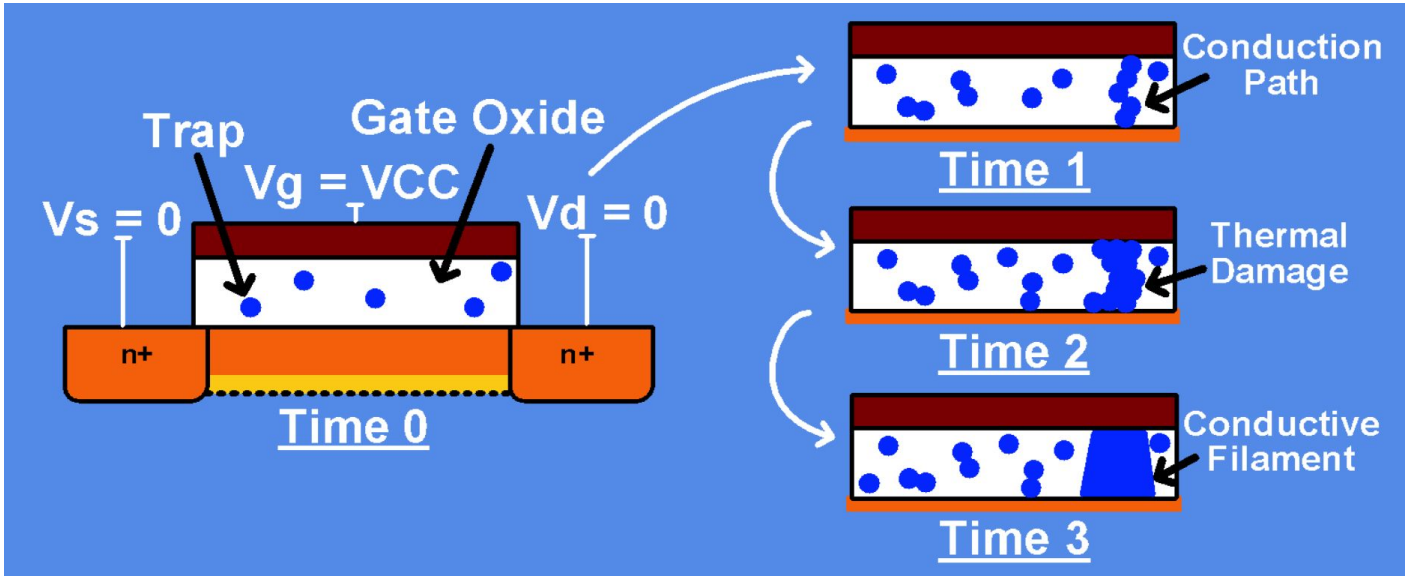
ADPLL Reliability - Impact on Jitter



Park et al, IRPS 2018

- **Aging affects jitter and reduces design margin**
- **Jitter measurements requires high speed probes or packages, off-chip drivers and connectors**
- **On chip degradation monitor provides higher jitter measurement accuracy**

TDDB basics



Keane, et al., VLSI Symp. 2009

- Traps generated under influence of electric field
- Traps overlap
  - Conductive path between gate and substrate
- Gate dielectric no longer a reliable insulator
  - Parametric or functional failure

Reliability Circuit Analysis & optimization

- TDDB defines the max supply that can be used for a product.
  - Need to know the total gate oxide area and the voltage and Temperature conditions over time
- The Ldi/dt effect also has impact on the the GOI margin.
  - Need to be able to monitor or predict the voltage overshoots and make sure we have enough margin for EOL.

Reliability Circuit Analysis & optimization

- DFVS limitation on the high and low side of the Voltage Supply range
- Need to be able to monitor the V, F pairs over time and predict the aging profile
- Need good control of loadstep
  - Current step/ramp up time control through u-Arch
  - Decoupling capacitance on board and the package
  - Active Ldi/dt control for fast loadsteps

Power Delivery Network (PDN)

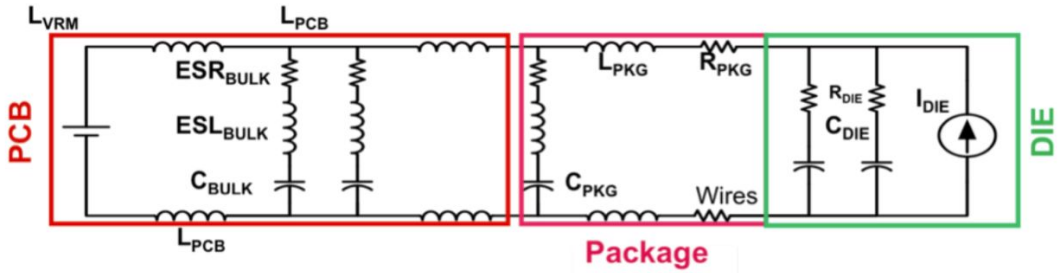


Figure 1. Simplified PDN model showing the Chip, Package and PCB components

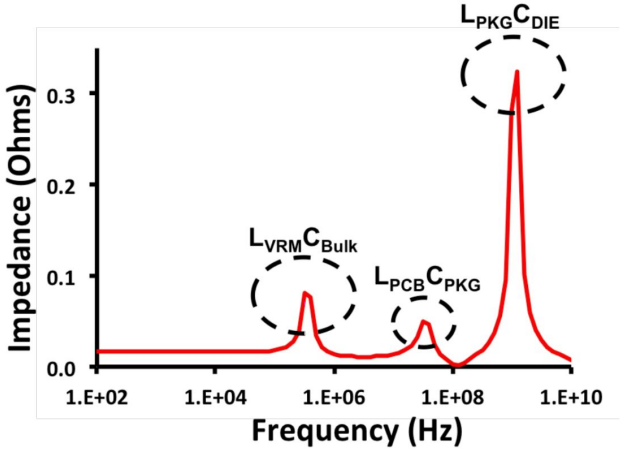


Figure 2. Frequency Response of the simplified PDN. The dominant resonance frequencies are labeled against their impedance peaks [6].

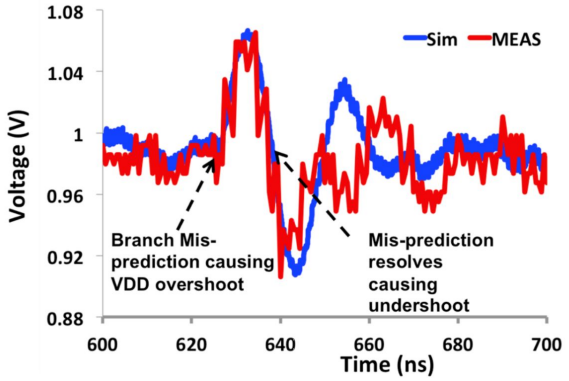


Figure 15. Time-domain simulated and measured waveforms showing PDN response to a branch-misprediction induced voltage overshoot.

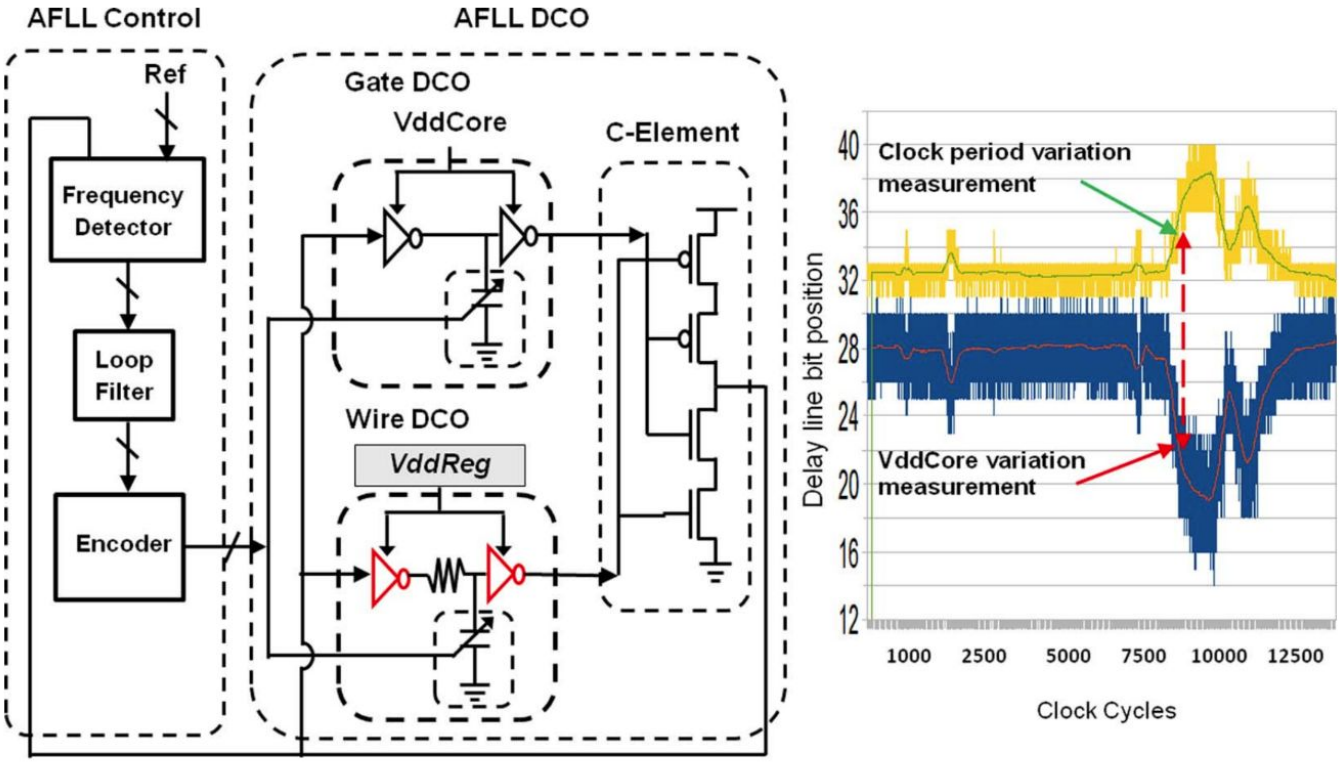
- Depending on the workload variations it can create voltage undershoots or overshoots

Das et al, ISLPED 2015

PDN impact on TDDB, Vmin

- Depending on the workload variations it can create voltage undershoots
  - timing failure issue due to low voltage at transistor
  - This will require to add margin to Vnom and burn more power for ever
- Overshoots can create GOI, TDDB issues and limit the max voltage
  - This will limit the max voltage we can use
  - Will the max performance we can achieve
- **Ldi/dt mitigation is a must**

Ldi/dt droop mitigation- FLL
(Frequency Locked Loop)

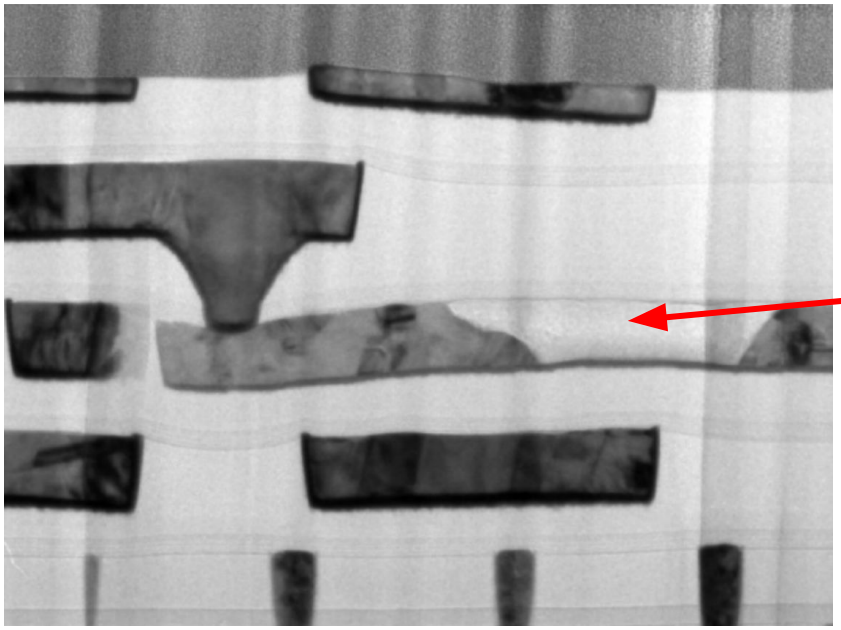


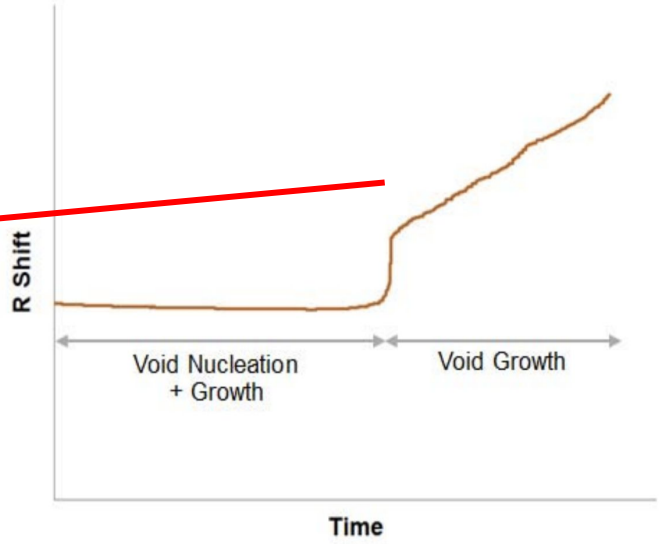
AFLL block diagram and Ldi/dt compensation.

- Reduces clock frequency temporarily when a sudden VDD droop is detected.
- Undershoot would have been 2x larger without the FLL mitigation

Konstadinidis et al, JSSC 2016

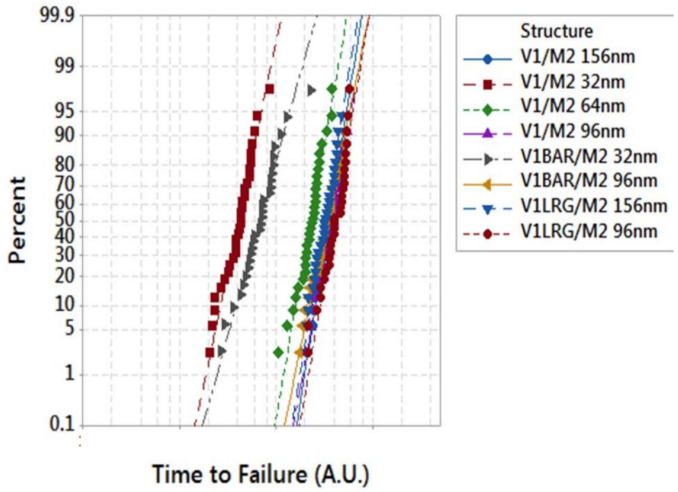
EM Failure Mechanism

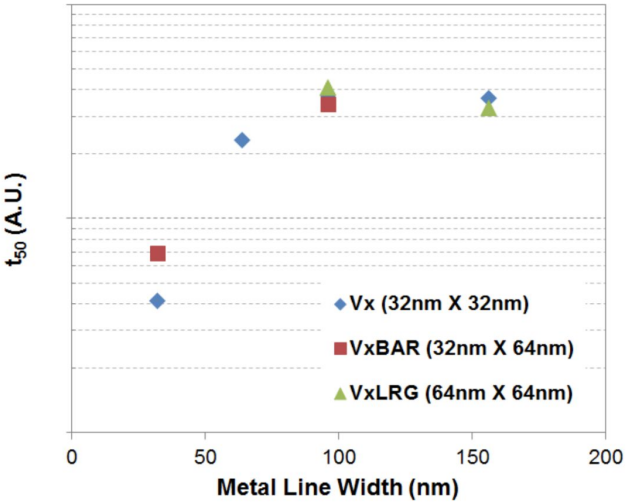




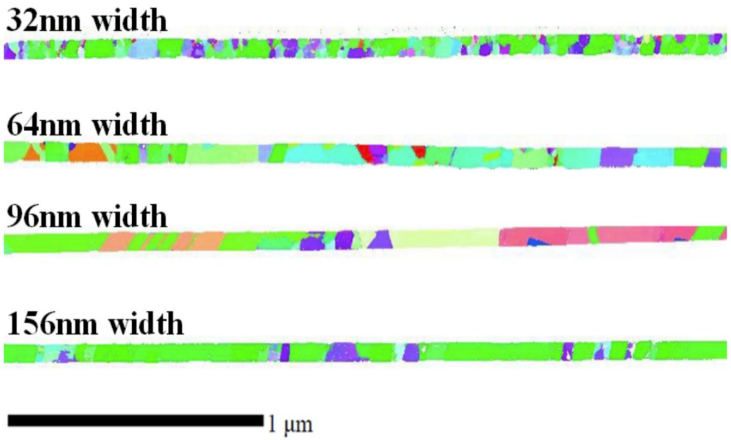
Choi,et al, IRPS 2018

EM failure vs Metal Width, Grain Size





- EM improves for up to 3x increase in width and then saturates.
- Strong dependency on the grain size and Cu drift velocity

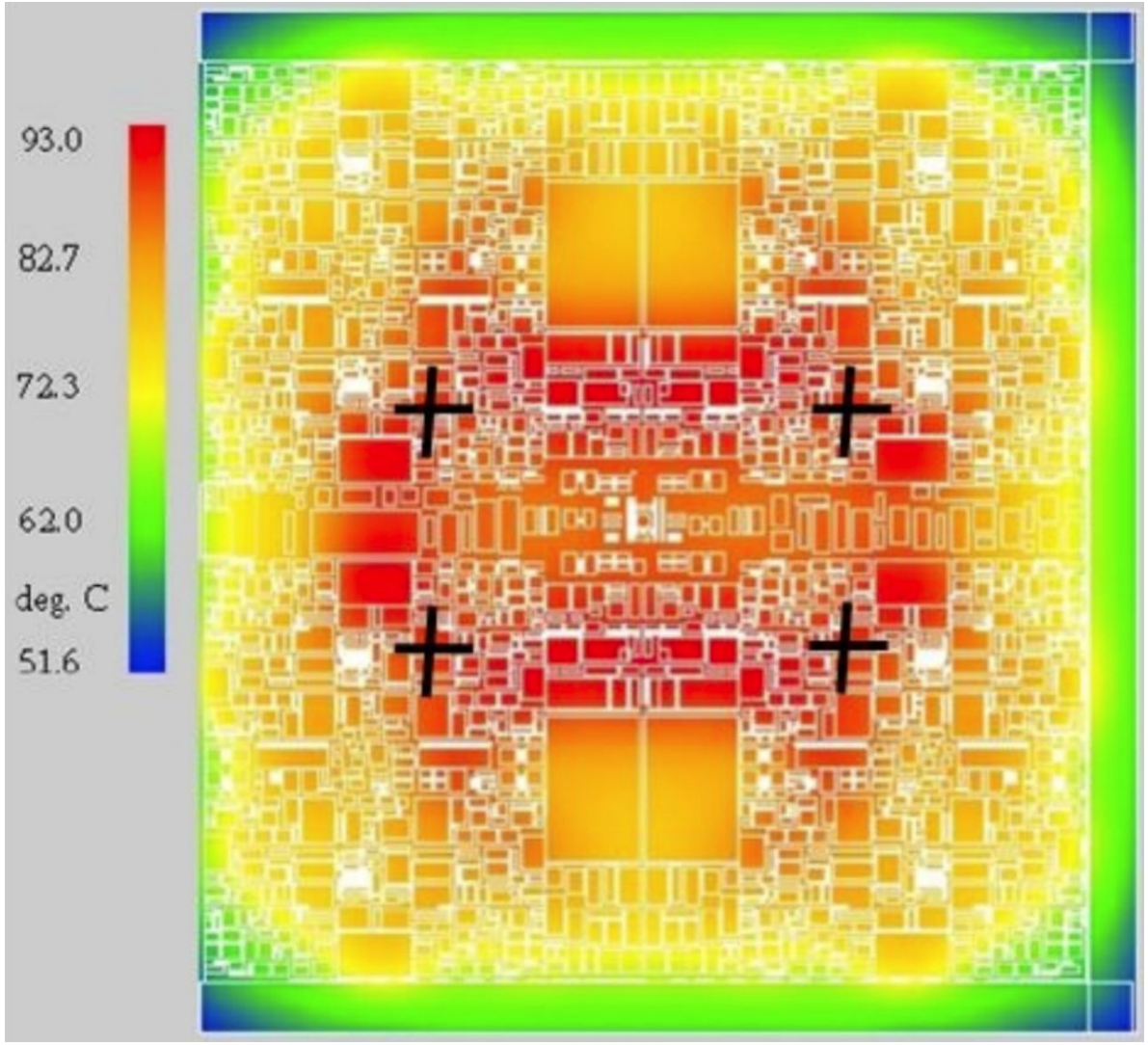


Choi,et al, IRPS 2018

Electromigration

- EM rules are based on DC measurements
- During the design phase one needs to take into account the activity, slew rates, thermal maps, self heating, and AC recovery to capture accurately the circuit degradation.
- Need Thermal maps, and Temp assigned to each wire segment of the same net

Thermal Map



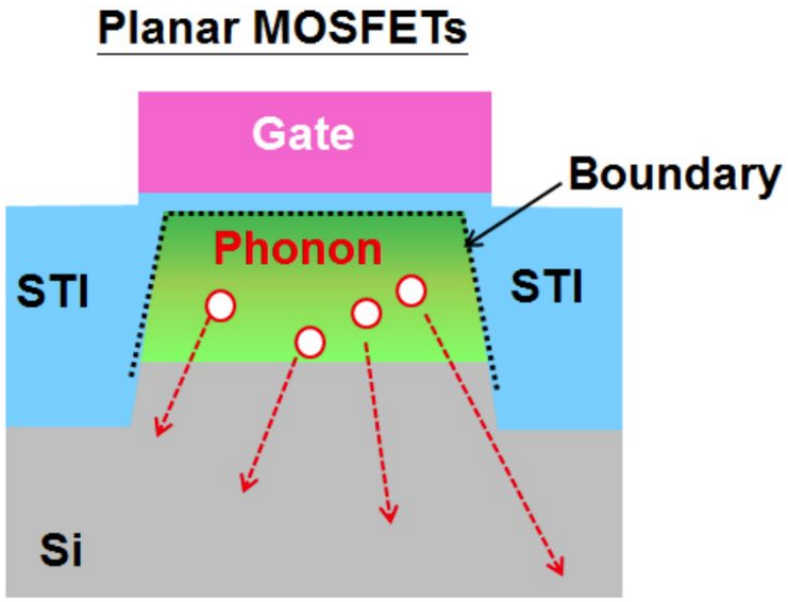
Konstadinidis et al, JSSC 2009

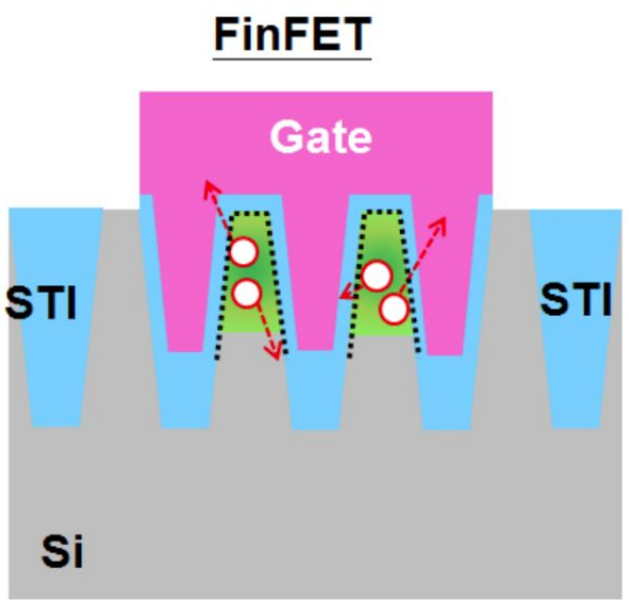
Electromigration

- Need to perform activity analysis
  - workloads to get good coverage, achieve robustness, and reduce pessimism
- Self heating in FinFET.
  - Impact of neighboring FinFEts, wires.
- Take advantage of Short Length rule relaxation
- Optimize the standard cell library design and via allocation. How pessimistic?
- Via Pillars for current redistribution
  - Impact on area, cell library pin access

Self Heating Effect (SHE) in FinFET

- Heat is carried out by phonons
- Phonon travelling is controlled by boundary scattering



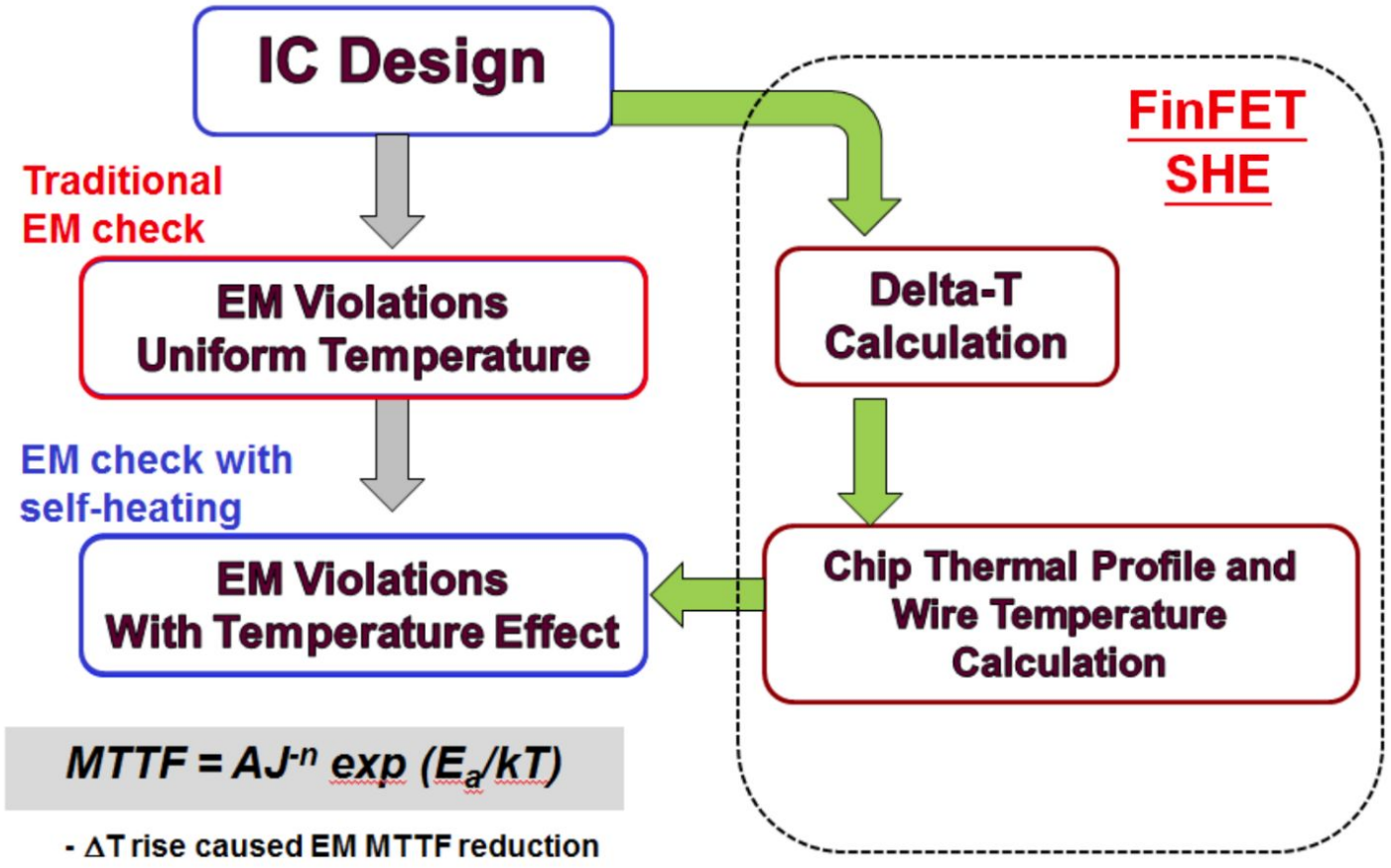


- λ of phonon ~ 300nm @RT
- Less self-heating

- λ limited by structure
- Self-heating

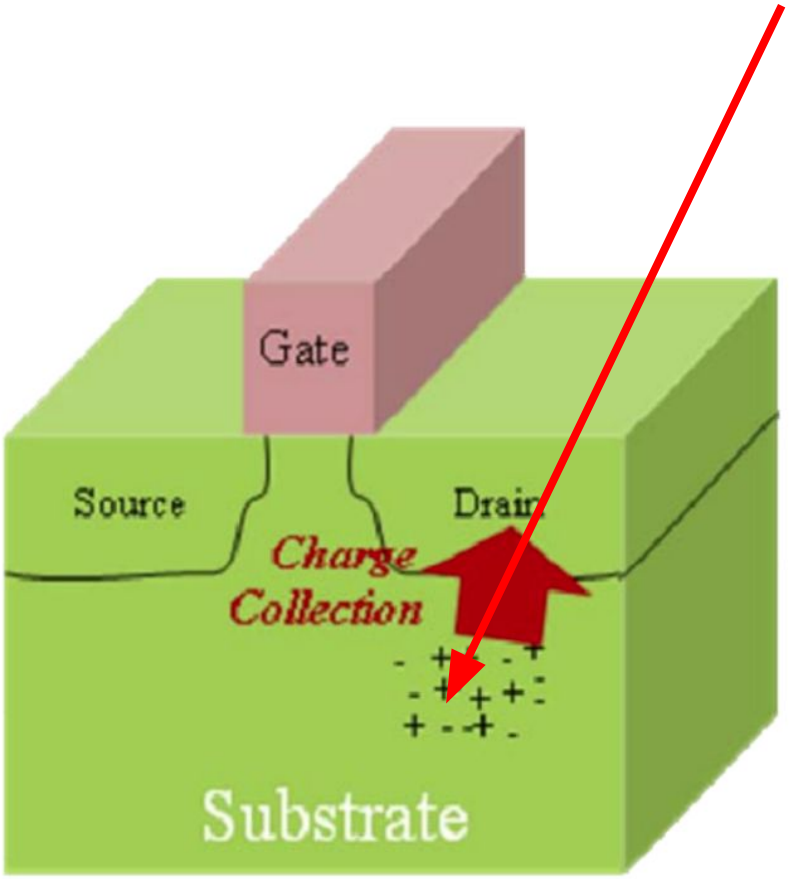
TSMC FinFET, IRPS 2014, Lu, IEDM 18

EM simulation for FinFET Self-Heating



TSMC FinFET, IRPS '14

SER basics

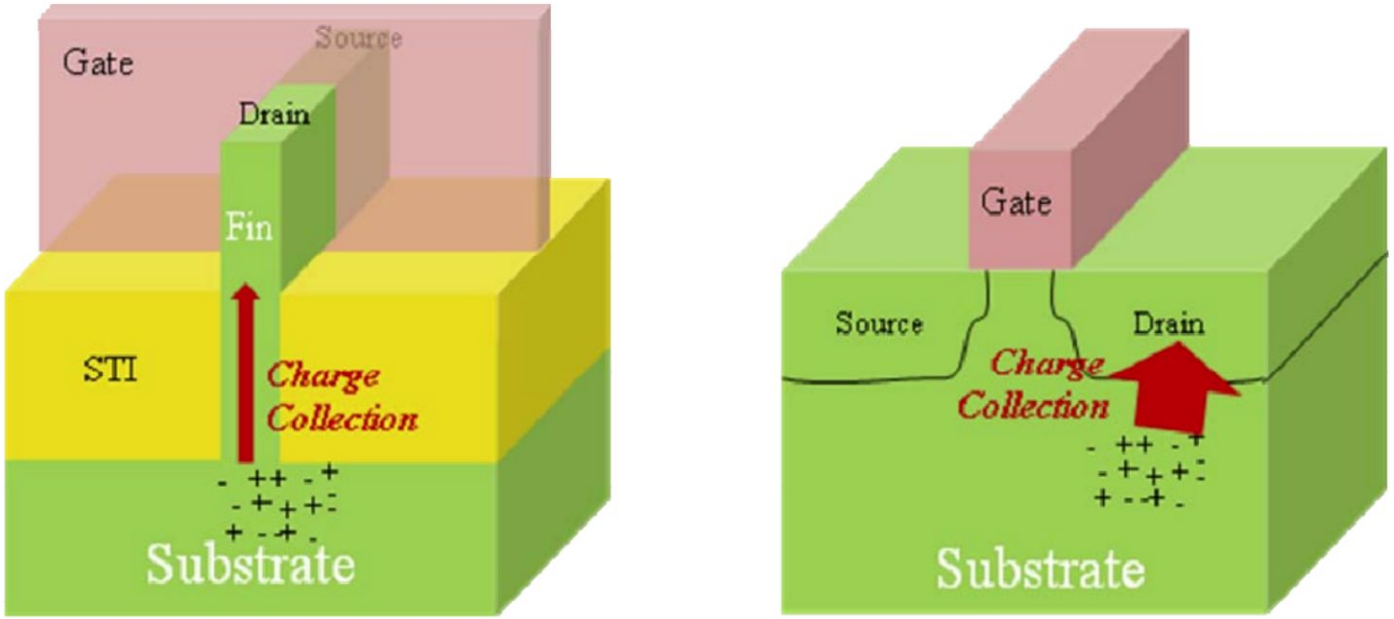


cosmic radiation
alpha particle

creates a current path
that can disturb storage nodes
like SRAM bits, Flops

Lee et al, IRPS 2015

SER in FinFETs vs Planar

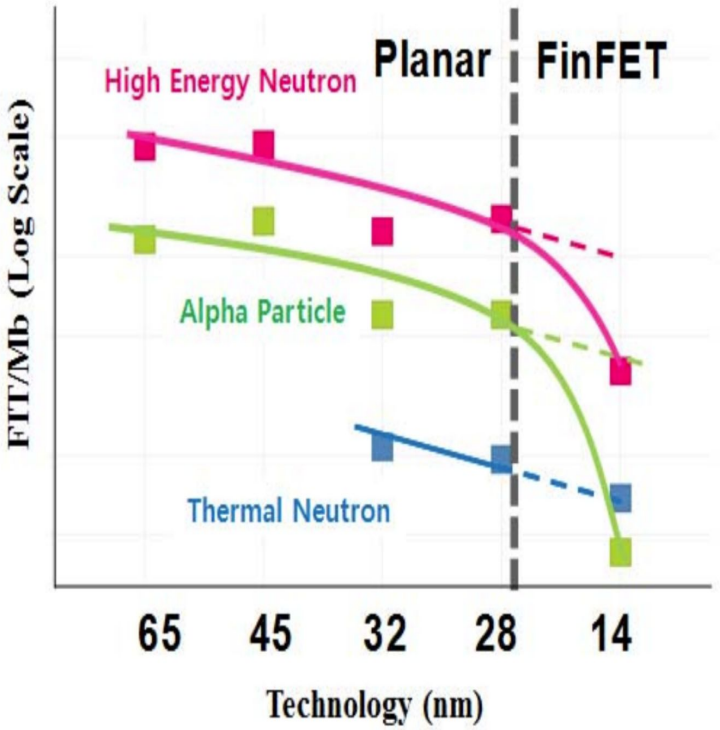


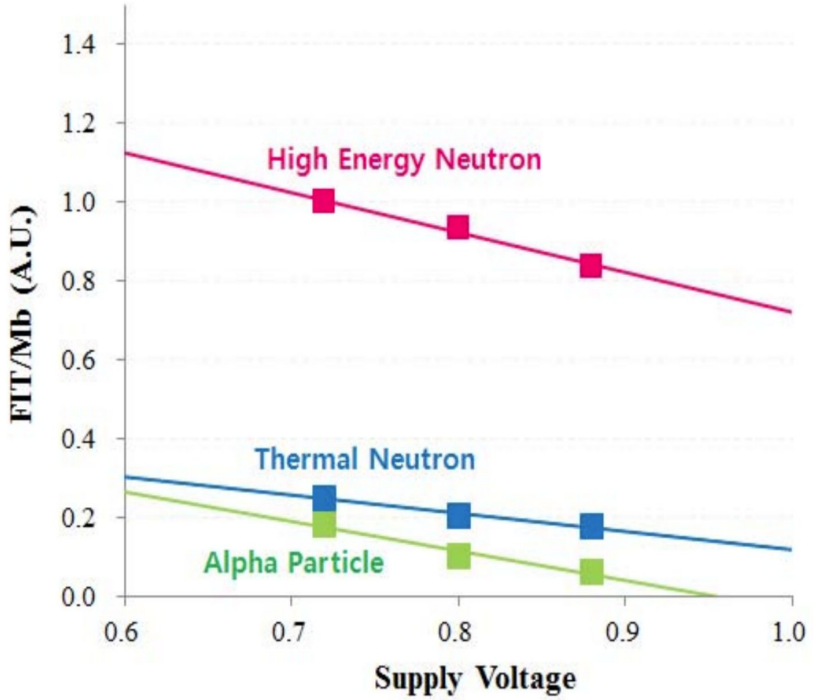
SER induced charge collection in (a) FinFET and (b) Planar FET.

FinFET presents lower charge collection area

Lee et al, IRPS 2015

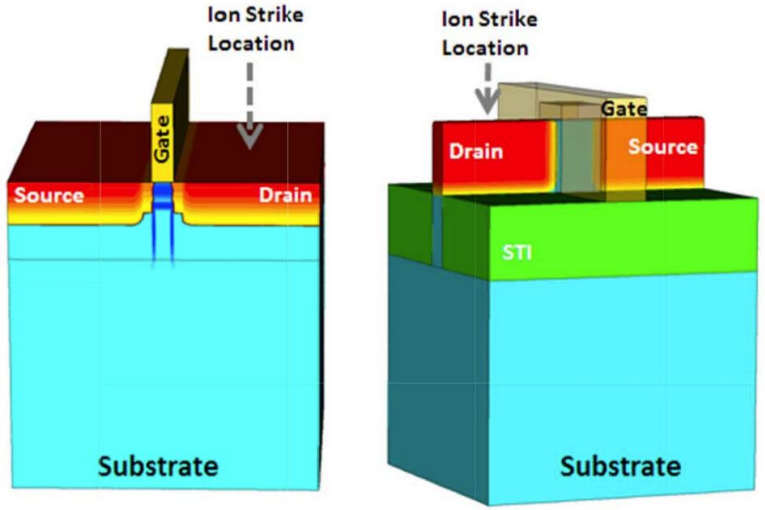
SER in SRAMs



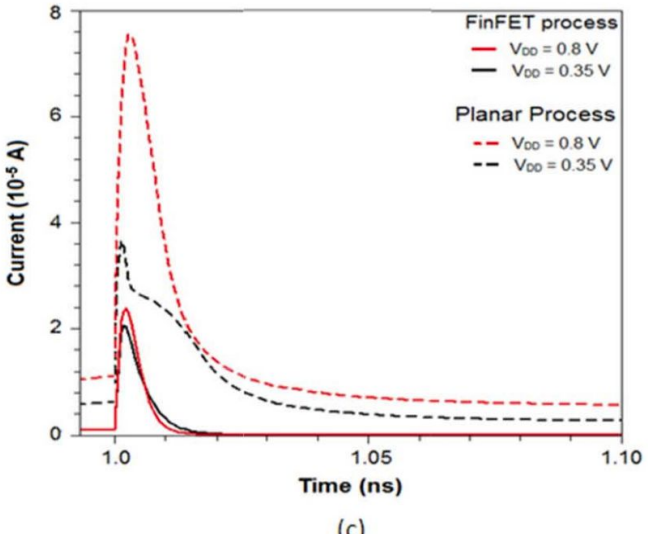


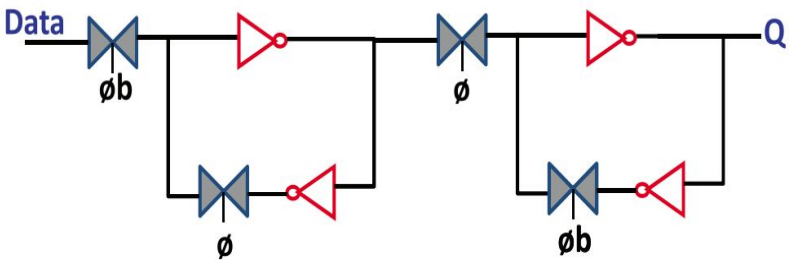
Lee et al, IRPS 2015

SER in Flops



current pulse waveforms





D-flip-flop

3D-TCAD model of
(a) planar and
(b) FinFET n-channel transistor
showing the ion-strike location.

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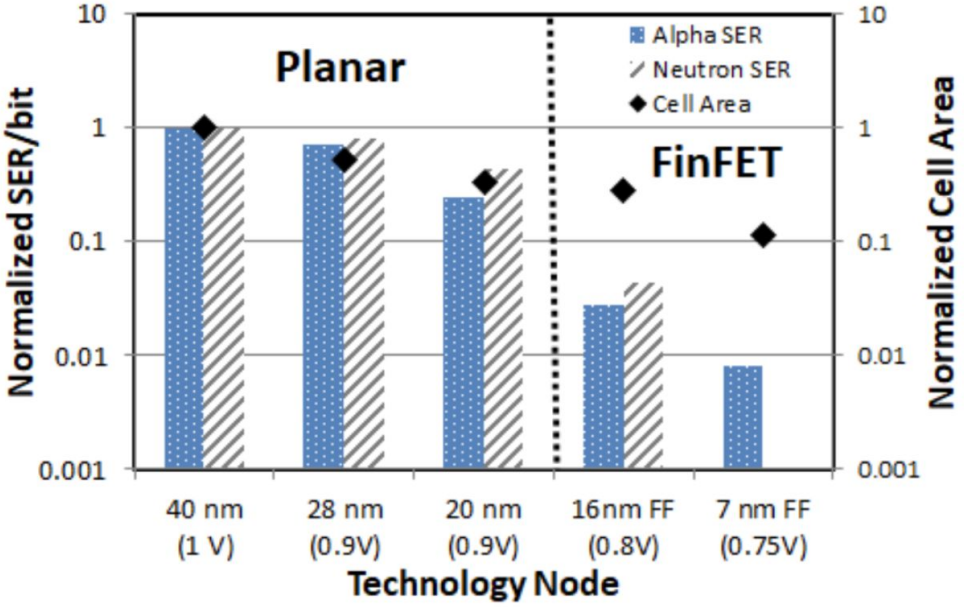
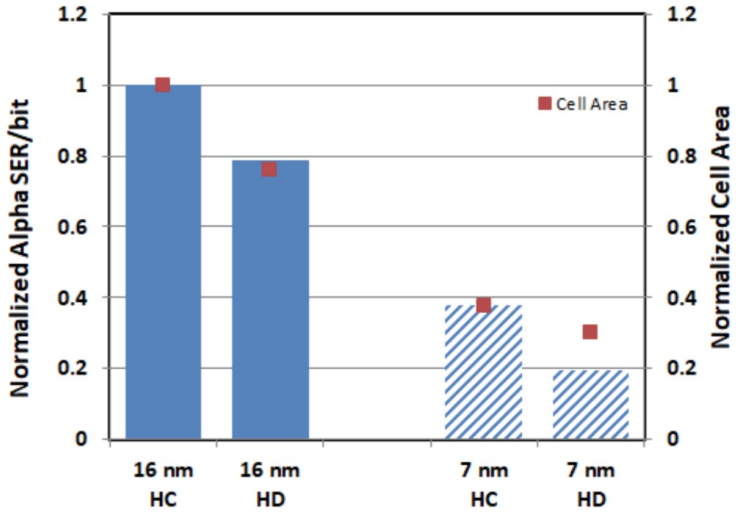
Narasimham et al, IEEE Trans. Nucl. S, 2015

SER vs Technology Node



Normalized scaling trends in the per-bit alpha and neutron SER
of SRAMs as a function of technology node; Secondary y-axis shows
the normalized SRAM bit-cell cell area comparison.

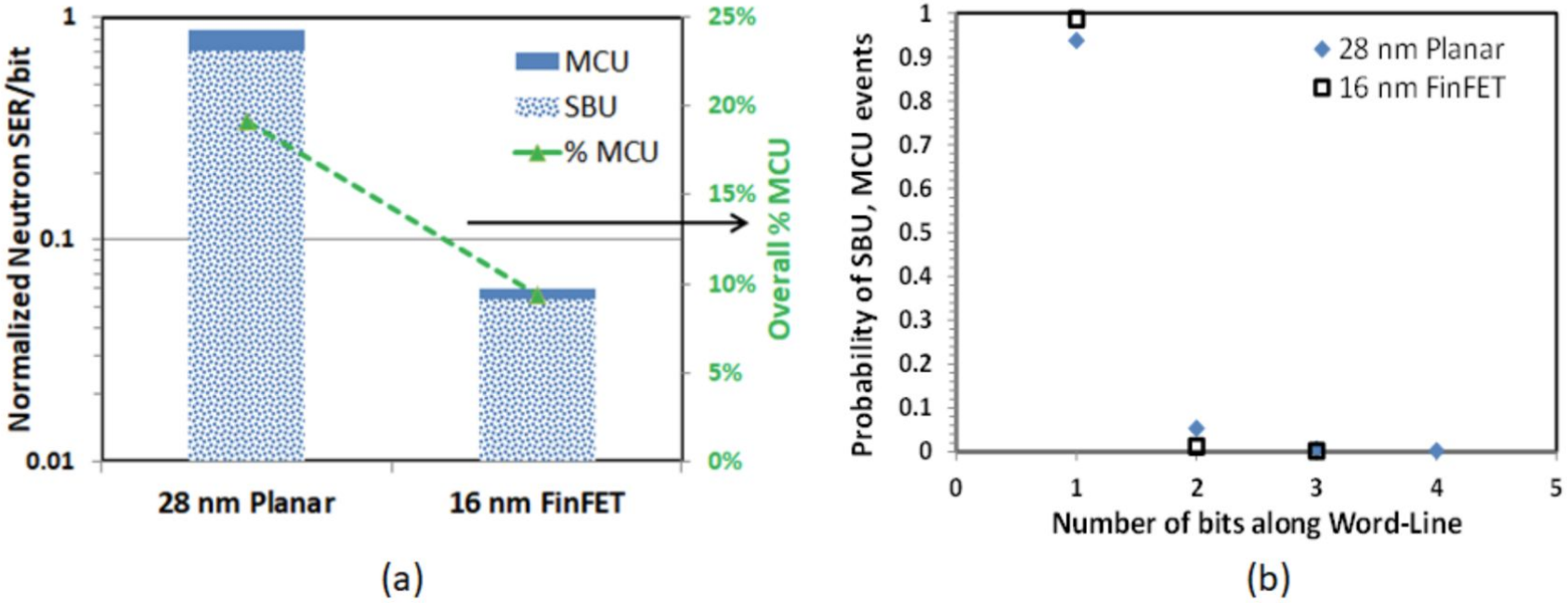


Normalized Alpha SER comparison between High-Current (HC)
and High-Density (HD) SRAM cells in 16 nm and 7 nm FinFET
processes. Secondary y-axis shows the normalized bit-cell area

comparison.

Narasimham, et al, IRPS 2018

Single Bit, Multi-Cell Upset

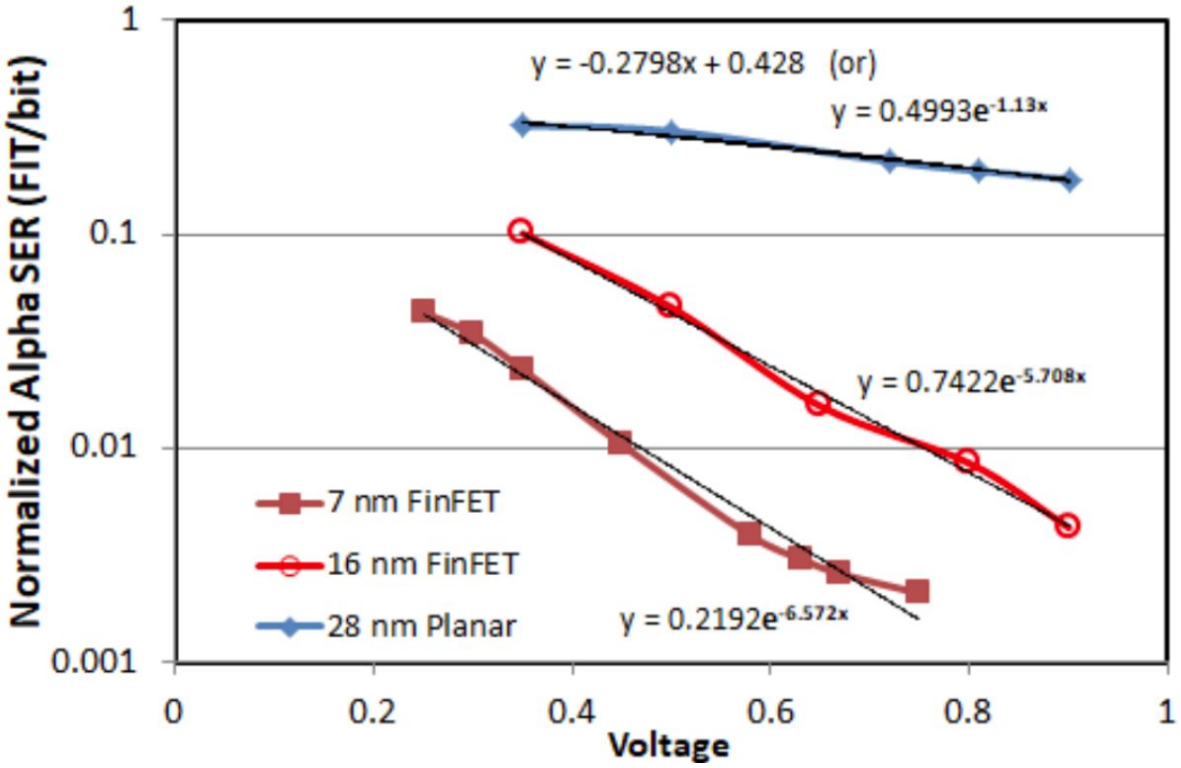


(a) Normalized single-bit and multi-cell upset neutron SER/bit for 28 nm and 16 nm processes; Secondary y-axis shows the overall percentage MCUs.

(b) Probability of SBU, MCU events as a function of number of bits along the word-line direction.

Narasimham, et al, IRPS 2018

SER Voltage Dependence



Bias dependence of the per-bit alpha particle SRAM SER for 28 nm planar, 16 nm and 7 nm FinFET processes

Narasimham, et al, IRPS 2018

SER Mitigation Techniques

- ECC
- Physical separation of columns in SRAM physical design
- Use of alpha hardened flops that use larger area and power.
- Majority voting circuits

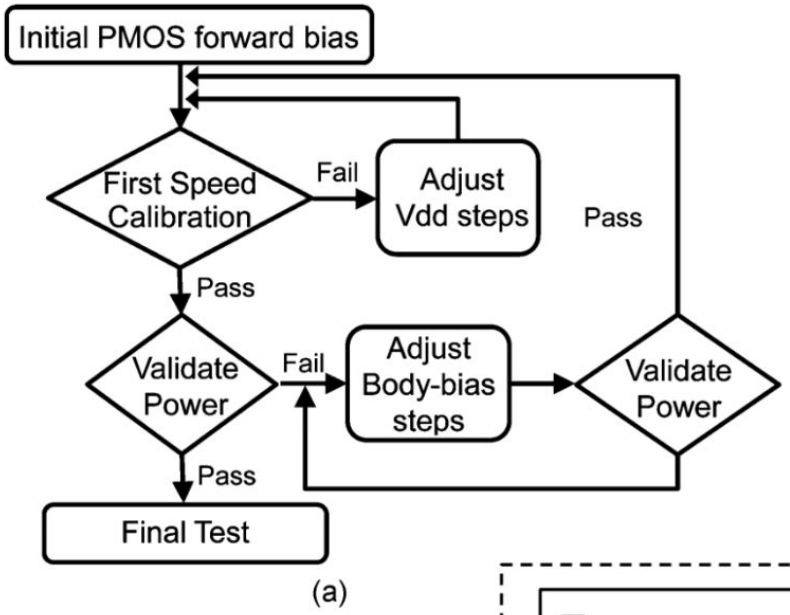
Adaptive Techniques

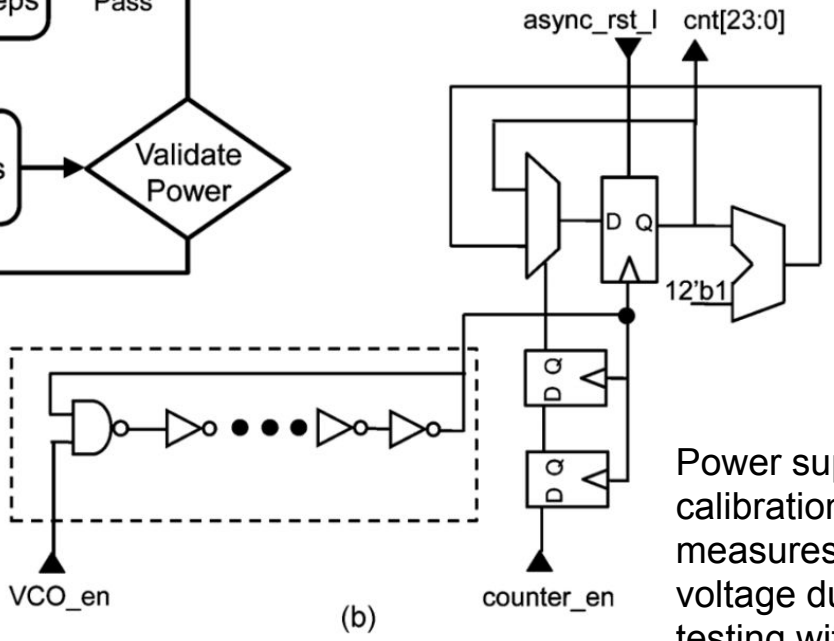
- The purpose of adaptive techniques is to
  - Mitigate reliability issues,
  - Maximize performance,
  - Reduce power
  - Maximize product lifetime
- Requires
  - Accurate reliability margin monitors
  - Power, voltage, timing margin, and thermal monitors
- Implemented typically as part of power management flow
  - Backbias, Power Gating
  - Increase voltage over time to compensate for degradation
  - Instruction or DVFS Throttling to reduce Junction Temperature
- Continuous monitoring of the monitors… and calculation of margin degradation over the lifetime of the product

Adaptive Techniques

- Back-biasing. Used to work for planar up to 40nm node, no more for FinFET.
  - SOI seems to still have reasonable back bias control
- Adaptive Voltage Scaling
- On chip monitoring and DVFS control
  - speed, voltage, thermal, FIT monitors
  - Dynamic Voltage Frequency Scaling
  - MaintainTj below a certain limit -> reduces aging
  - Adjusts the voltage to optimal setting over time to maximize performance under a given power constraint.

Body Bias Adaptation



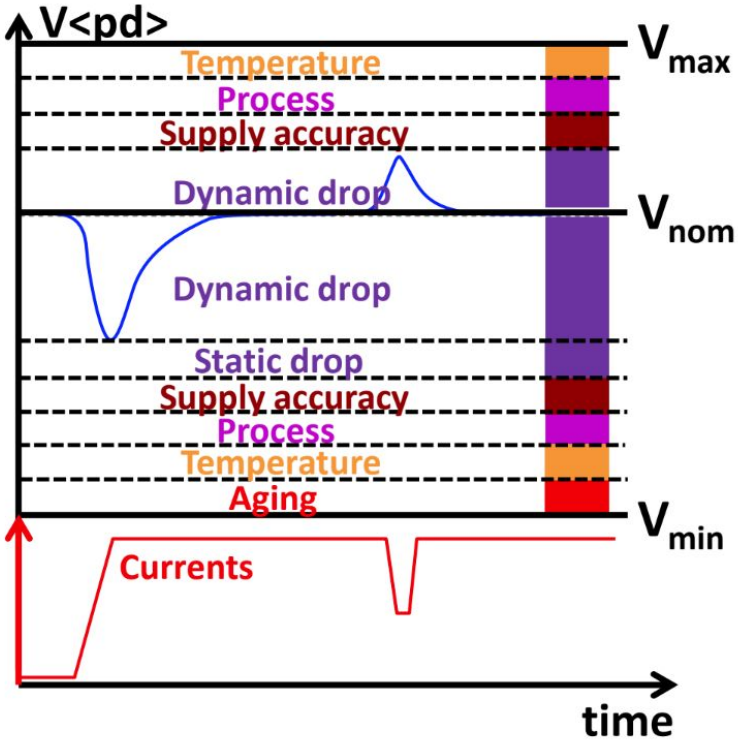


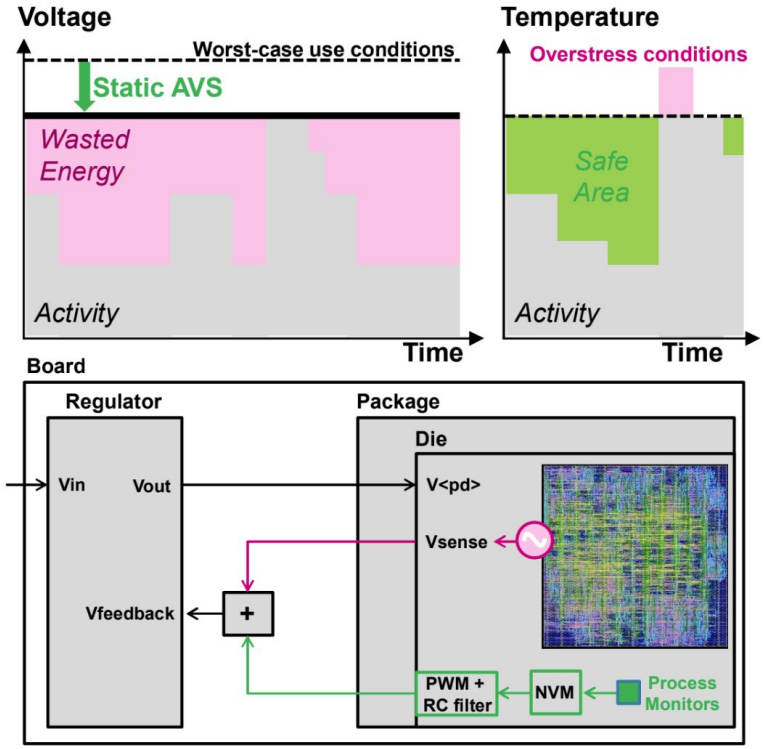
Body-bias and per part VDD to screen out parts that meet both speed and power targets

Power supply calibration circuit measures the exact voltage during testing with a voltage controlled ring oscillator

Shin et al, JSSC 2013

Adaptive Voltage Scaling

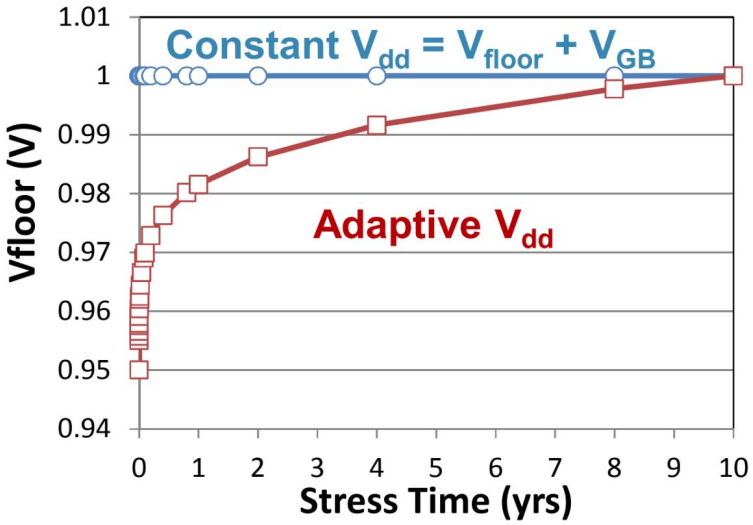


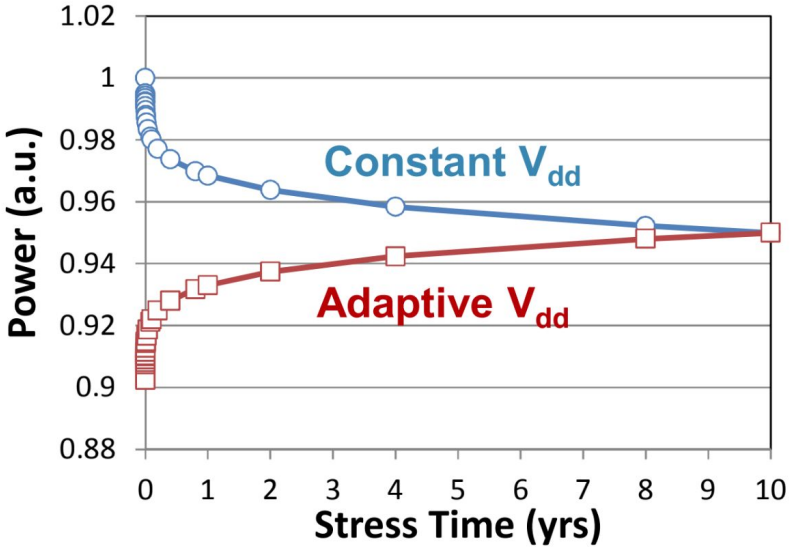


To cope with worst-case (WC) scenario conditions, voltage margins are added on top of nominal minimum voltage to account for various sources of variations either static (process or IRdrop) or dynamic (aging, temperature and workload).

Huard et al, IRPS 2018

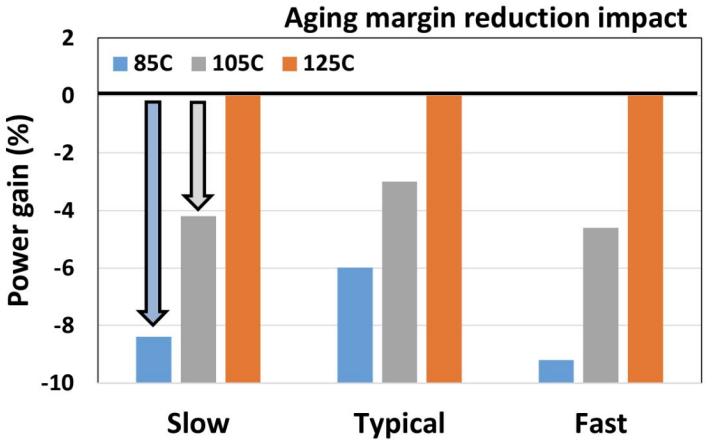
AVS impact on Power



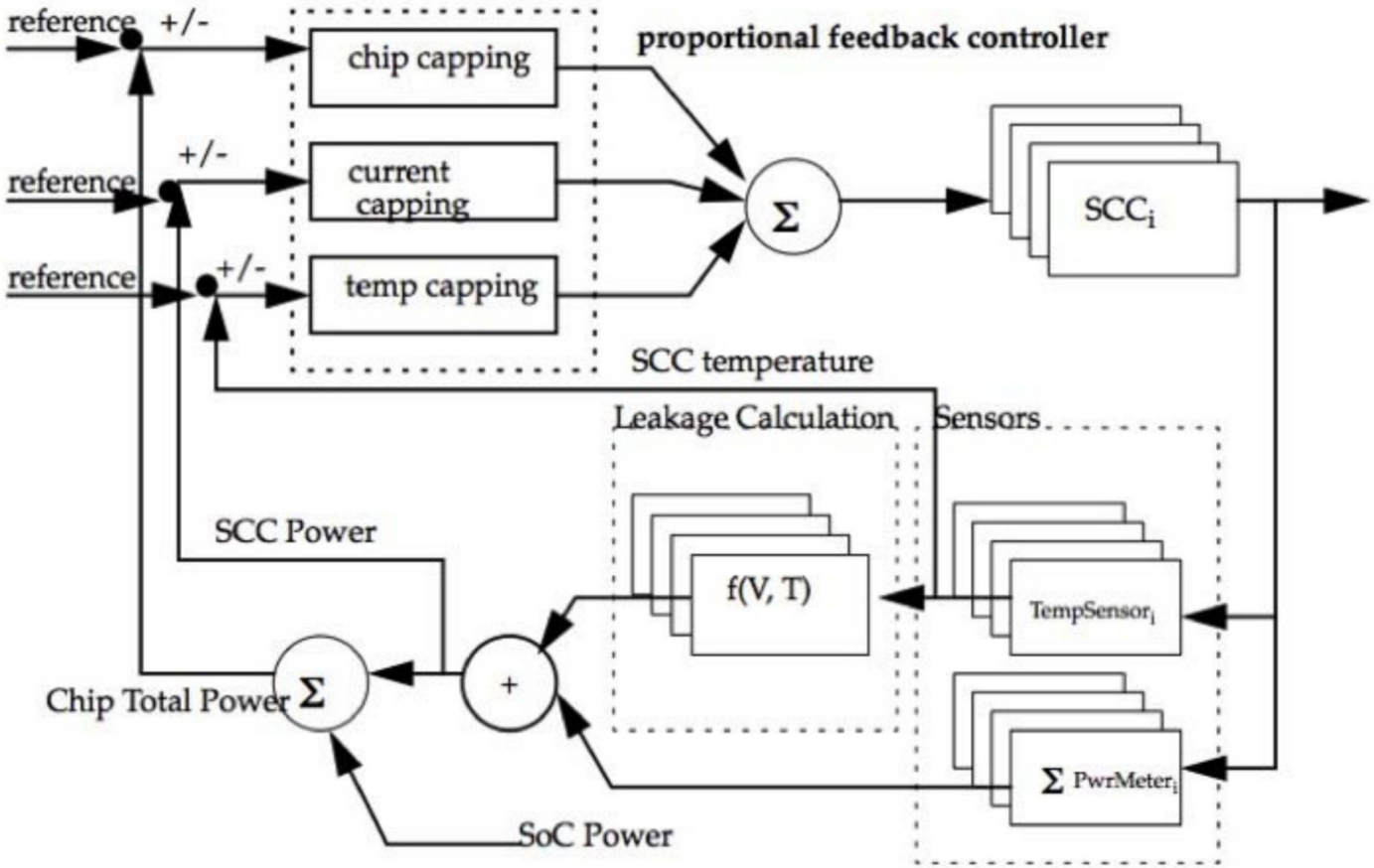


- Fresh parts need lower voltage to operate at the required frequency
- As the parts ages the voltage is gradually increased to compensate for the speed loss due to aging.
- Accounting for EOL margin form the very beginning leads to waste of power.

Huard et al, IRPS 2018



Power Management Control



Based on key nodal activity predicts the power consumption and applies DVFS to maintain Temperature and power under constraints while achieving maximum performance

Konstadinidis et al, JSSC 2016

HTOL Survival Guide

- Symmetrical stress, balanced activity, marching algorithms keep balanced count of 0 and 1 written into the SRAMs
- Free running PLLs
- Disable clock gating
- Main clock trunks in bypass mode at low frequency but running all time during HTOL
  - avoids PLL duty cycle distortion & and timing failures in B phase memories.
- Balanced scan clock stress
- Bottom line: Count of 0->1 and 1->0 transitions per device during HTOL needs to be balanced/ symmetrical

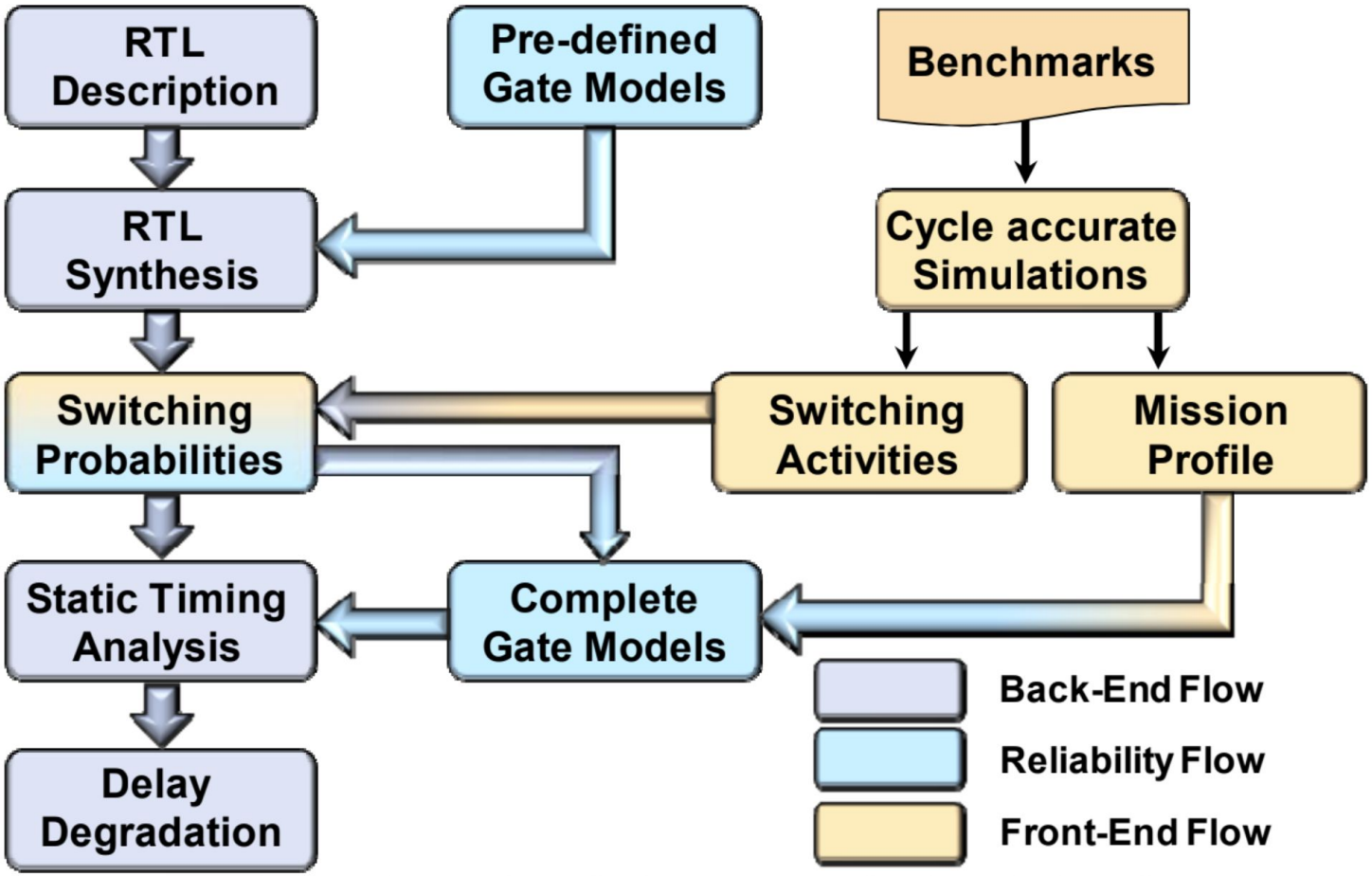
Outline

- Introduction
- Main Reliability Degradation Mechanisms
  - Voltage, Temperature, Activity dependencies
- Impact on Circuits and Products
  - Reliability Circuit Analysis & optimization
  - Aging monitors
  - Adaptive techniques
  - HTOL Best practices
- **EDA requirements**
- Conclusions

Reliability Simulators

- The Need:
  - Excessive Design margins add time to market, loss in performance, may kill product competitiveness
- It does not affect only HPC devices
- Consumer Electronics and Automotive are equally affected
  - Need fast and accurate reliability simulators to handle not only transistor level circuits but large VLSI

System Reliability Framework



Huard et al, IRPS 2012

Additional EDA requirements

- Need separate reliability models at transistor level with common API interface
- Characterization of standard cell libraries and at various voltage biasing, slew rate and Temperature conditions and generation of reliability macromodels
- The VLSI reliability tools need to use these macromodels and back annotate to the Temperature per device based on full chip Thermal map and SHE
- Activity based on RTL/gate level simulation
- Timing, slew rates, based on STA analysis,
- IR data per device based on dynamic IR back-annotation, biasing conditions

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Conclusions

- Product Reliability analysis is a Must
- Worst case analysis is a thing of the past
- Co-optimization of product performance, robustness and time to market requires avoidance of overdesign
  - -> that requires accurate reliability analysis
    - -> that requires good understanding and cooperation between Reliability Physics, Circuit, and EDA communities...

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