Fachhochschule
Dortmund
University of Applied Sciences and Arts

Radiation-Hard Power Management and Control Circuits for the ATLAS Pixel Detector High-Luminosity Upgrade

TWIN Relect Workshop, Βόλος

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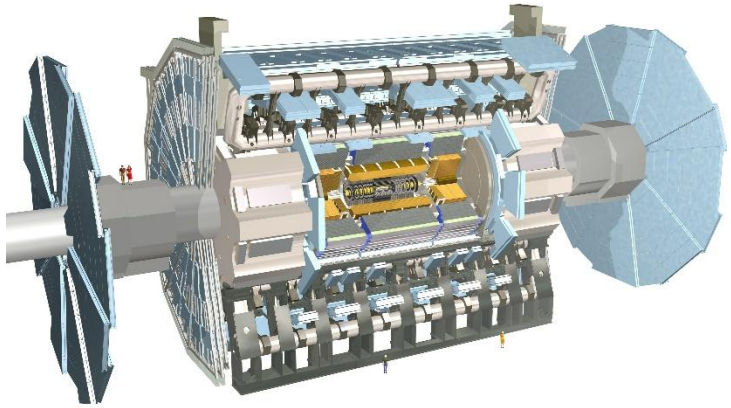
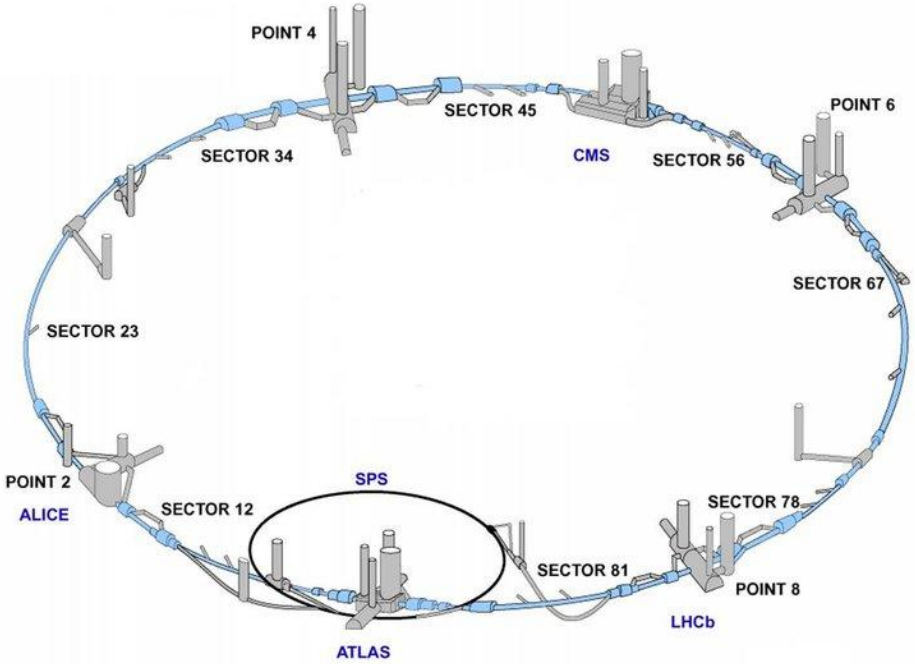
ATLAS Pixel Detector at the LHC CERN Geneva/Switzerland

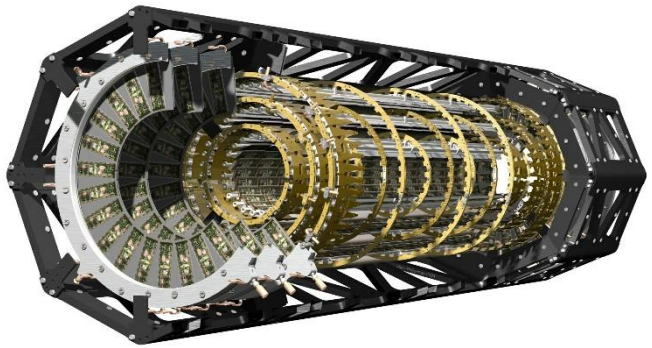
- ASICs for the LH-LHC upgrade
- Study of elementary particles and their interactions
- Higgs Boson discovered in 2012
- pixel detector is used for particle tracking



ATLAS Experiment

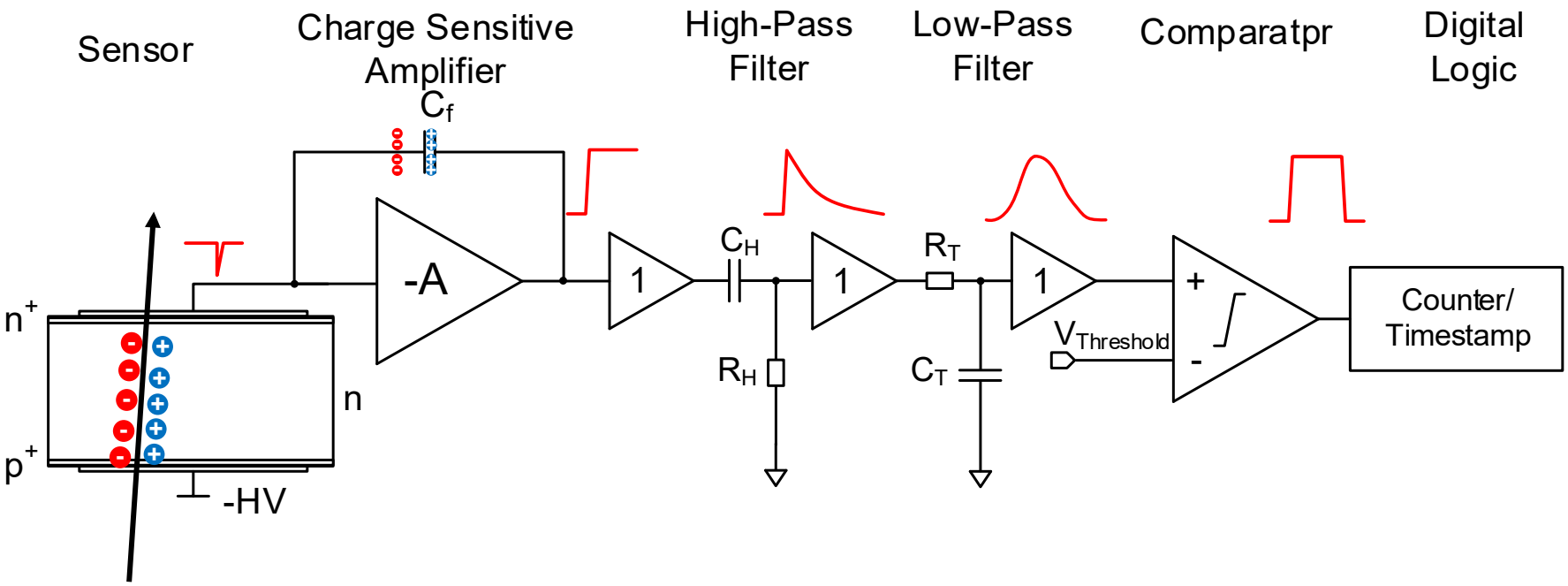


Large Hadron Collider



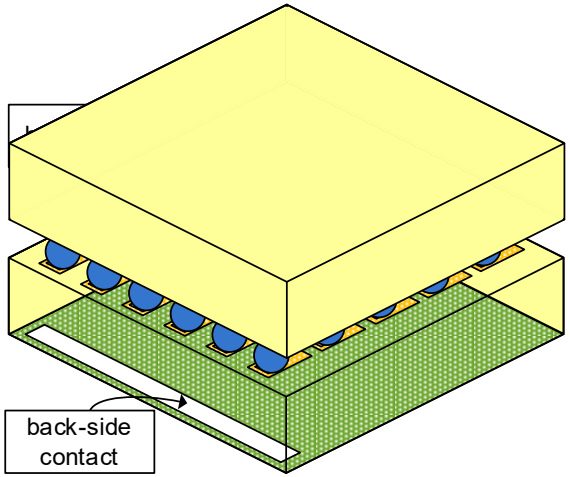
Pixel Detector

Detection of Ionizing Radiation

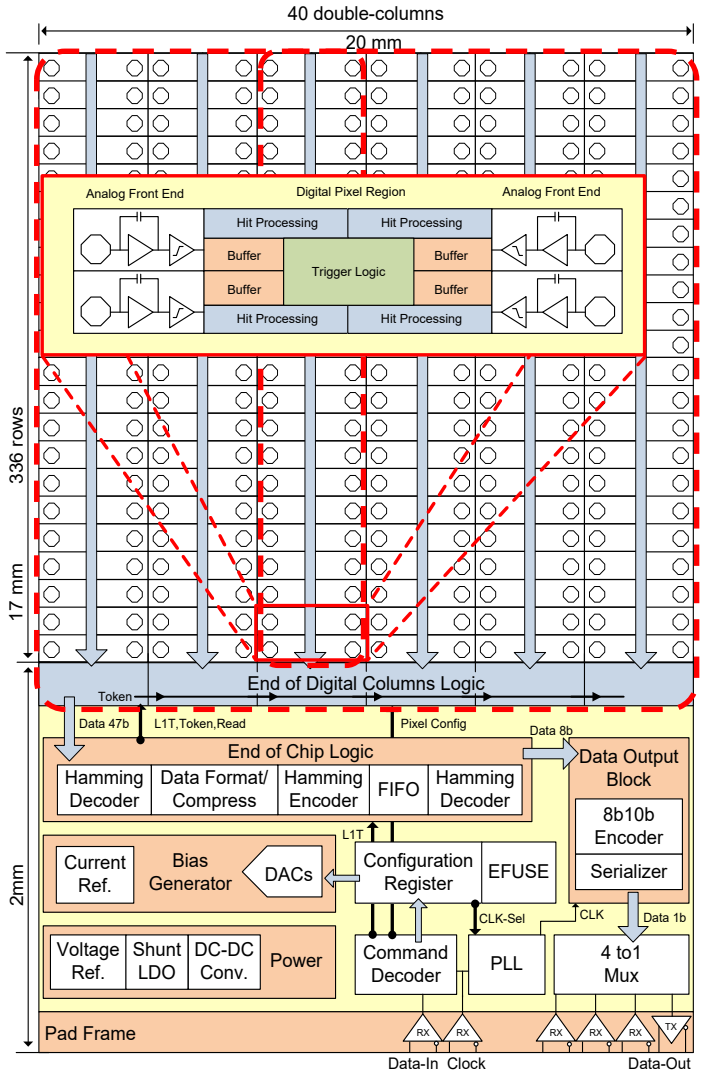


- The sensor is a fully depleted reverse biased PN diode
- High-energy charged particles generate electron/hole
- Charge carrier movement induces a current flow at the sensor electrodes
- The charge signal is integrated, filtered, and compared with a threshold

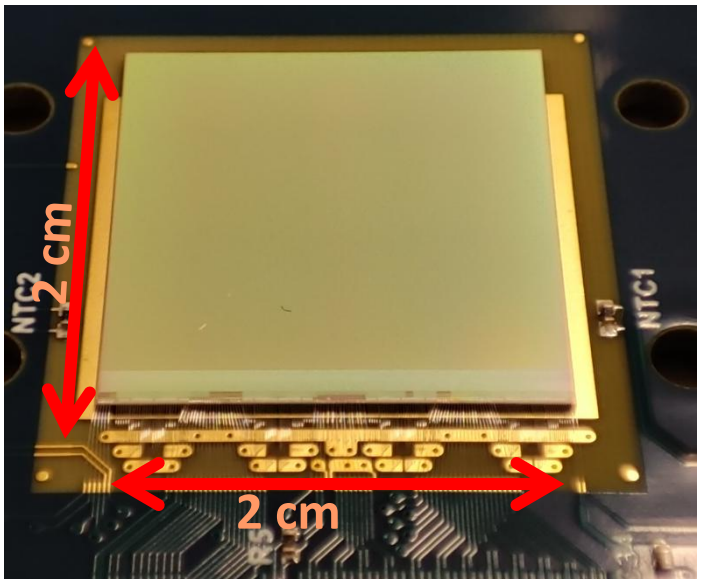
Hybrid Pixel Detector & Readout ASIC



- 2-dimensional segmentation
- 50µm x 50µm pixel size
- Sensor and readout circuits on different chips
- flip-chip bump bonding
- double column-readout architecture
- pixel region
- digital top implementation
- „analog islands in digital sea“



RD53 Hybrid Pixel Detector Module



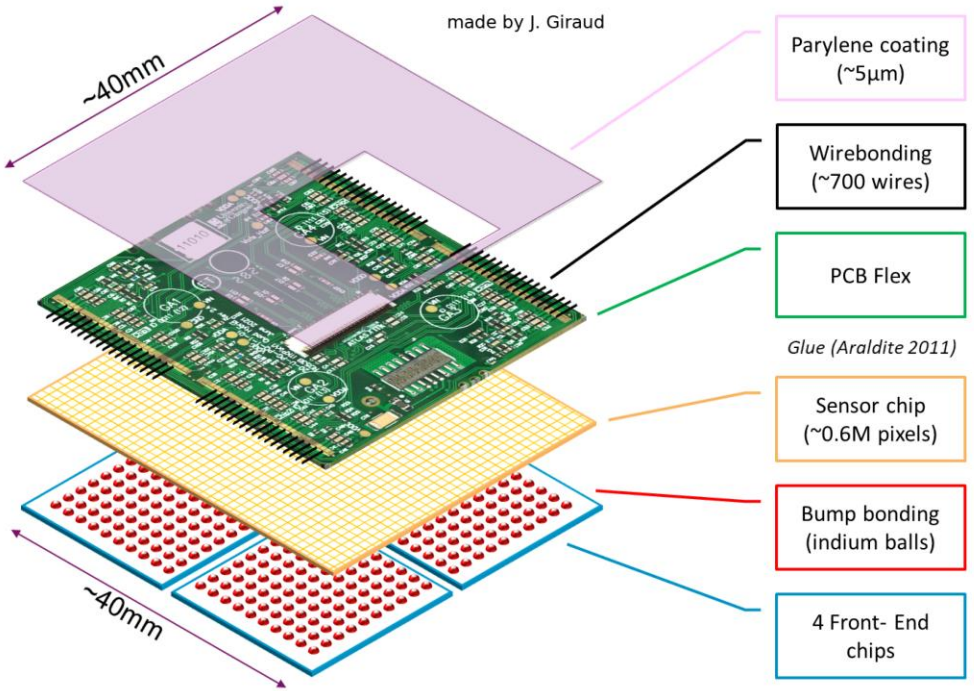
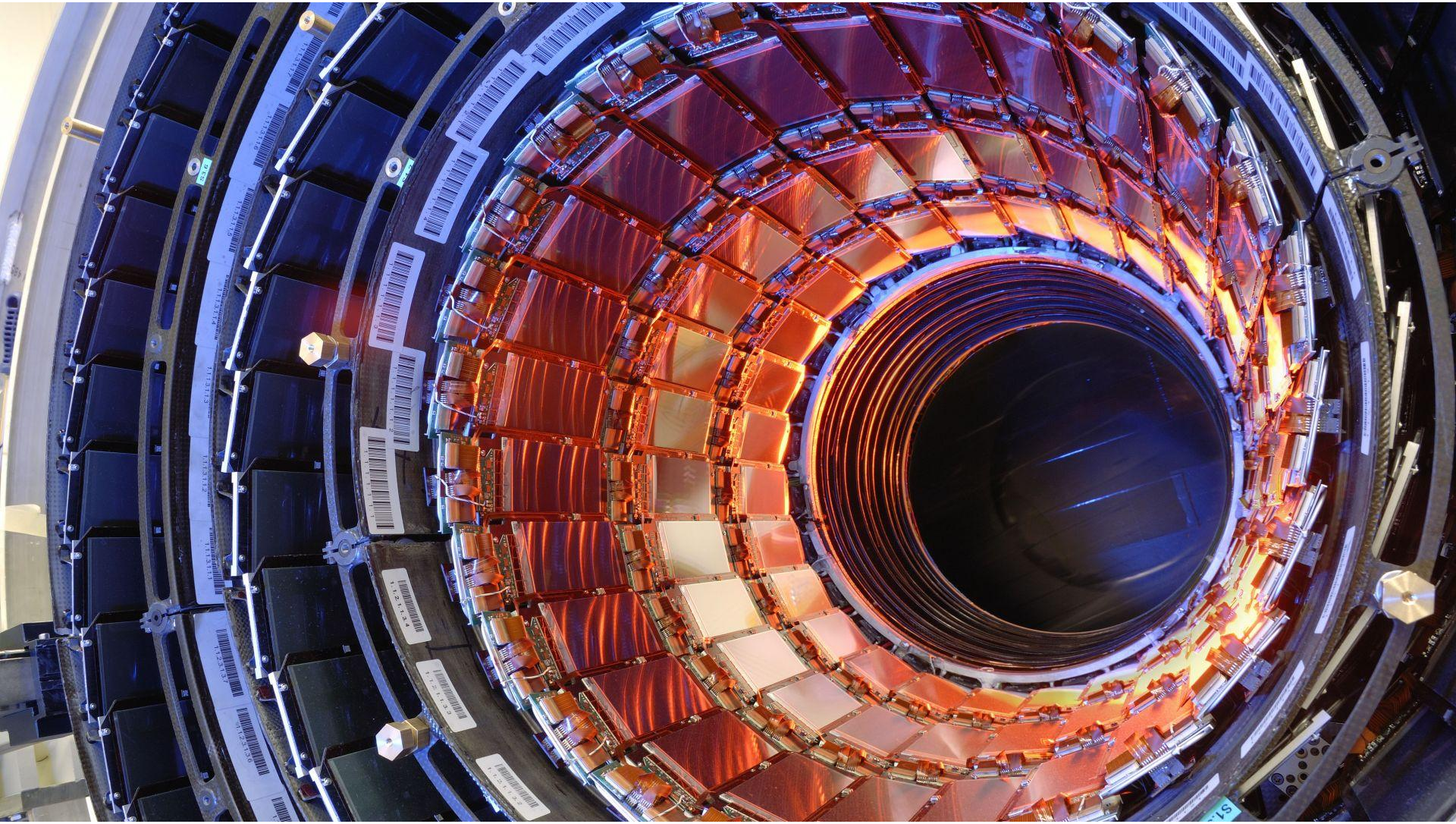
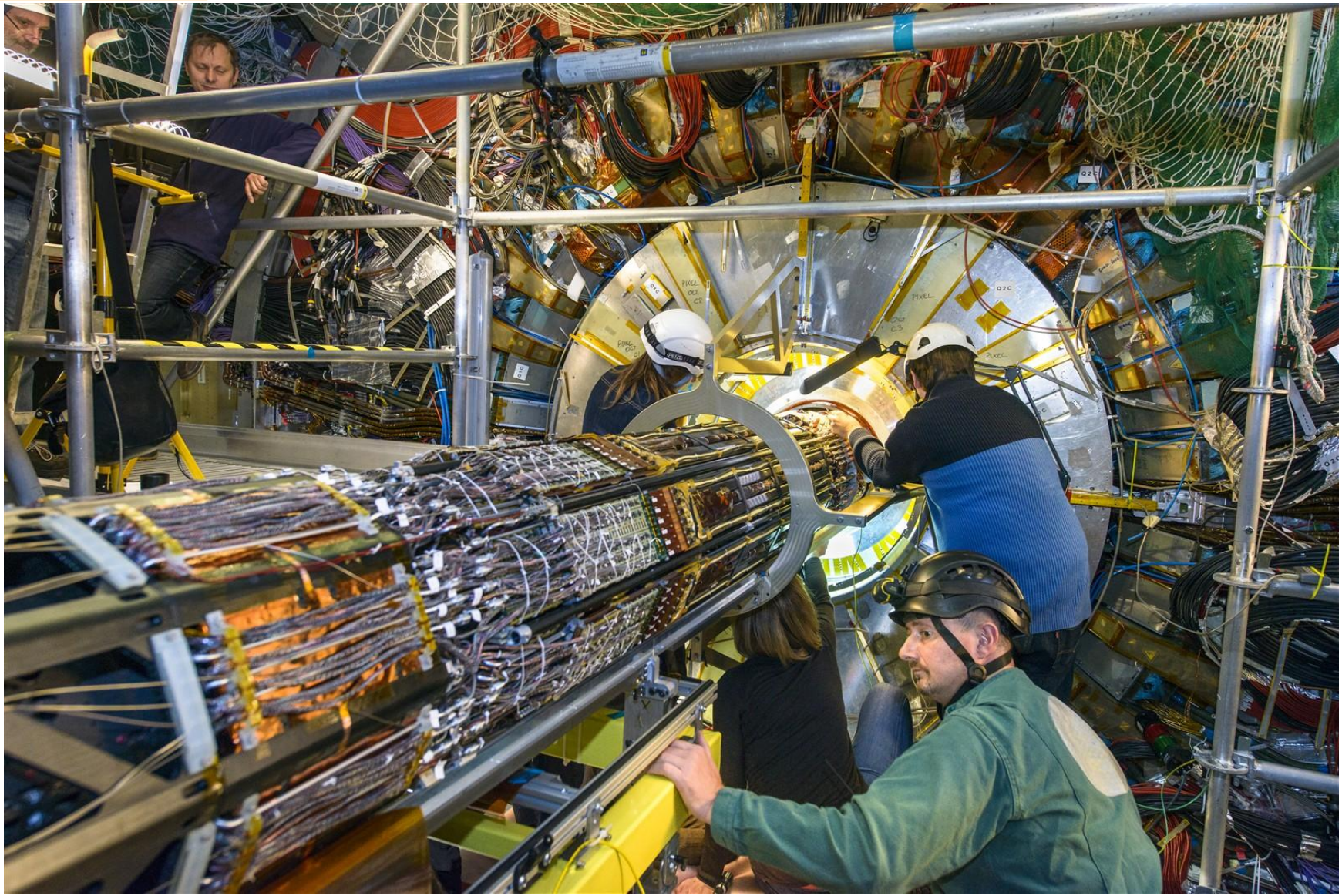


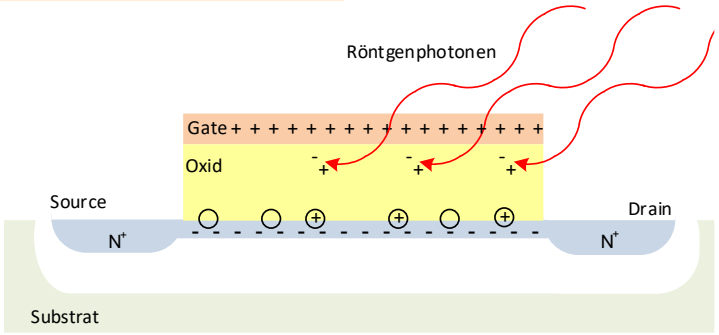
Photo of a Pixel Detector barrel



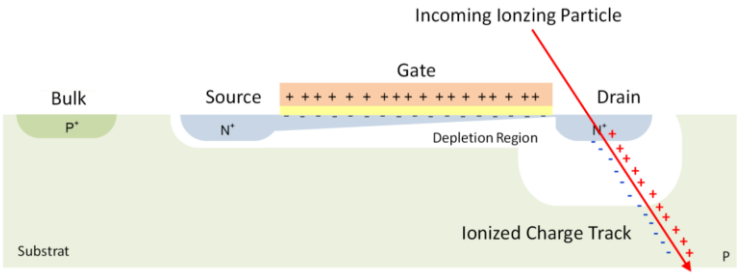
Installation of the IBL pixel detector



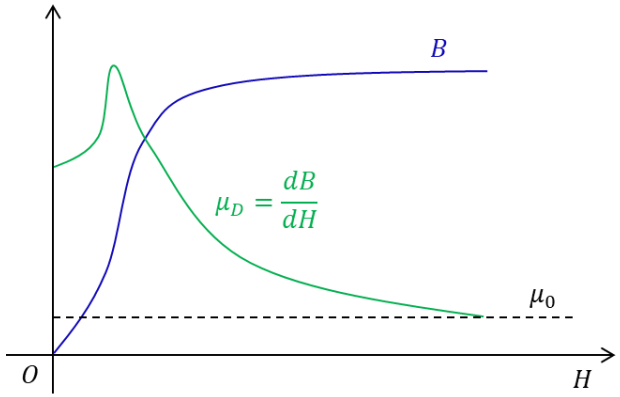
Special Conditions in HEP Experiments



- 1 Gigarad (10 MGy) of Total Ionizing Dose
- significant radiation induced threshold voltage shifts for gate-oxide thickness larger than 5nm

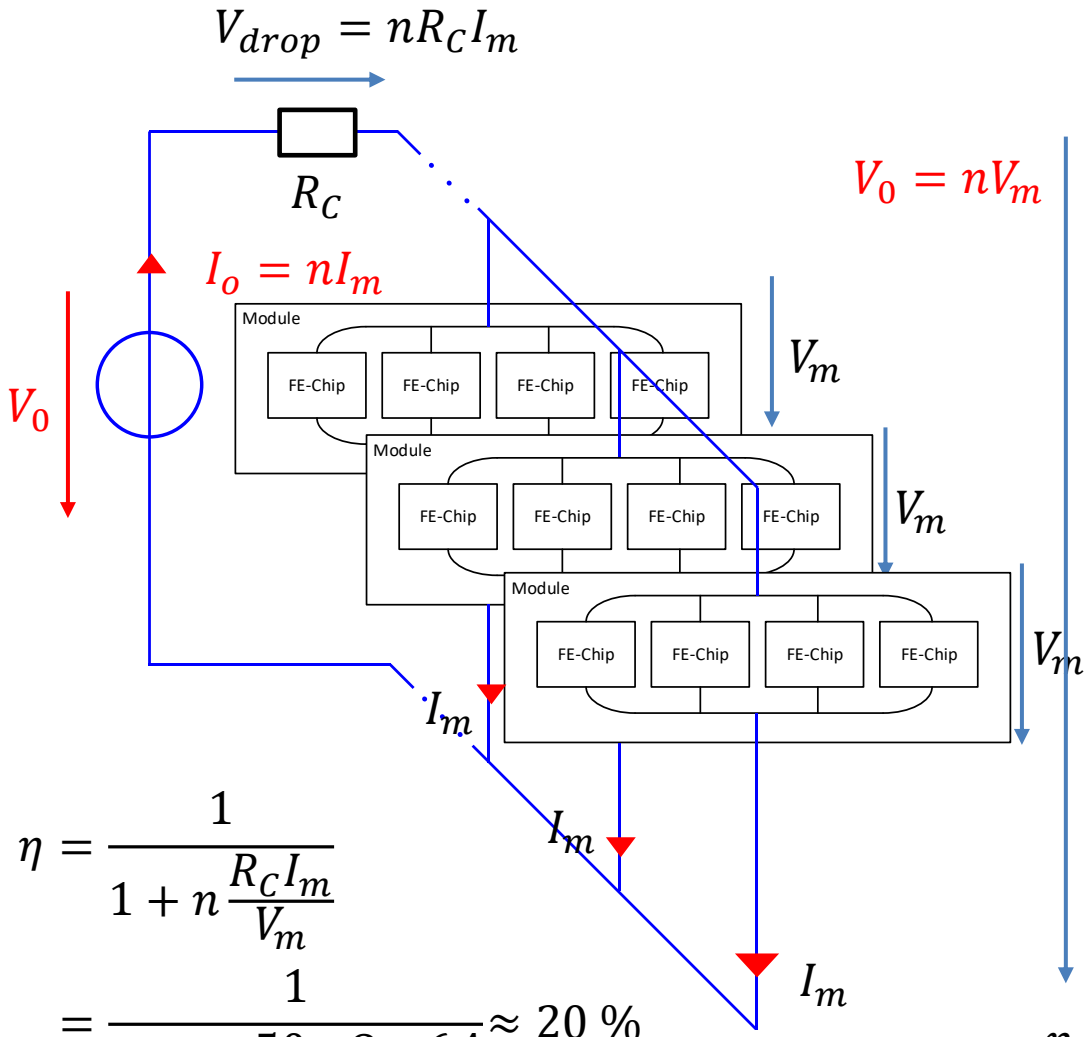


- particle hit rate of 1 GHz/cm^2
- Single Event Upsets (SEU)
  - Bit flips in memory elements (FF, Latches, SRAM)
- Single Event Transients (SET)
  - Glitches or transients in logic or analog circuits



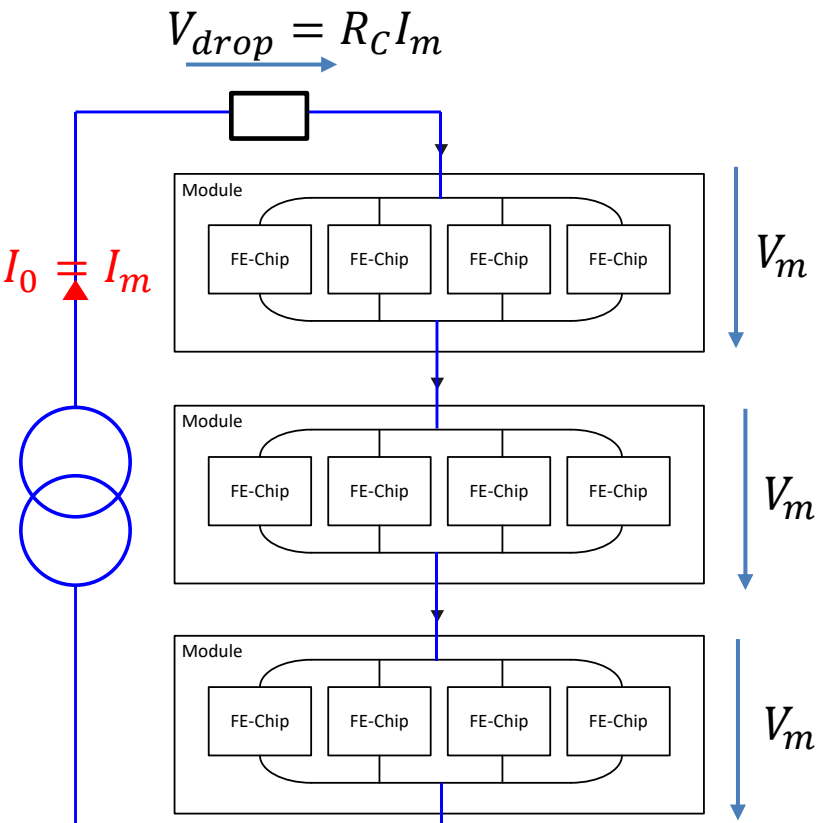
- High magnetic field (2-4T) to identify charged particles
- ferromagnetic materials saturate
- only air coils applicable
- air coils have larger dimensions than coils with core

Optimization of Power Efficiency in Detector Electronics



$$\eta = \frac{1}{1 + n\frac{R_C I_m}{V_m}}$$

$$= \frac{1}{1 + 16\frac{50m\Omega \cdot 6A}{1{,}2V}} \approx 20\ \%$$

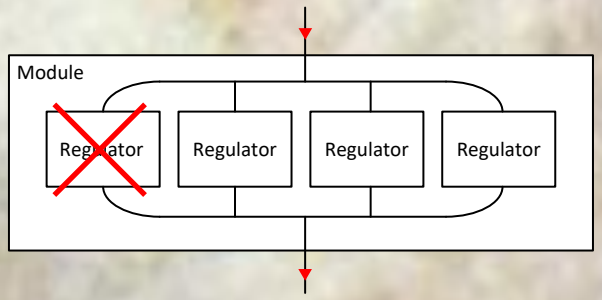


$$\eta = \frac{1}{1 + \frac{R_C I_m}{nV_m}} \approx \frac{1}{1 + \frac{50m\Omega \cdot 6A}{16 \cdot 1.2V}} \approx 98{,}5\ \%$$

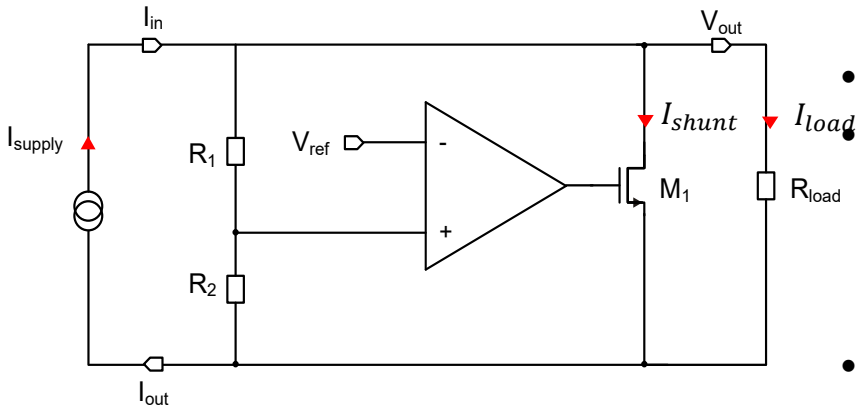
The Serial Powering Commandments

- **You shall prevent the break of the serial powering chain**
- **You shall avoid hot spots**
- **You shall distribute power equally across the chips and the module**
- **You shall avoid single point of failure**
- **You shall introduce redundancy**

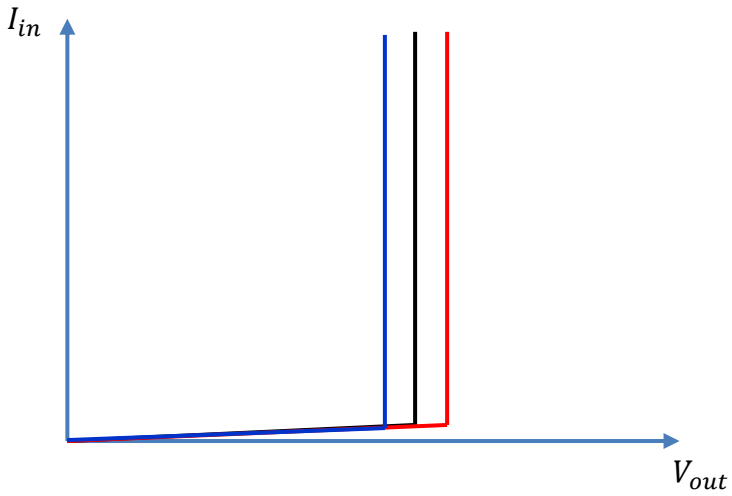
- **You shall operate several regulators in parallel on module level**

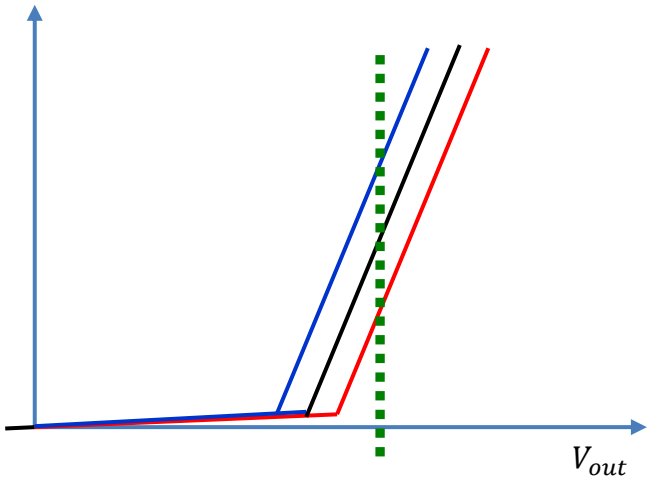


Shunt Regulator Restrictions



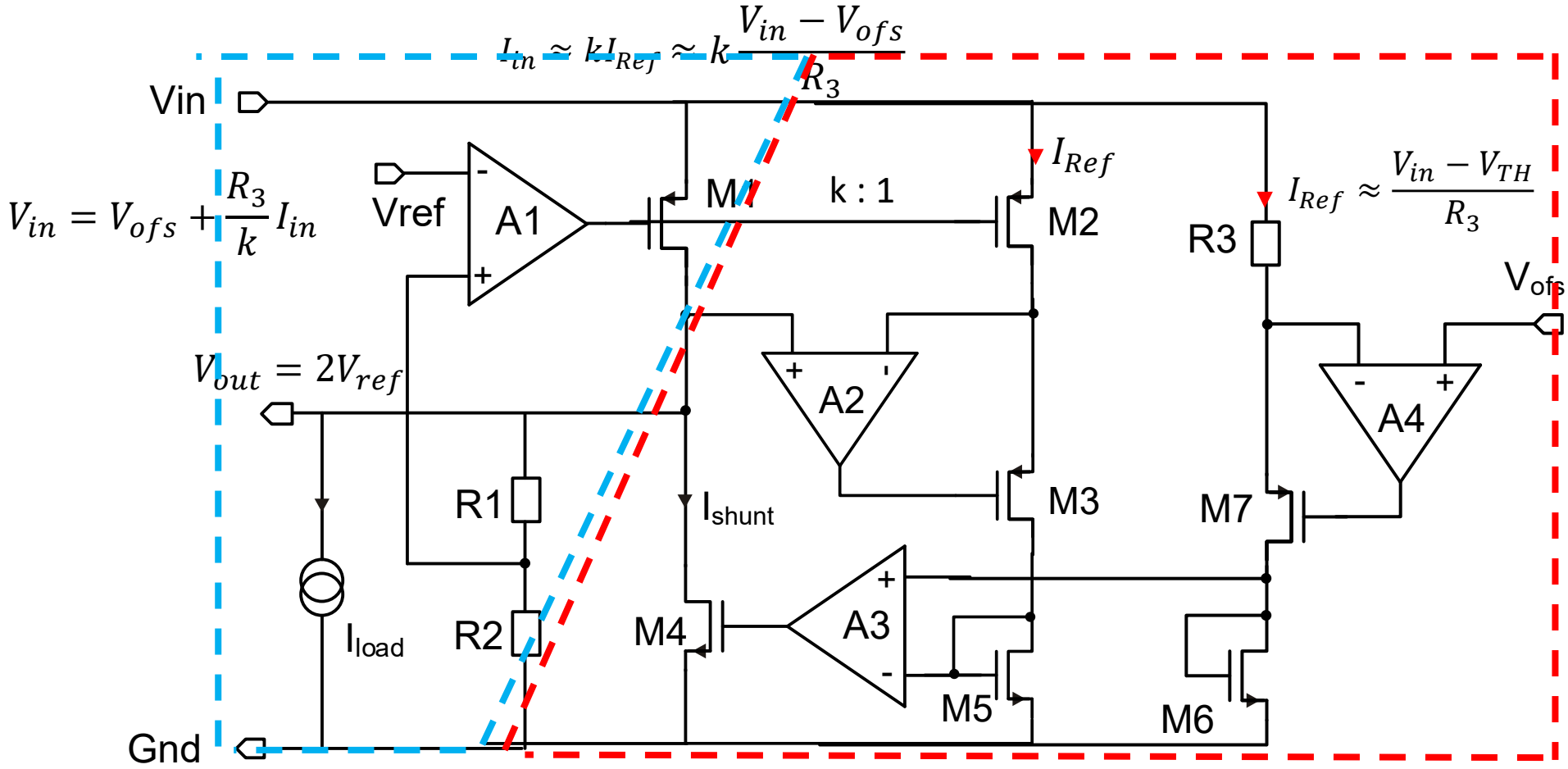
- parallel placed regulators increase reliability
- very steep voltage to current characteristic
  → Small output impedance ☺
  → Offset voltages lead to unbalanced current distribution across parallel placed regulators ☹
- less steep V/I characteristic helps current balancing





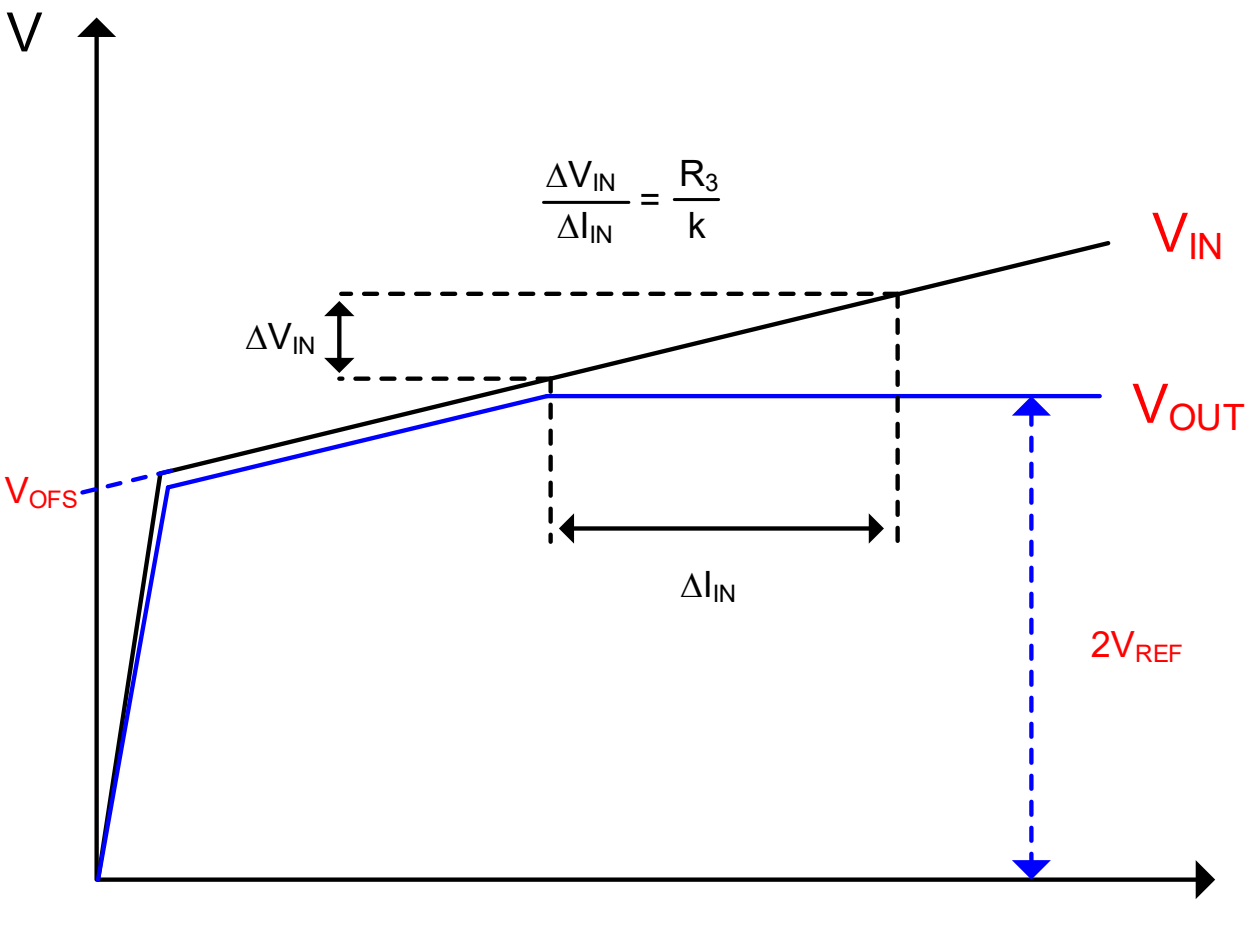
Shunt-LDO Regulator Design Concept

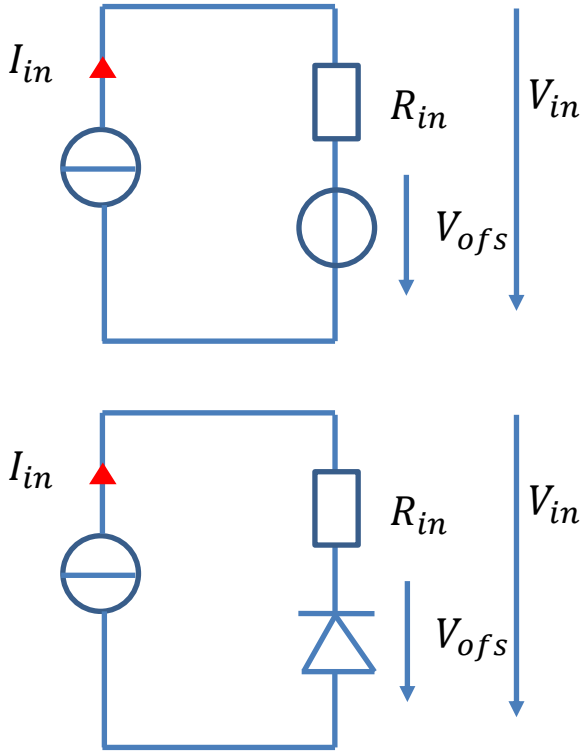
- The Shunt-LDO regulator combines the functionality of an LDO voltage regulator with the capability of a shunt regulator to drain a constant current
- Two control loops: 1) constant output voltage 2) constant current flow through the regulator



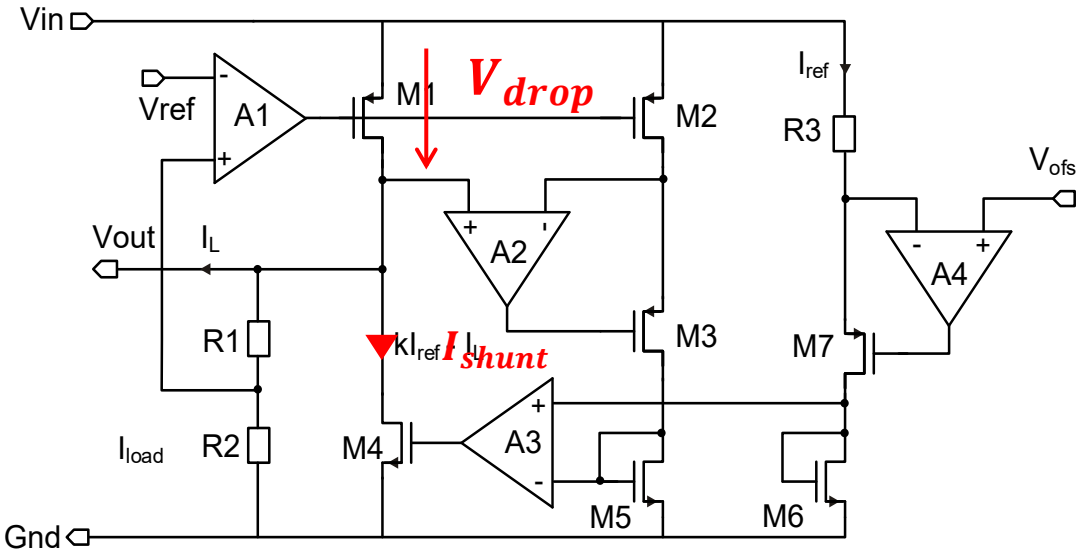
Shunt-LDO Regulator V/I Characteristics

$$V_{in} = V_{ofs} + \frac{R_3}{k} I_{in}$$



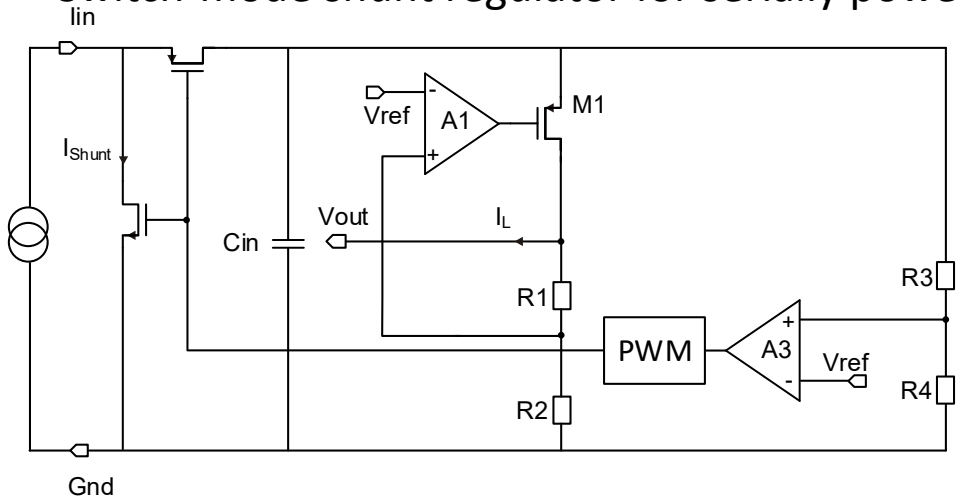


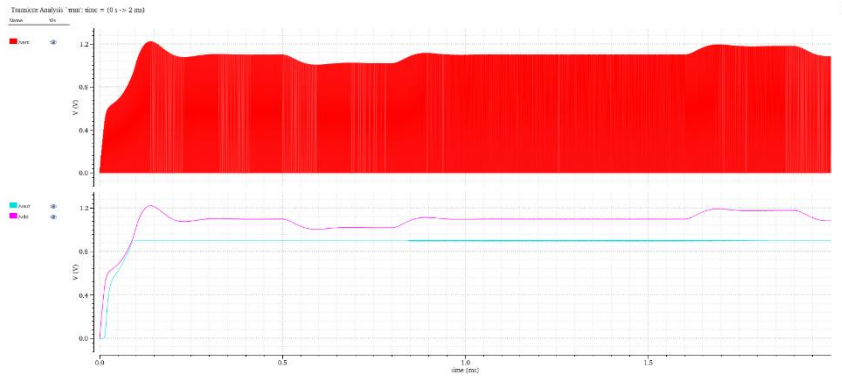
High-Efficient Switch-Mode Shunt Regulator



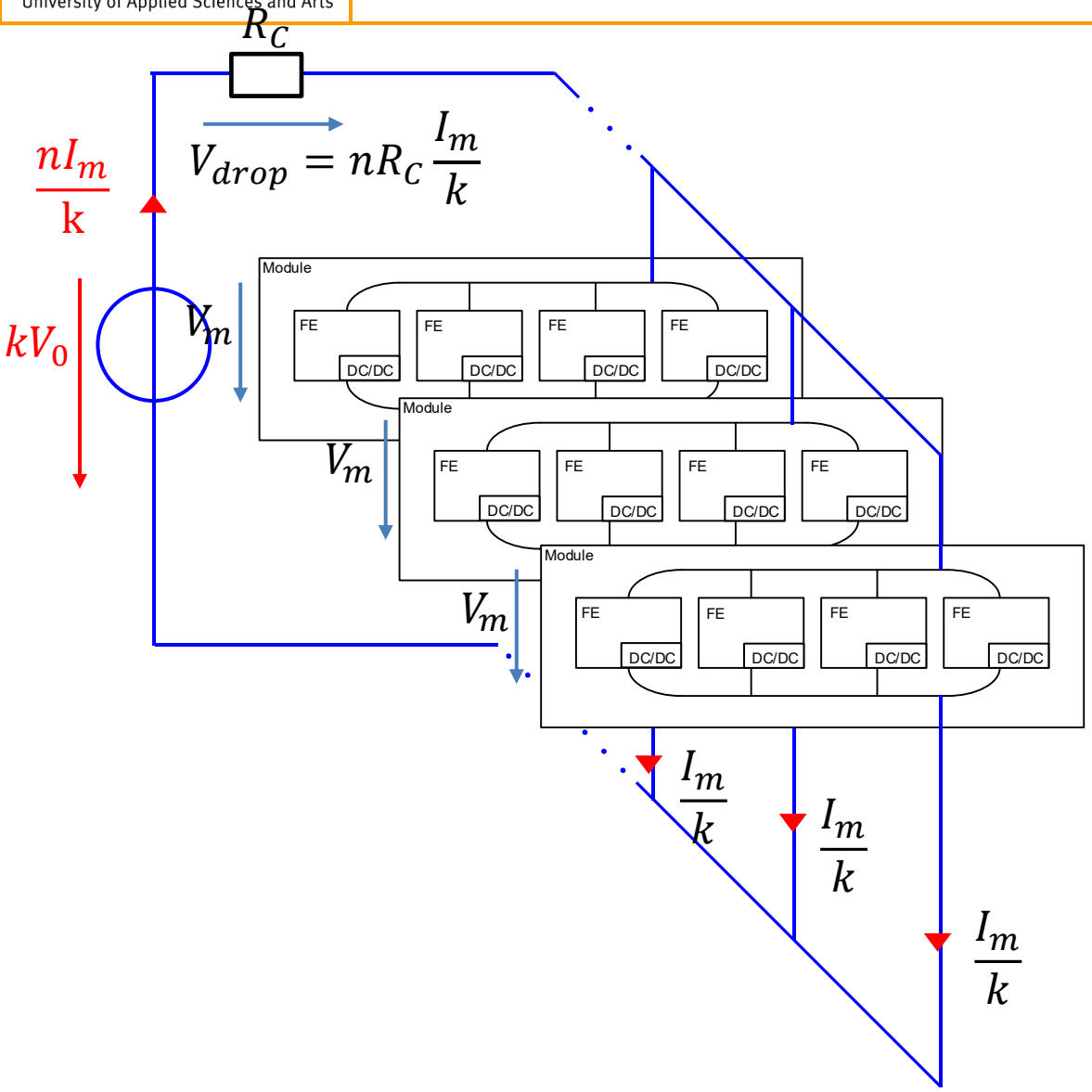
$$\eta = \frac{1}{\left(1 + \frac{V_{drop}}{V_{out}}\right)\left(1 + \frac{I_{Shunt}}{I_{load}}\right)}$$

- Switch-mode shunt regulator for serially powered systems





DC / DC Conversion



- power is distributed at k-times higher supply voltage
- supply voltage is converted down close to the load
- supply current is reduced by k

$$\eta = \frac{1}{1 + \frac{n}{k^2}\frac{R_C I_m}{V_m}}$$

$$\eta_4 = \frac{1}{1 + \frac{16}{16}\frac{1\Omega \cdot 6A}{1.2V}}$$

$$\approx 16.7\ \%$$

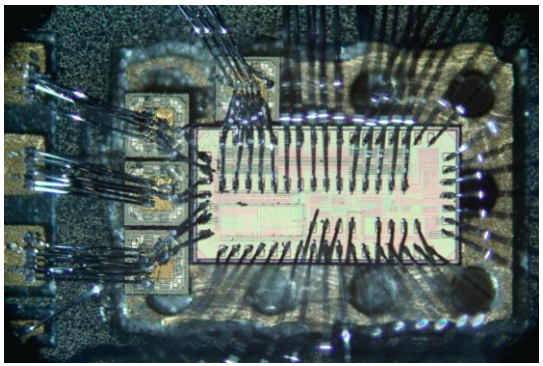
$$\eta_8 \approx 44.4\ \%$$

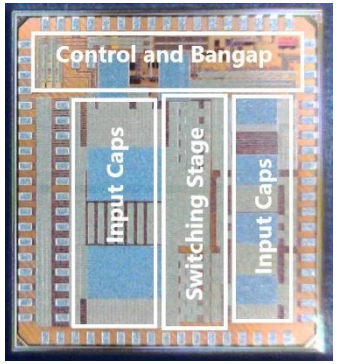
$$\eta_{16} \approx 76.2\ \%$$

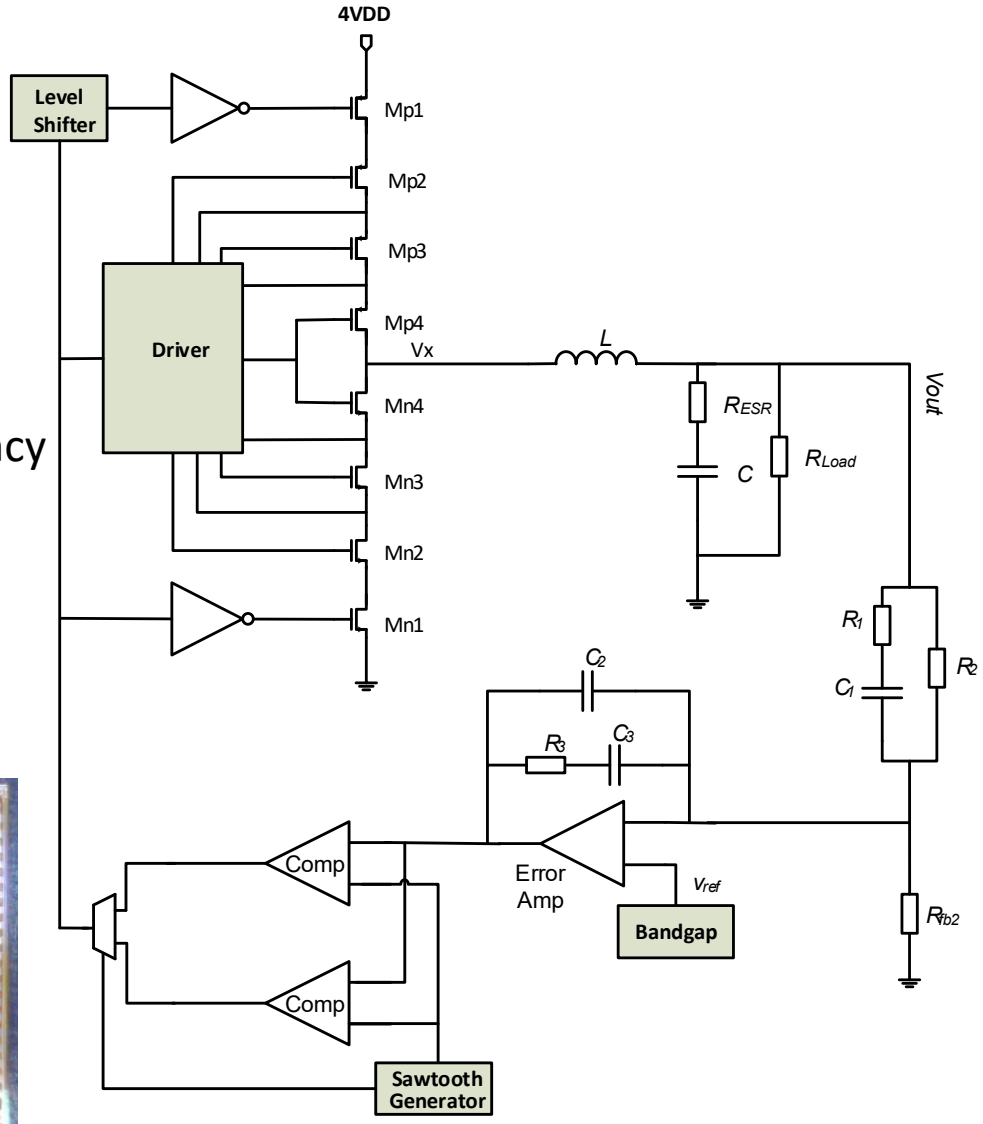
- Multi-stage approach to reach required conversion factor

High-Frequency DCDC Buck Converter

- cascoded switching stage
  - high radiation tolerance
  - high voltage handling
- high switching frequency (100 MHz)
  - requires small inductance
  - low volume air coil
- control circuitry optimized for high frequency
  - crosstalk and kickback issues to solve
- Ringing mitigation
  - External bondable capacitors
  - On-chip capacitors

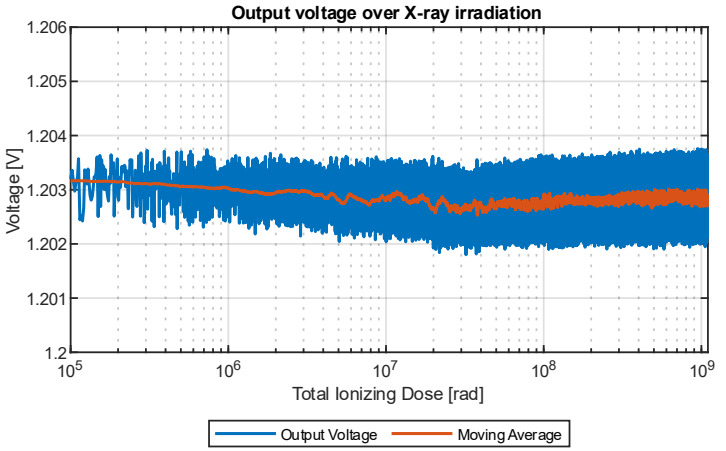




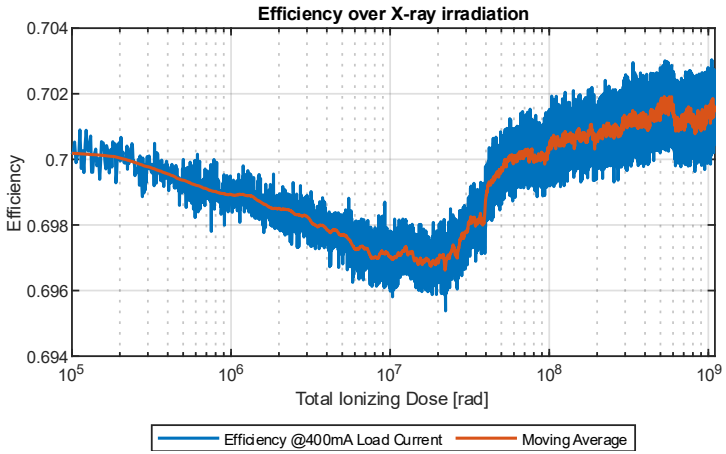


X-Ray Irradiation Campaign

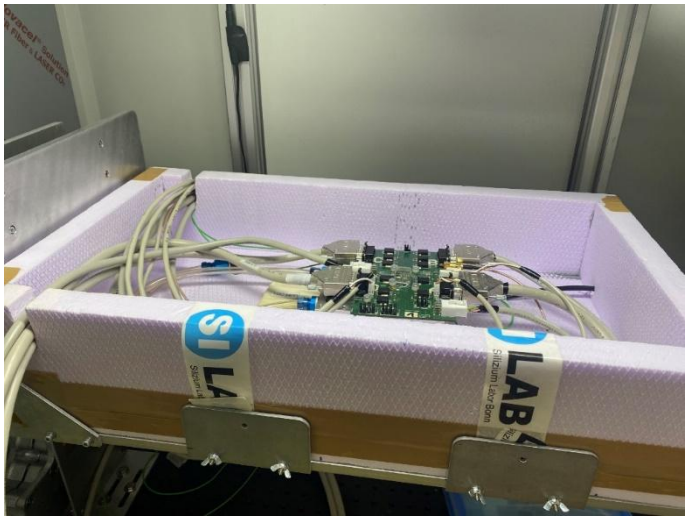
- Chip irradiated with X-rays at 2Mrad/h
- 1 Gigarad Total Ionizing Dose reached after 3 weeks
- Low temperature -15°C to match experiment conditions



variation < 0,2 %

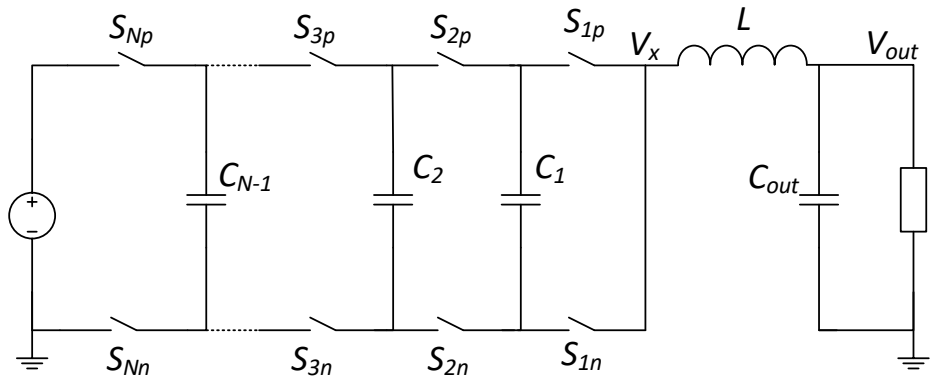


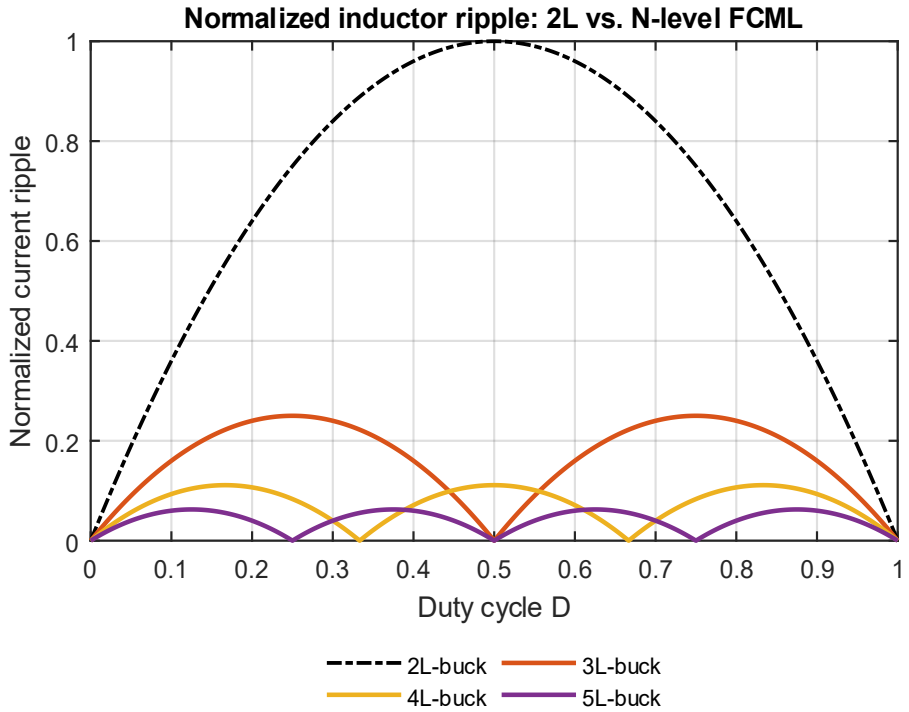
variation < 1 %



Flying Capacitor Multi Level Converter

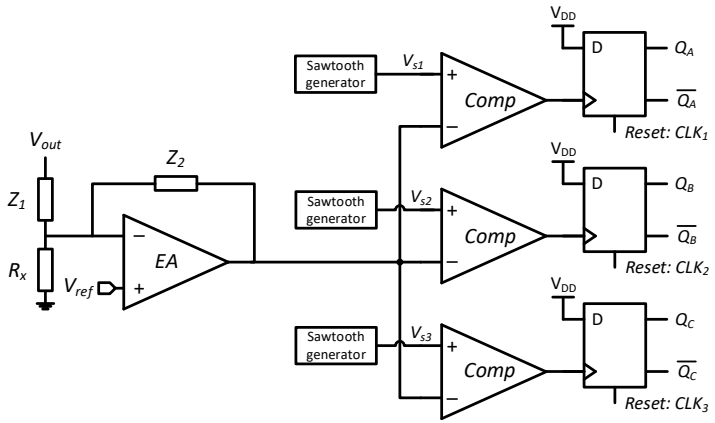
- N = number of voltage ripples at V
- Effective switching rate seen by L and C: $f_{eff} = (N - 1)f_{sw}$
- More voltage levels N
  - → smaller ripple
  - → smaller L & C
- Voltage/Capacitor ripple scales with $\frac{1}{(N-1)}$
- Current/Inductor ripple scales with $\frac{1}{(N-1)^2}$

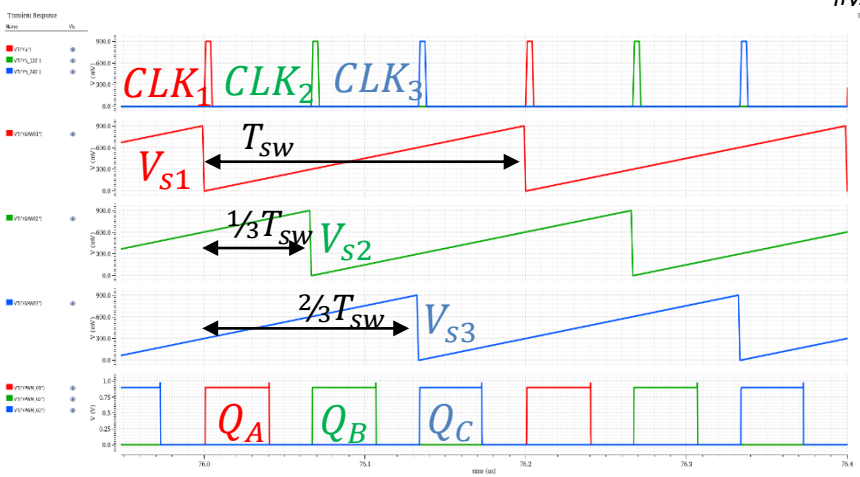


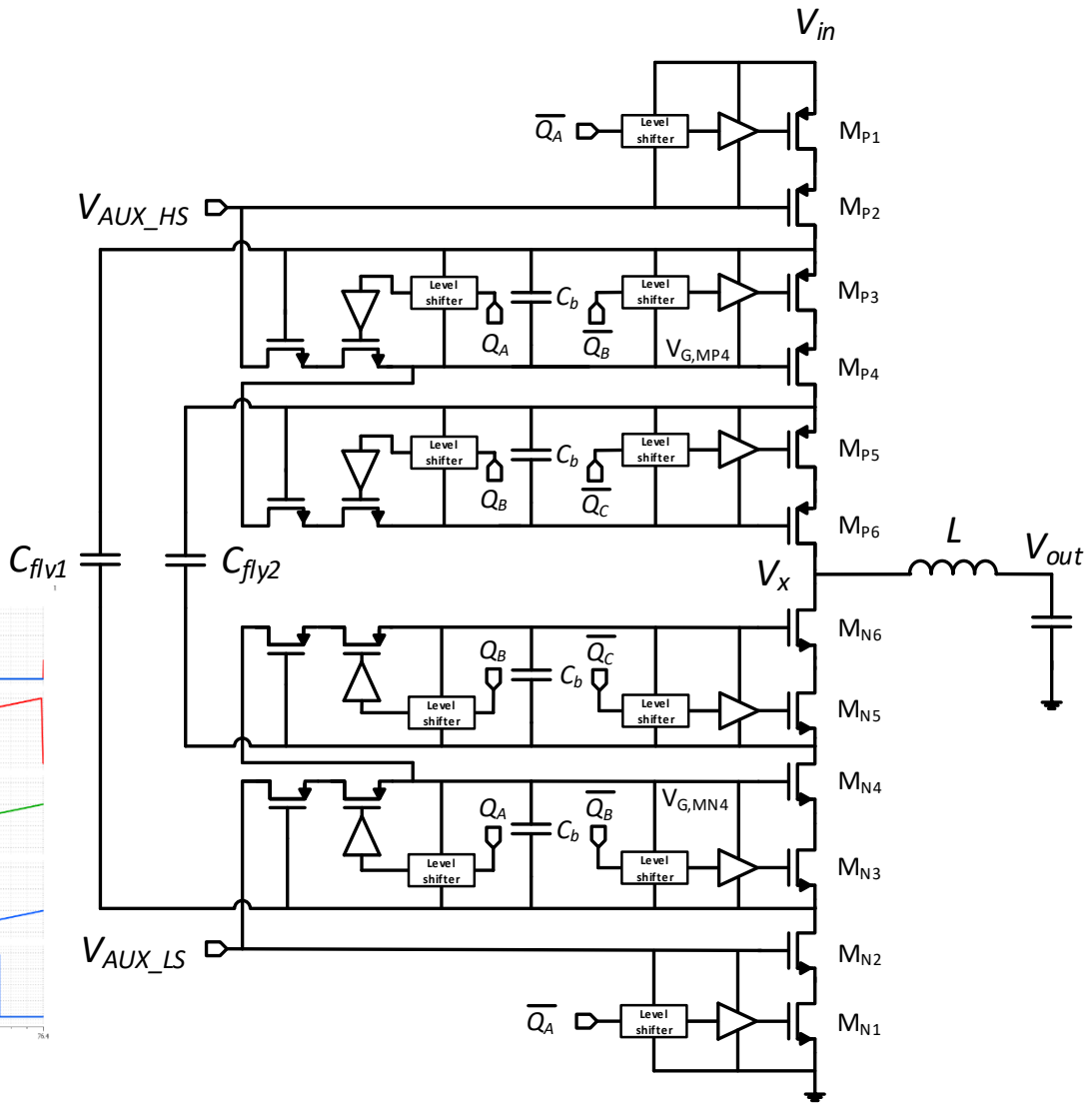


- 5 – 10 MHz switching frequency with small volume air core inductors
- Cascoding & flying capacitors allows higher V_{in} while using thin gate oxide transistors (no HV-devices necessary)

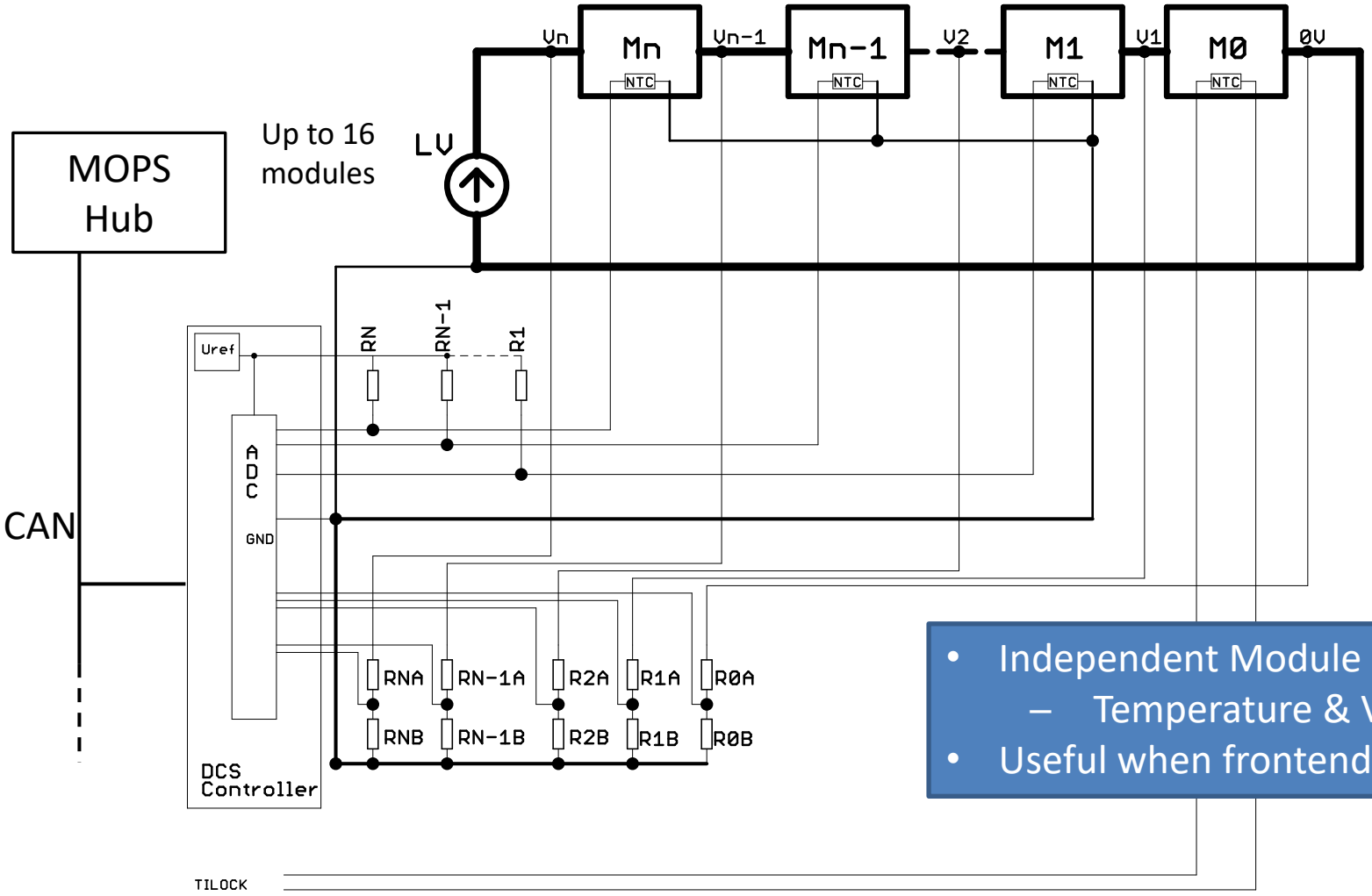
Radhard FCML 4-Level buck converter in 28nm





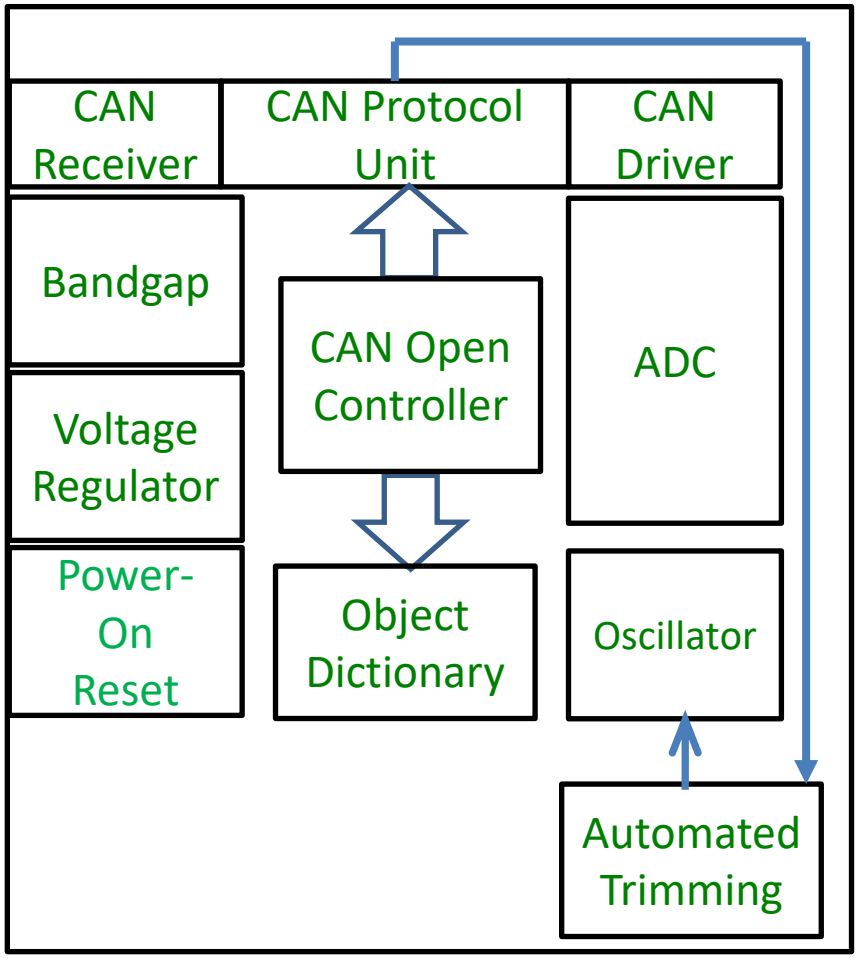


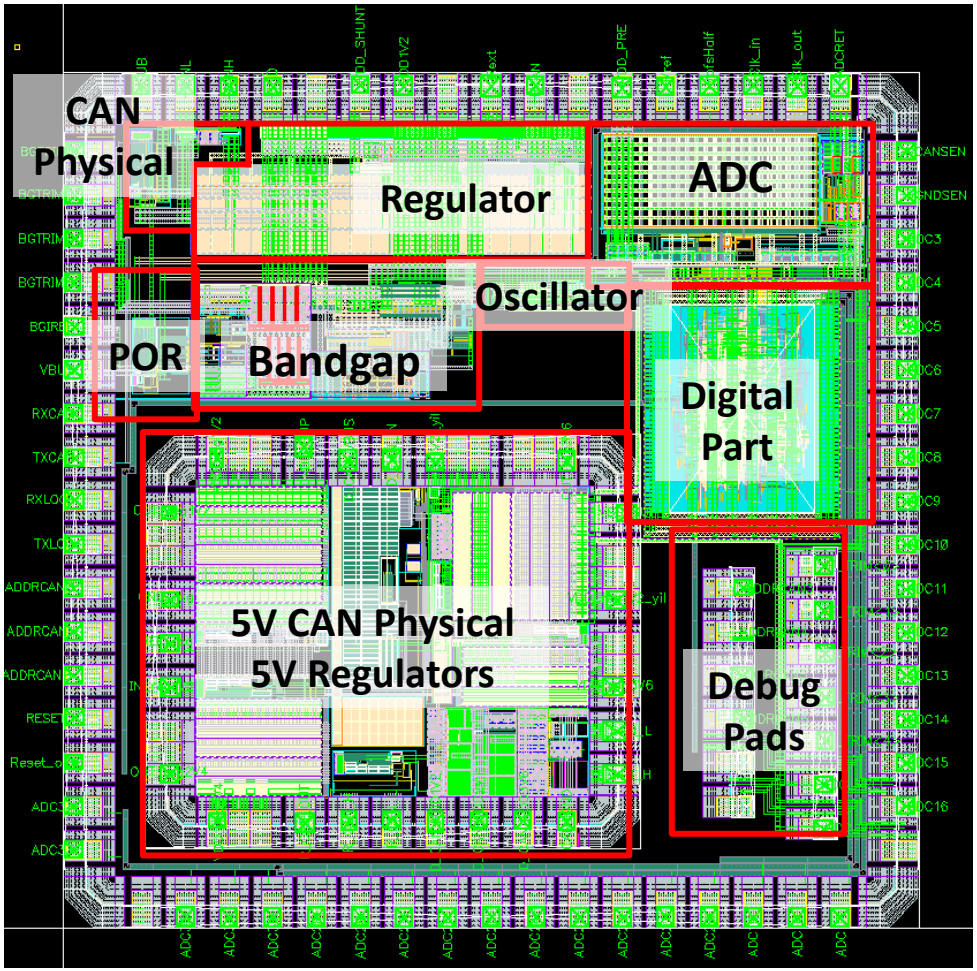
Monitoring of Pixel System (MOPS)



- Independent Module Monitoring
  - Temperature & Voltage
- Useful when frontends are offline

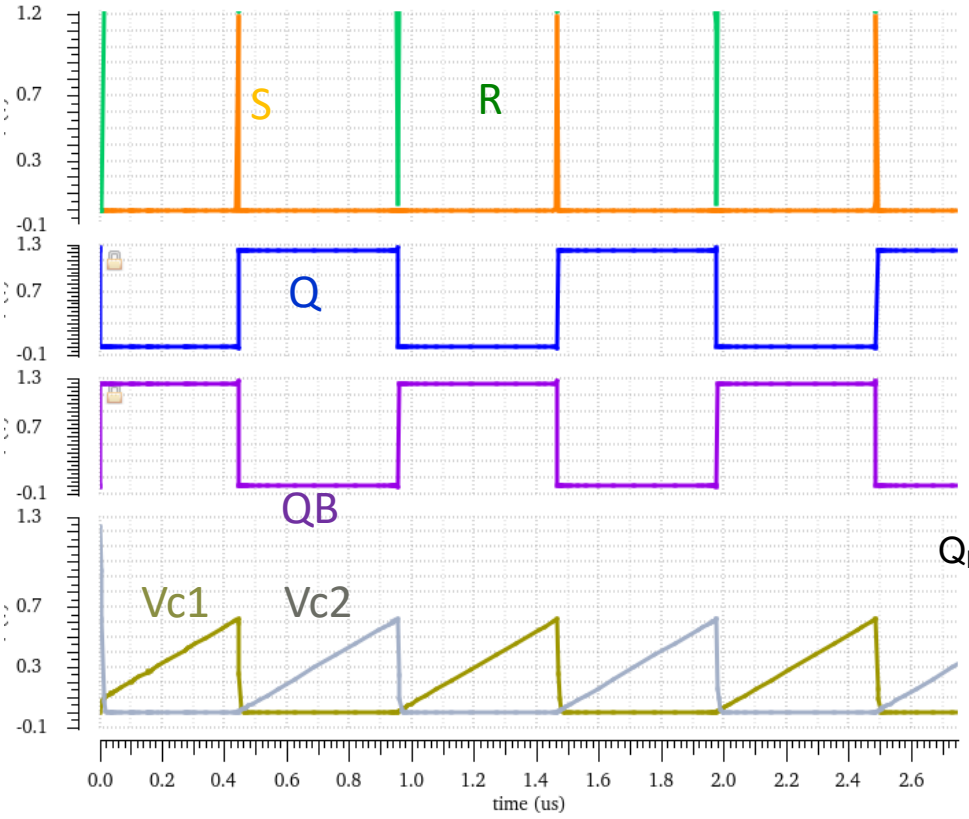
MOPS Chip Architecture

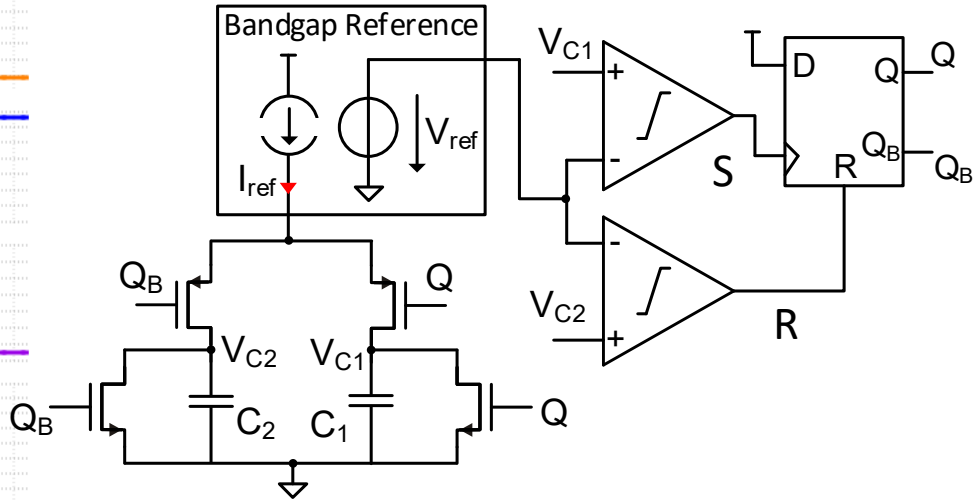




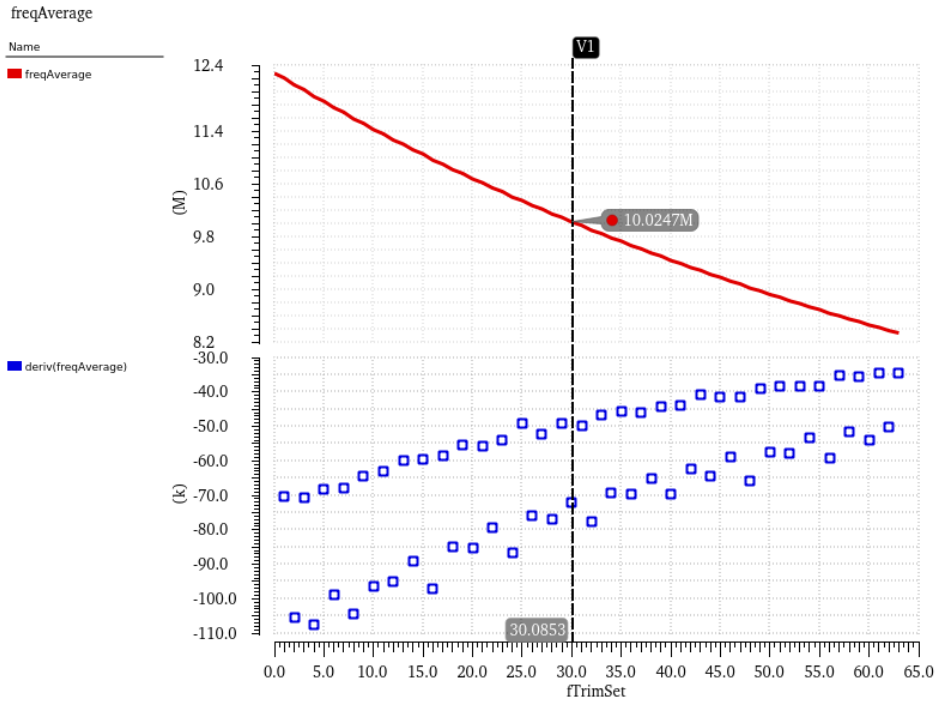
Relaxation Oscillator Design

- With CAN, data is transmitted without a clock signal
- CAN nodes require their own oscillator for synchronization
- MOPS uses a relaxation oscillator
- Two capacitors are alternately charged and discharged





Compensation for Production Variations



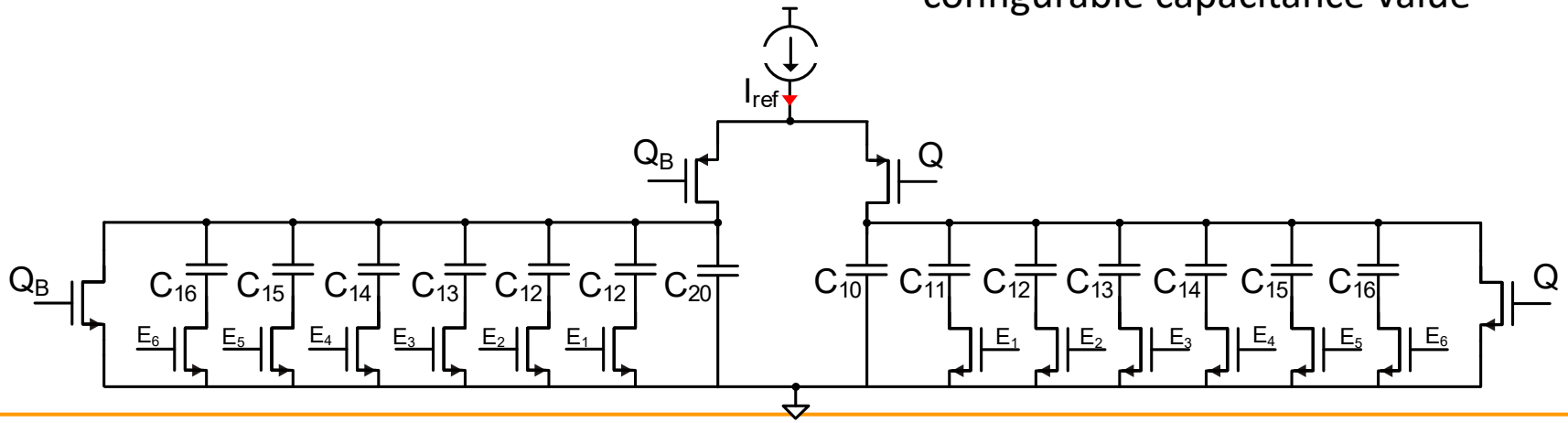
Oscillator frequency is influenced by

- process variations
- temperature
- radiation

$$f = \frac{I_{REF}}{2CVref}$$

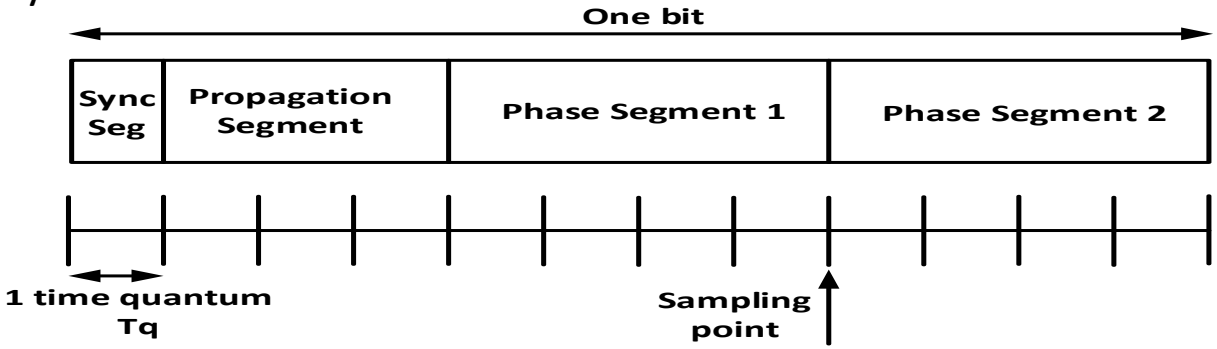
To ensure stable CAN communication, the oscillator frequency must not vary by more than 3%.

- frequency trimming introduced
- configurable capacitance value

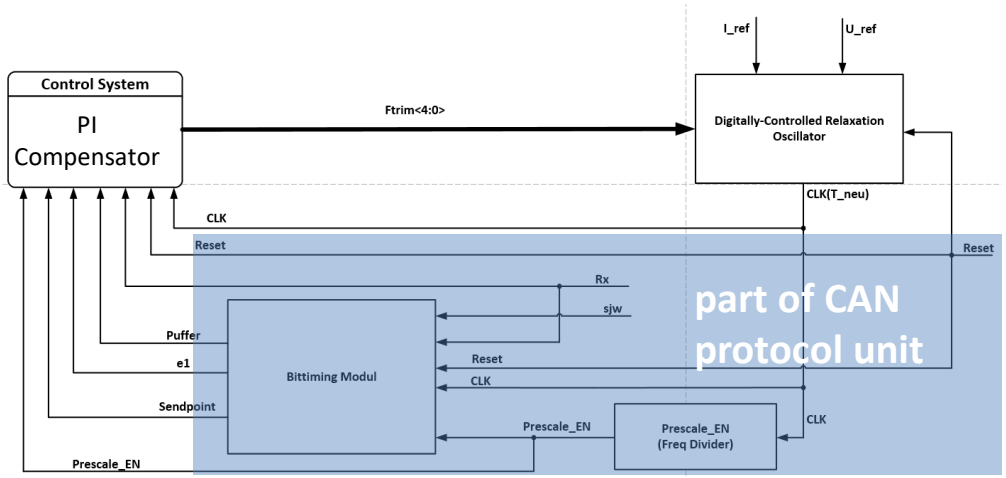


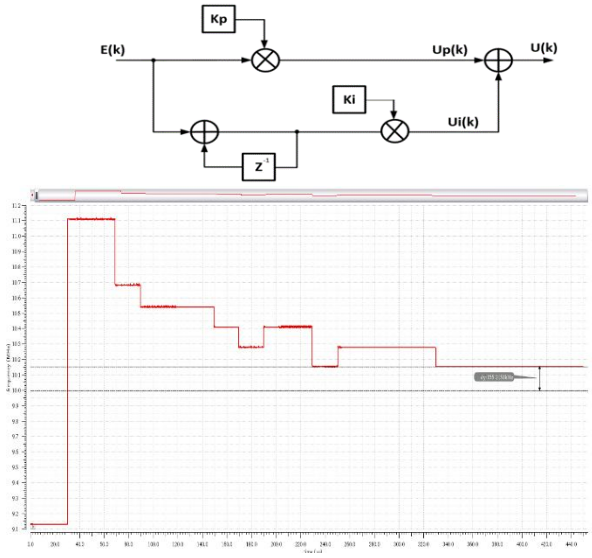
Automatic Frequency Calibration

- The bit timing functionality of the CAN protocol unit performs phase correction by default to establish synchronization between the transmitter and receiver



- Phase error signal of the bit timing unit is fed to a digital PI controller, which trims the frequency of the oscillator.



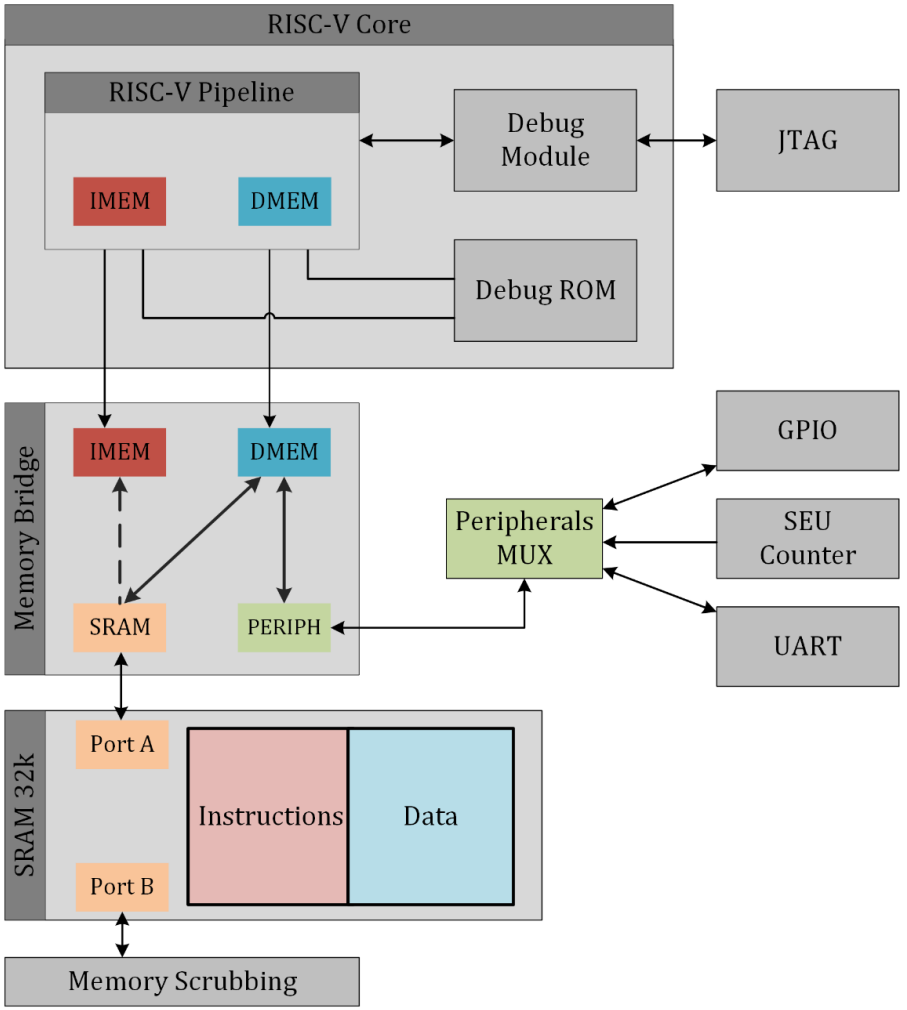


CAN Open Communication

- **CANopen** is a higher-layer protocol and device model on top of **CAN**
  - Defines a standard application interface and communication scheme
- data is organized in the **Object Dictionary**
  - 16-bit index + 8 bit subindex
  - 0x1000 Device type, 0x1001 Error register, 0x1018 Identity, 0x1400/0x1600… RPDO/TPDO comms & mapping, 0x2000–0x5FFF manufacturer-specific
- communication methodology based on Objects
  - Process Data Objects **(PDO)**
    - small messages for fast event-driven process data exchange
  - Service Data Objects **(SDO)**
    - multi frame communication
- CAN is implemented in hardware CANopen is usually implemented in software
  - No experience with microcontroller integration (back then)
  - No microcontroller core available with proven radiation hardness for LHC inner layers
- **An integrated microcontroller core would have made the MOPS chip very versatile**
  - **Usage as configurable sensor and/or power management node**

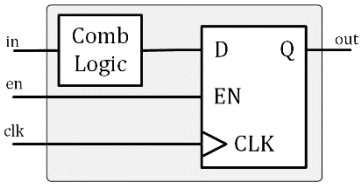
STRV Microcontroller Architecture

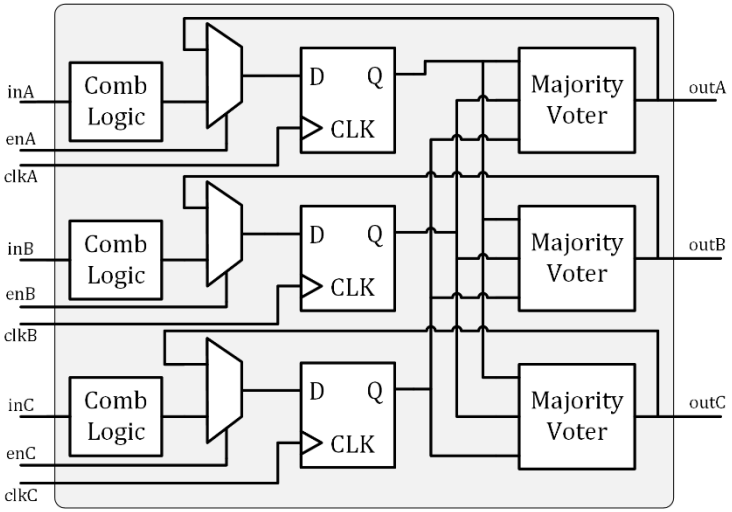
- AIRES RISC-V core from Fraunhofer IMS
  - RV32-IMC Core
  - 3 stage pipeline
- JTAG Interface
  - JTAG TAP & debug module
  - Non-volatile debug ROM with debug ISR
- Peripherals
  - Memory mapped registers
  - UART
  - GPIOs
- 32KByte Dual Port SRAM
- Separate power domains for
  - RISC-V Core
  - SRAM
  - periphery und pad ring
- thing-gate-oxide core-transistor-only implementation for high TID robustness



SEE Protection Scheme of Logic

- Full Triple modular redundancy (TMR)

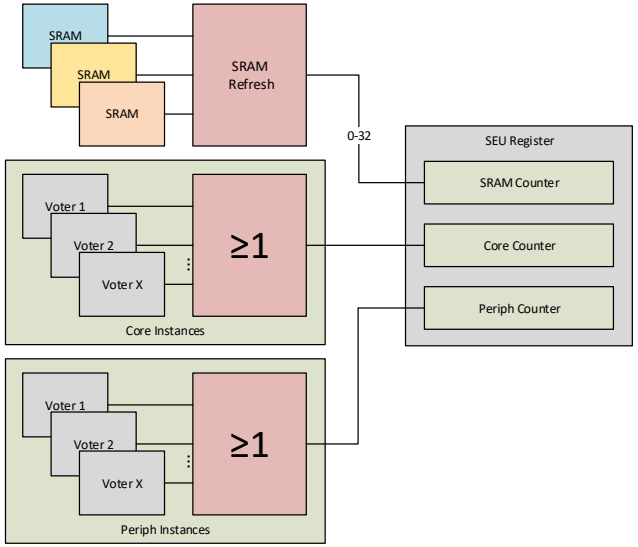




  - Triplication of combinatoric logic & FFs
  - Three clock trees
  - Three majority voter
  - 15 µm distance between triplicated instances

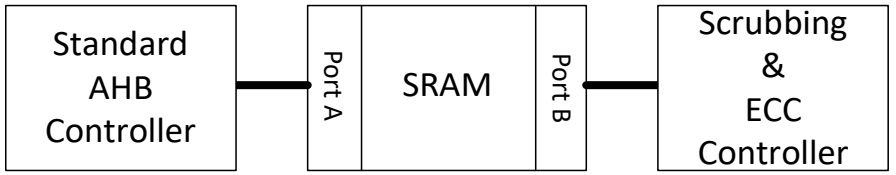
- STRV-1 has even three pads for clock, reset and JTAG

- SEU counter counts corrected SEUs per domain
  - SEU detection signals of all majority voters OR-ed
  - detects one SEU per clock cycle per domain



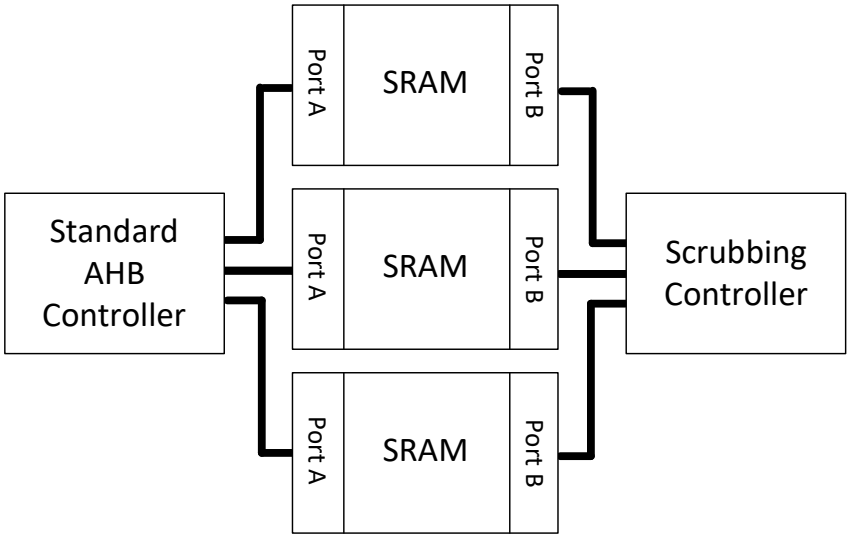
SEE Protection Scheme of SRAM

- Scrubbing with ECC
  - Data is stored in SRAM protected by ECC (e.g., Hamming code)
  - Memory is read cyclically
  - Detected errors are corrected
  - Corrected data is written back



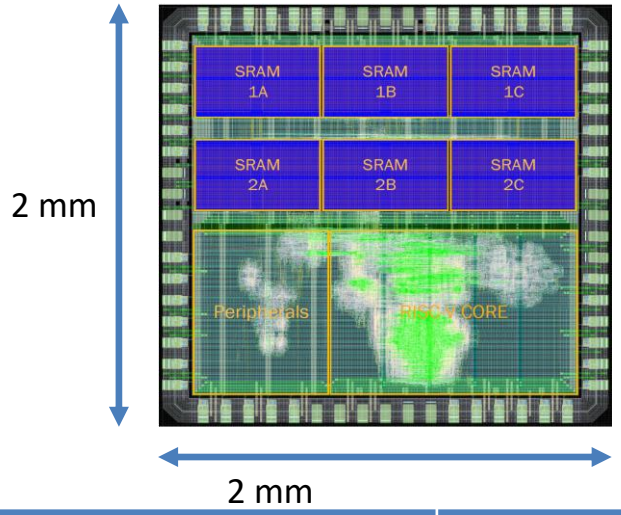
- Problem
  - Hardening level of address logic in commercial SRAM macros is unknown
  - If the address decoder is hit, corrected data may be written to the wrong address

- Scrubbing with Triplication
  - 3 SRAM macros are written/read in parallel
  - Allows for multiple bit error correction
  - Has huge chip area penalty

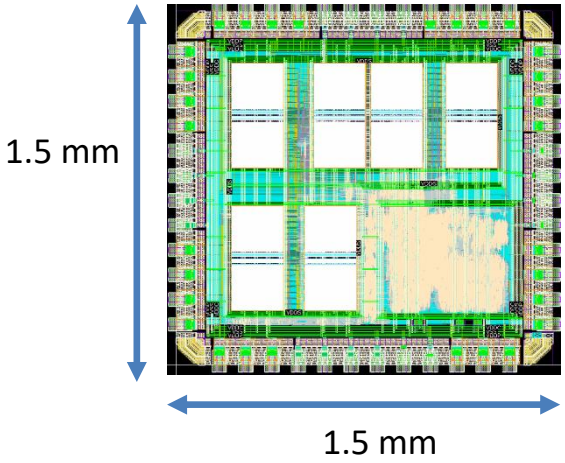


STRV-1/2 Microcontroller Features

STRV-1 (65nm)



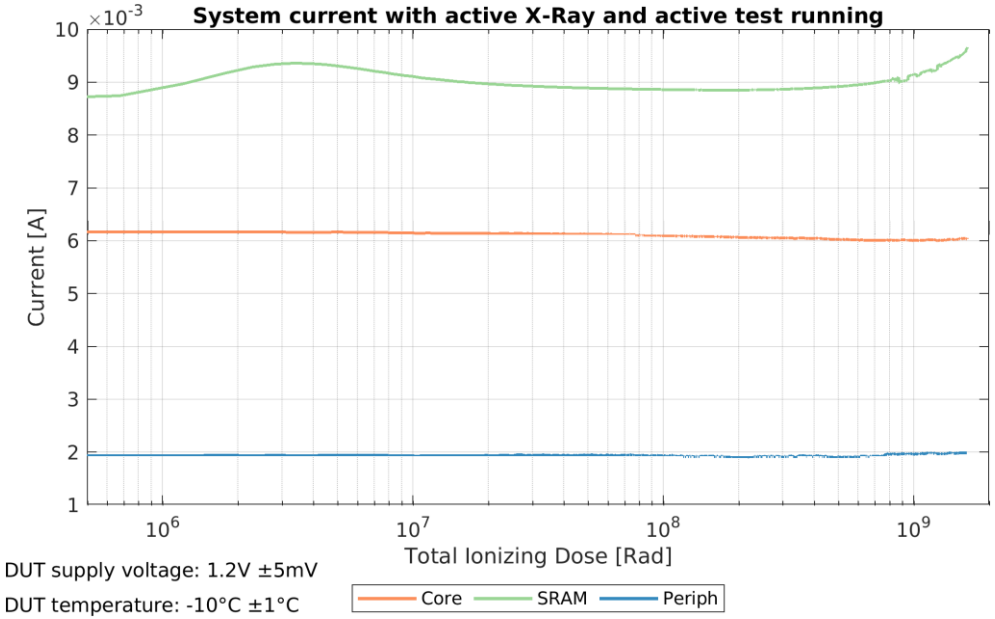
STRV-2 (28nm)

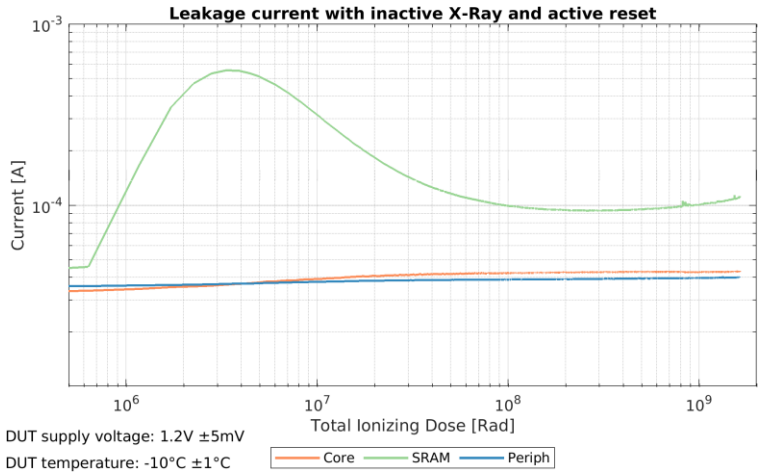


	STRV-1	STRV-2
Frequency	50 MHz	100 MHz
Supply Voltage	1.2V	0.9V
Power with Scrubbing	20 mW	17 mW
Power without Scrubbing	15 mW	12 mW
TID hardness	1 Gigarad	1 Gigarad
SEE hardness	2.2 SEFI/h @ 10^9 p/cm²/s	-

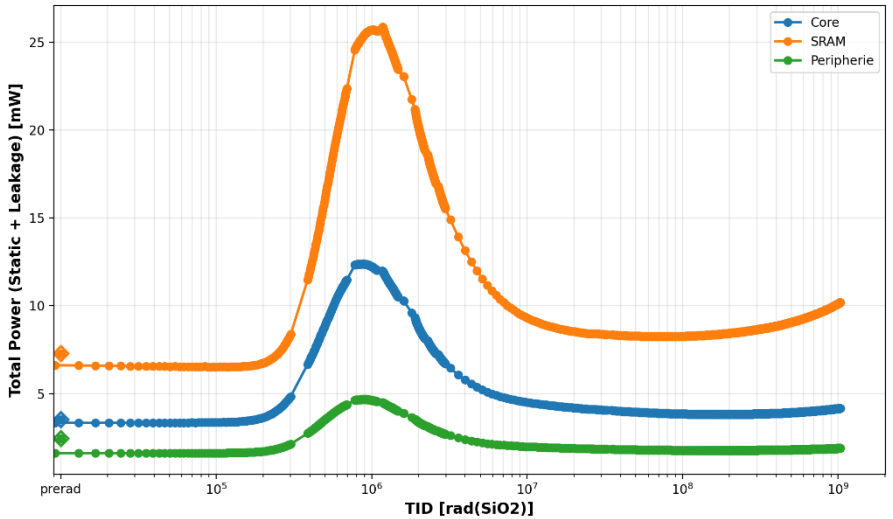
TID Characterization with X-Rays

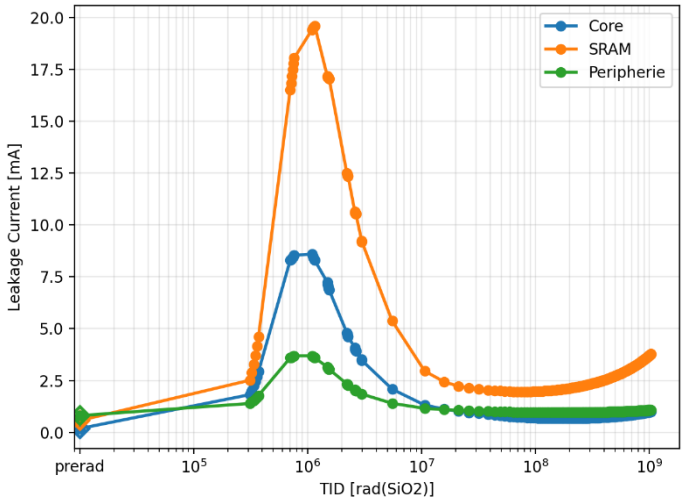
STRV-1 (65nm)





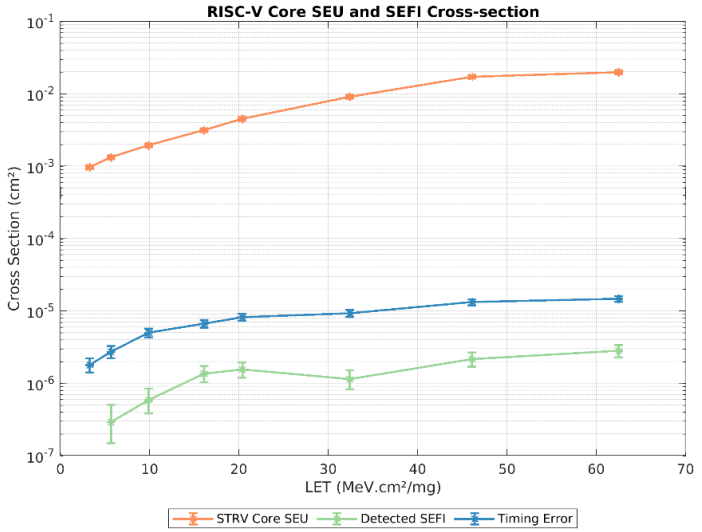
STRV-2 (28nm)





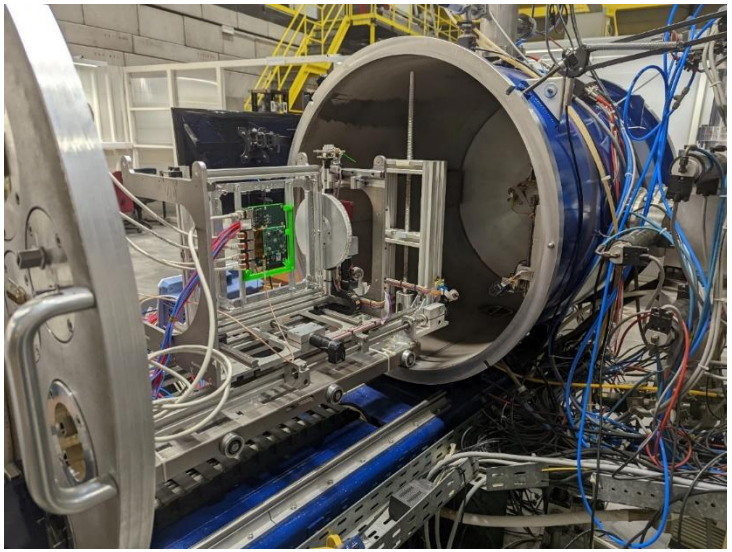
STRV-R1 | Heavy-Ion Irradiation SEFI

- Despite the SEE mitigation techniques SEFIs occur
  - SEFIs observed during heavy-ion Irradiation
    - corrupted data, delay, time-out
  - Average improvement over SEU cross-section
    - At low LETs (<16 MeV.cm²/mg): 2800x
    - At high LETs (>32 MeV.cm²/mg): 7700x
- Estimated SEFI rate in HL-HLC environment
  - SEE particle flux 1 × 10^9 p/cm²/s
  - 2.2 Chip level SEFI per hour



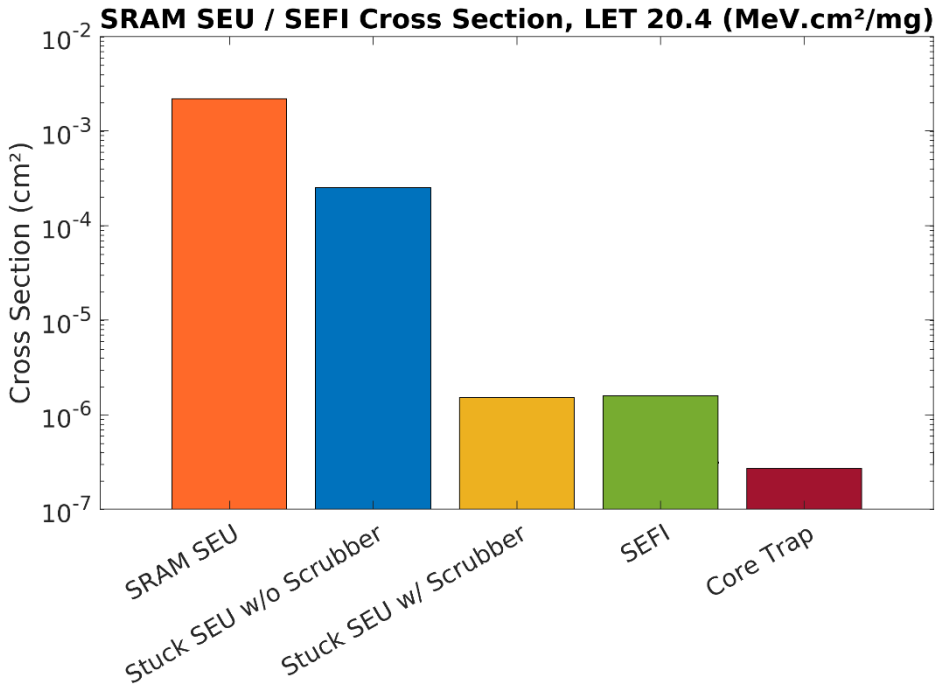
Cross-section	L_0 [$\frac{MeVcm^2}{mg}$]	$\sigma_{HI\infty}$ [cm^2]	$L_{0.25}$ [$\frac{MeVcm^2}{mg}$]	$\sigma_{p\infty}$ [cm^2]
SEU	< 1.0	4.27×10^{-2}	18.87	2.66×10^{-9}
SEFI	< 5.7	2.95×10^{-6}	10.32	6.15×10^{-13}
Timing	< 3.3	2.86×10^{-5}	19.95	1.58×10^{-12}

Cross-section	$\sigma_{p\infty}$ [cm^2]	[a] Φ [$\frac{Hz}{cm^2}$]	Event rate [Hz]	Events / h [$\frac{1}{h}$]
SEU	2.66×10^{-9}	1×10^9	2.66	8.14×10^3
SEFI	6.15×10^{-13}	1×10^9	6.15×10^{-4}	2.21

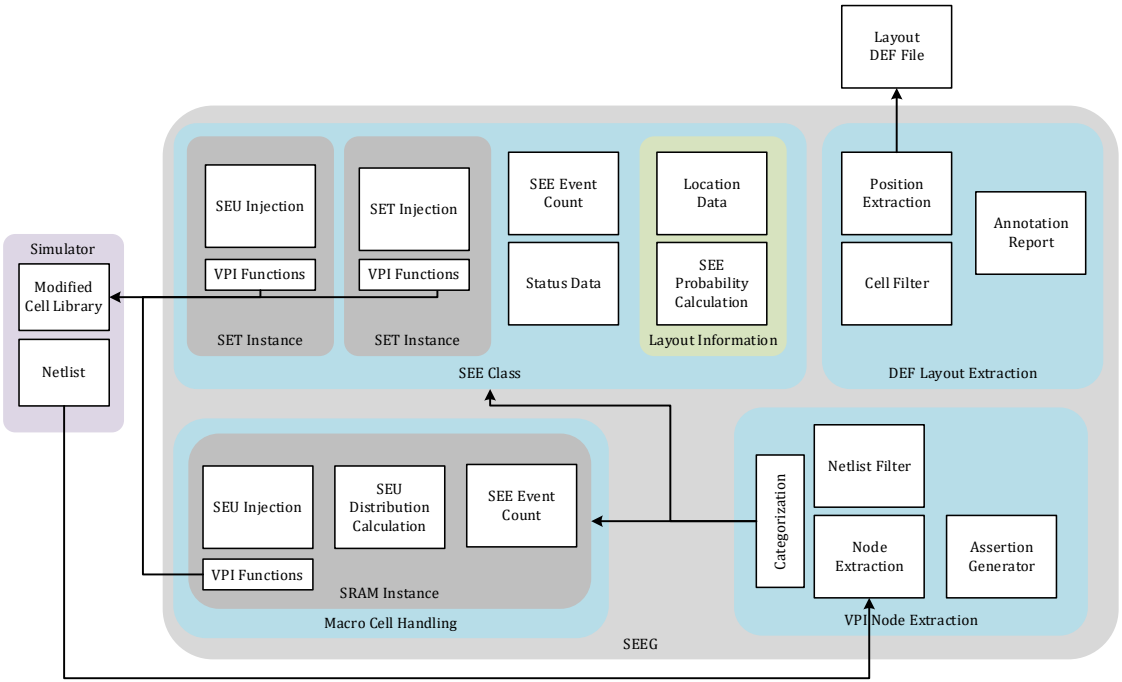


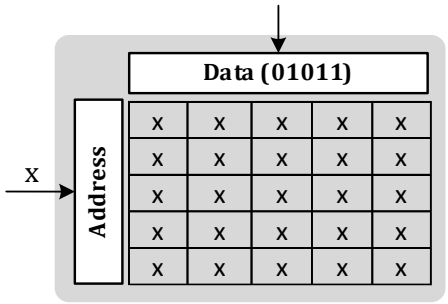
SEFI and SRAM Stuck-SEU rate comparison

- Special heavy ion irradiation campagne for SRAM study
- SEFI and Stuck-SEU SRAM cross-section very similar
- Analysis of SRAM content indicates correct data has been stored in wrong address
- TMR protection of SRAM logic not correctly implemented

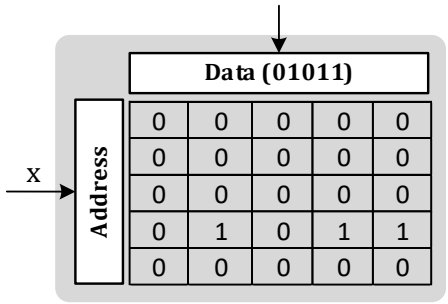


SEE Injection Simulation Framework





Default foundry SRAM model

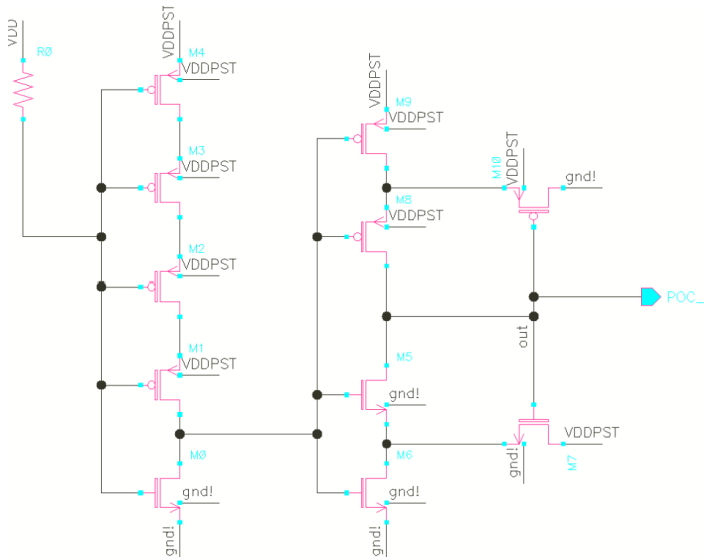


Modified foundry SRAM model

- Testbench based on VPI functions
- Post-synthesis/implementation netlist processed
- physical position of cells included from DEF file
- SEU/SET/Marco fault injection
- PRNG for randomness and reproduceability
- Filtering options: nodes/cell-names/cell-type
- Modified SRAM and standard cell libraries to avoid x at timing violations
- Automatic generation of assertions to check correct implementation of TMR

Preliminars SEE Heavy Ion Characterization Results of 28nm Design STRV-2

- No crashes observed
  - No call of the trap handler, UART data arrive timely and free of errors
- Resets seldomly observed
  - Execution time of benchmark reduced signifcantly
  - SEU registers reset to zero
- SEU in Power-On-Control circuit triggers low-active reset



SEU SENSITIVITY OF THE POC CELL DERIVED FROM GPIO GLITCH MEASUREMENTS.

Ion	Flux [10^4 ions/cm^2 s]	Time [s]	Fluence [10^7 ions/cm^2]	Glitches [#]	σ_{POC} [10^{-6} cm^2]
Ni	1.5	469.44	0.70	5	0.71
Xe	1.5	670.14	1.01	11	1.09

- Variation of benchmark execution time

TABLE VII
DELAY-SEFI STATISTICS FROM EXECUTION TIME DEVIATIONS.

Bench.	Ion	Fluence [10^7 ions/cm^2]	Events [#]	σ_{delay} [10^{-6} cm^2]	Mean ΔT [cycles]
Dhrystone	Ni	1.79	61	3.41	2.33
Dhrystone	Xe	1.34	66	4.91	4.32
Matrix Mult.[a]	Ni	1.99	33	1.66	2.33
Matrix Mult.[a]	Xe	1.35	92	6.79	2.93
March SRAM	Ni	1.82	93	5.11	2.09
March SRAM	Xe	1.37	120	8.78	3.20
Qsort	Ni	1.81	76	4.19	1.96
Qsort	Xe	1.36	129	9.49	3.16

[a] Usage of the Multiply/Divide Integer Extension

Summary / Conclusion / Outlook

- **Radiation-hard ASICs are a key enabling technology**
  - for the High-Luminosity Upgrade LHC future and beyond
- **Reliable power management** requires dedicated circuit concepts
  - Serial powering - Shunt-LDO regulators
  - High-frequency and multilevel DC/DC converters
- **Radiation tolerance must be addressed across all abstraction levels**
  - from device physics and circuit design to architecture, verification, and system integration.
- **Radiation-hardened RISC-V microcontrollers** enable flexible detector control while combining TID robustness with comprehensive SEE mitigation.
- **Current research is extending these concepts towards on-detector intelligence based on radiation-hard AI/ML accelerators, high-bandwidth LPDDR memory interfaces, and next-generation reliable computing platforms.**

Bibliography

[1] Evans, Lyndon, and Philip Bryant. "LHC machine." *Journal of instrumentation* 3.08 (2008): S08001.

[2] AIRAPETIAN, A., et al. ATLAS detector and physics performance: Technical Design Report, 1. ATLAS-TDR-014, 1999

[3] AAD, G., et al. ATLAS pixel detector electronics and sensors. Journal of instrumentation, 2008, 3. Jg., Nr. 07, S. P07007

[4] MENG, Lingxin. Atlas itk pixel detector overview. arXiv preprint arXiv:2105.10367, 2021

[5] FACCIO, F. Radiation issues in the new generation of high energy physics experiments. International Journal of High Speed Electronics and Systems, 2004, 14. Jg., Nr. 02, S. 379-399

[6] STOCKMANNS, Tobias, et al. Serial powering of pixel modules. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2003, 511. Jg., Nr. 1-2, S. 174-179

[7] KARAGOUNIS, Michael, et al. An integrated Shunt-LDO regulator for serial powered systems. In: 2009 Proceedings of ESSCIRC. IEEE, 2009. S. 276-279.

[8] KAMPKÖTTER, Jeremias, et al. Characterization and verification of the Shunt-LDO regulator and its protection circuits for serial powering of the ATLAS and CMS pixel detectors. In: Journal of Physics: Conference Series. IOP Publishing, 2022. S. 012071.

[9] KAMPKÖTTER, Jeremias, et al. SISSA: Stabilization and Protection of the Shunt-LDO regulator for the HL-LHC pixel detector upgrades. *PoS*, 2020, S. 067.

Bibliography

[10] KAMPKÖTTER, Jeremias; KARAGOUNIS, Michael; GRABMAIER, Anton. Step-down converter with stacked core transistors for the innermost layers of high-luminosity high-energy physics experiments. *IEEE Transactions on Nuclear Science*, 2024

[11] KAMPKÖTTER, Jeremias; KARAGOUNIS, Michael; KOKOZINSKI, Rainer. A high frequency radiation hardened DC/DC-converter with low volume air core inductor. *Journal of Instrumentation*, 2024, 19. Jg., Nr. 01, S. C0 1052

[12] KAMPKOETTER, Jeremias; KARAGOUNIS, Michael; KOKOZINSKI, Rainer. Design and characterization of a cascode switching stage for high frequency radiation hardened DC/DC converters for the supply of future pixel detectors. *Journal of Instrumentation*, 2022, 17. Jg., Nr. 12, S. C12022

[13] AHMAD, Rizwan, et al. Second generation monitoring of pixel system (mops) chip for the detector control system (dcs) of the atlas itk pixel detector. *Journal of Instrumentation*, 2023, 18. Jg., Nr. 04, S. C04015.

[14] AHMAD, Rizwan. The monitoring of pixel system (mops) chip for the detector control system of the atlas itk pixel detector. In: Journal of Physics: Conference Series. IOP Publishing, 2022. S. 012094.

[15] WALSEMANN, Alexander, et al. SISSA: A CANopen based prototype chip for the Detector Control System of the ATLAS ITk Pixel Detector. PoS, 2020, S. 013

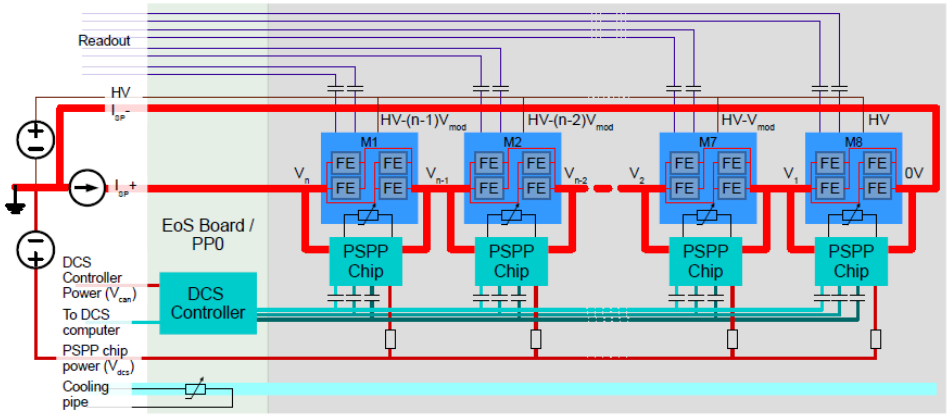
Bibliography

[16] WALSEMANN, Alexander, et al. STRV—a radiation hard RISC-V microprocessor for high-energy physics applications. Journal of Instrumentation, 2023, 18. Jg., Nr. 02, S. C02032.

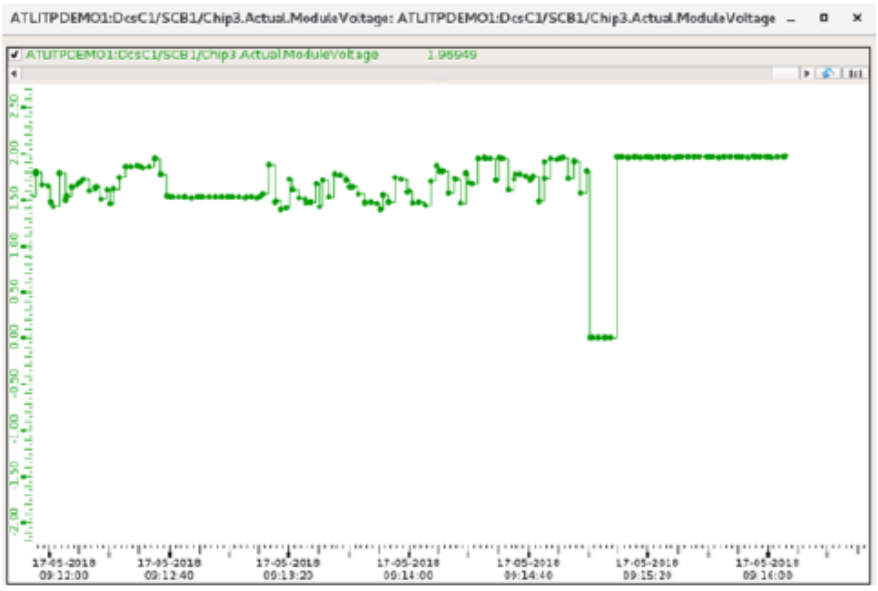
[17] WALSEMANN, Alexander, et al. A radiation hard RISC-V microprocessor for high-energy physics applications. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2023, 1056. Jg., S. 168633

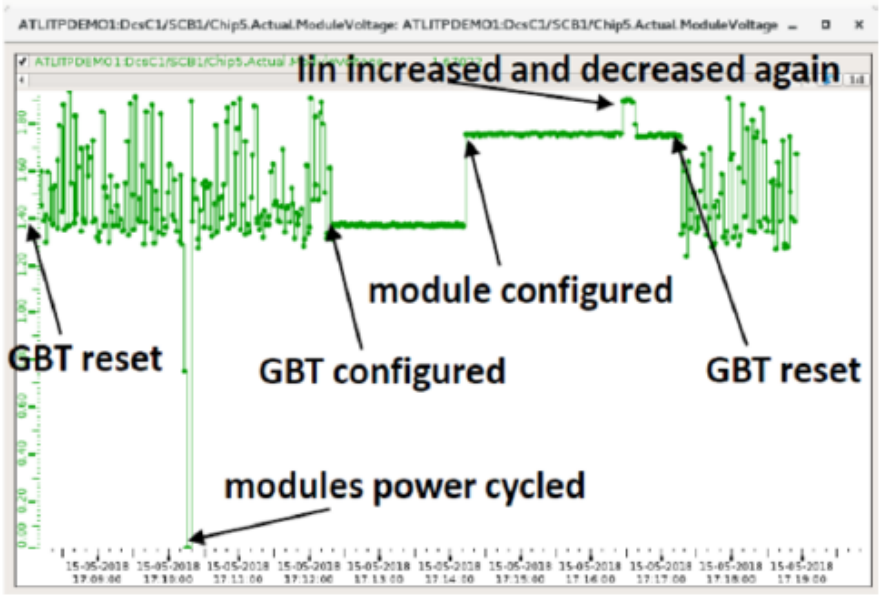
[18] WALSEMANN, Alexander, et al. Fault tolerance evaluation study of a RISC-V microprocessor for HEP applications. Journal of Instrumentation, 2024, 19. Jg., Nr. 02, S. C02012.

Lessons Learned Outer Barrel Demonstrator

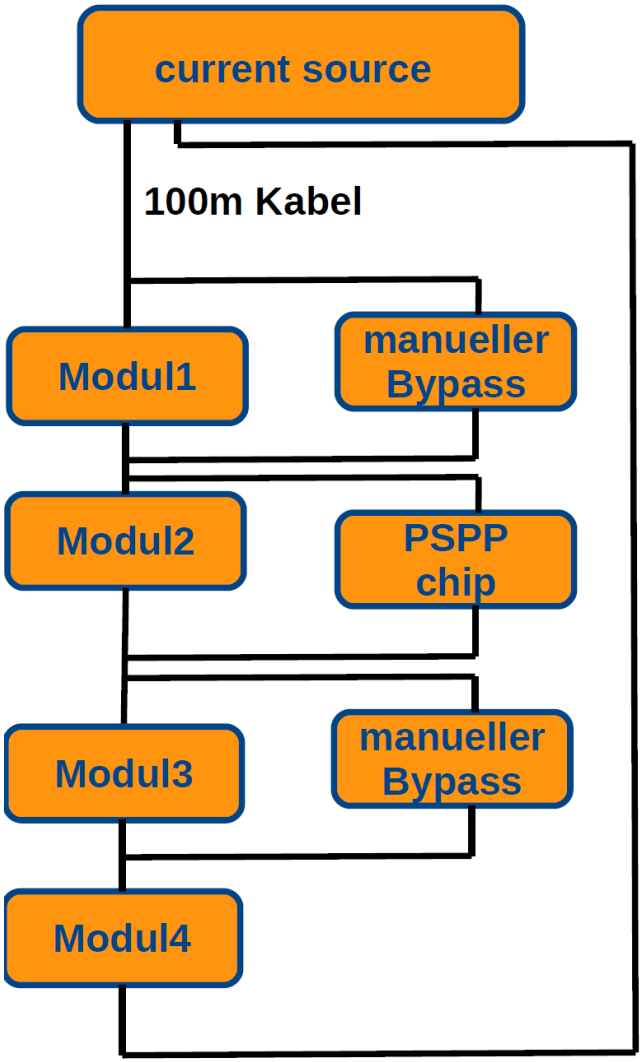


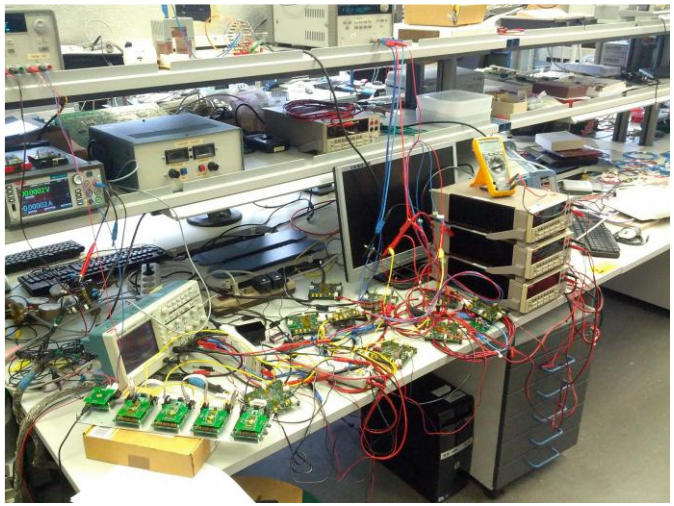
- FE-I4 quad module based serial chain
- Overload current situation reduces module (SLDO input) voltages

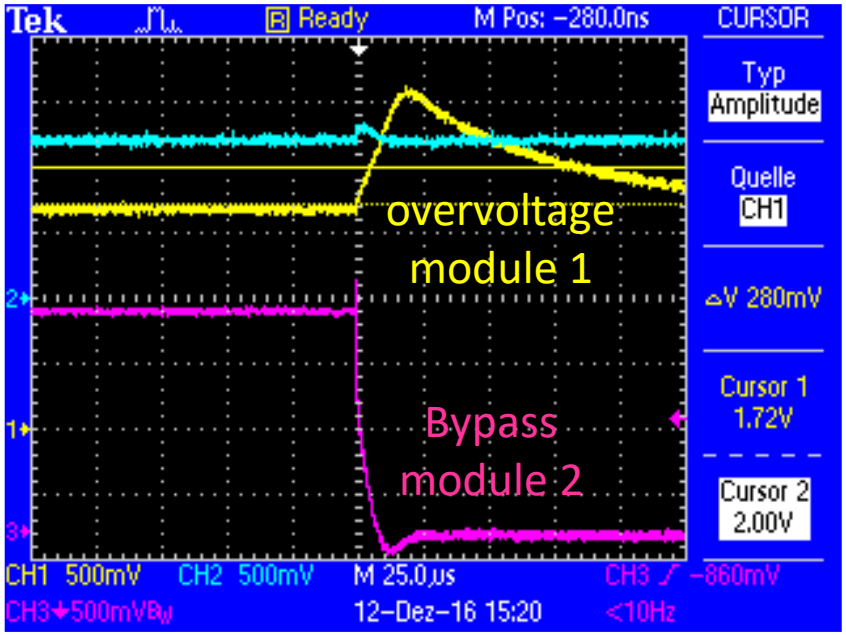




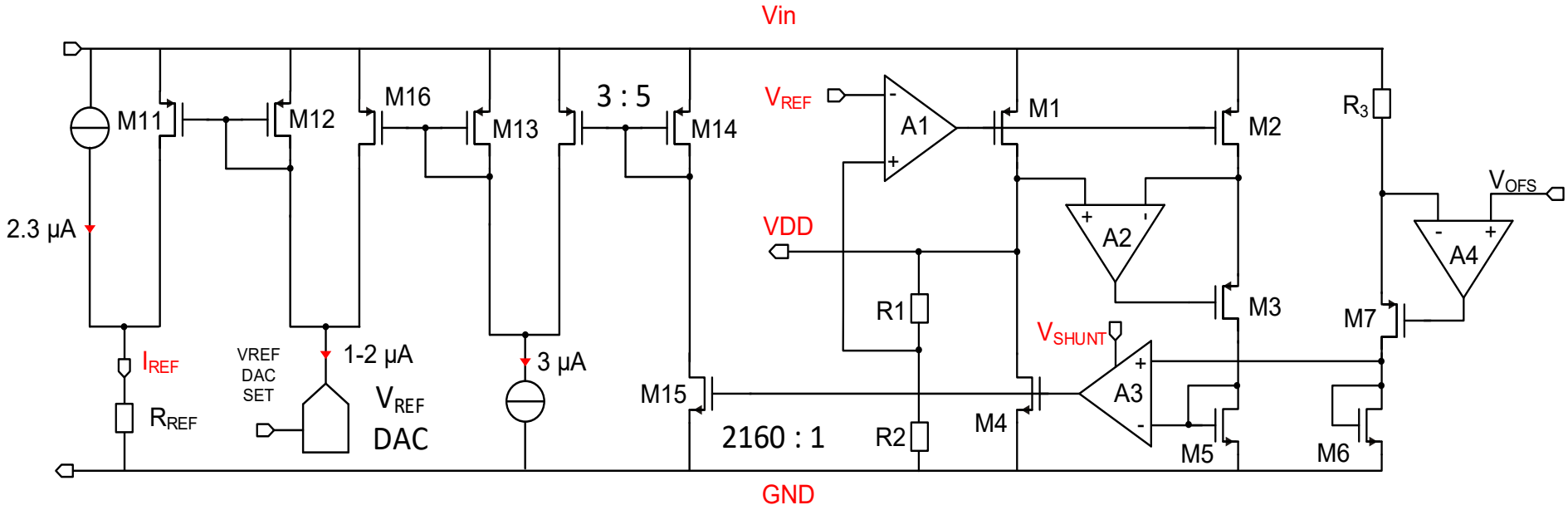
Bypass Tests







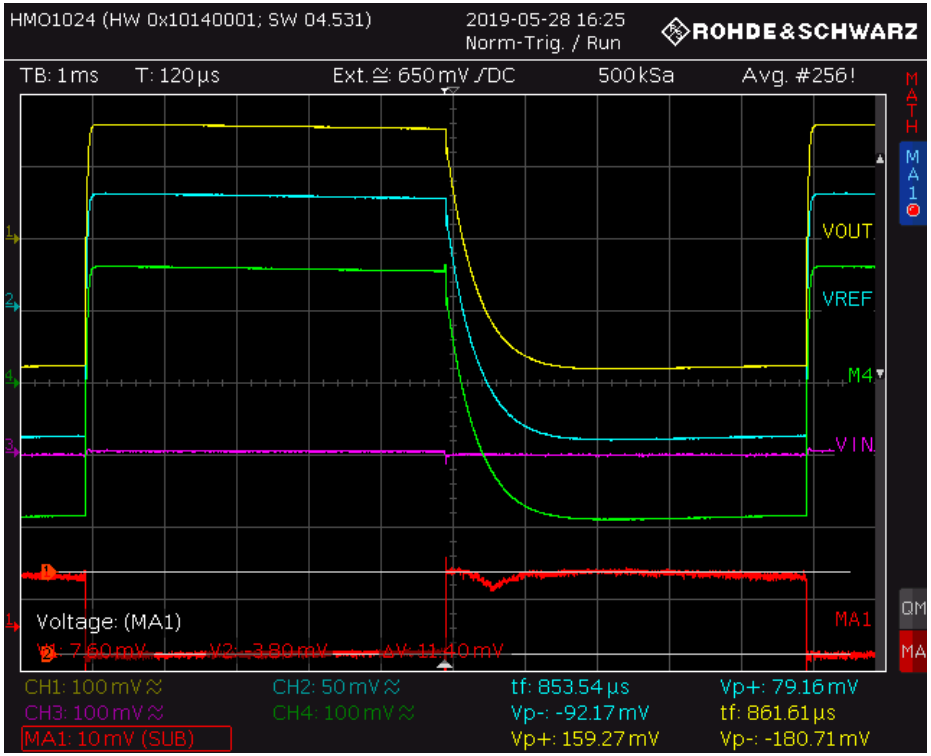
Protection Feature: Overload Protection



- With RD53A overload currents lead to collapse of regualtor input voltage
  - This lead to overvoltages at other modules in the serial chain
- RD53B protects against overloads which are considered as undershunt current scenarios
  - high load current reduces shunt current
- In undershunt current case Vout is reduced
  - Vout is lowered by lowering Vref
- Activation Threshold Ishunt < 10 mA
- Vout minimimum value 700mV → Vref minimum value 350 mV

Measurement of Overload/Undershunt Protection

Enabled



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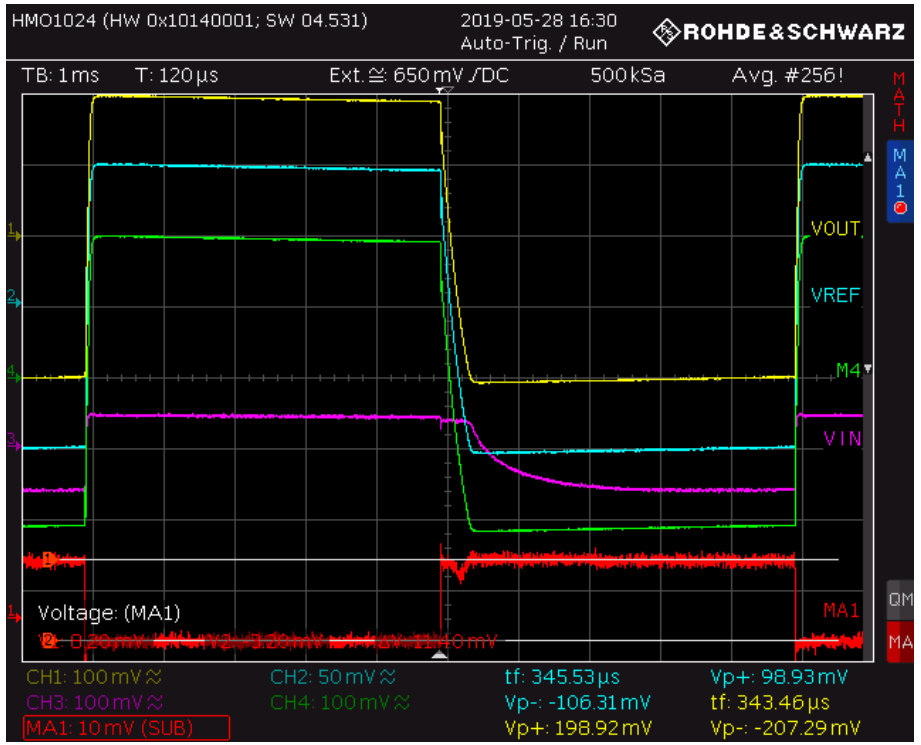
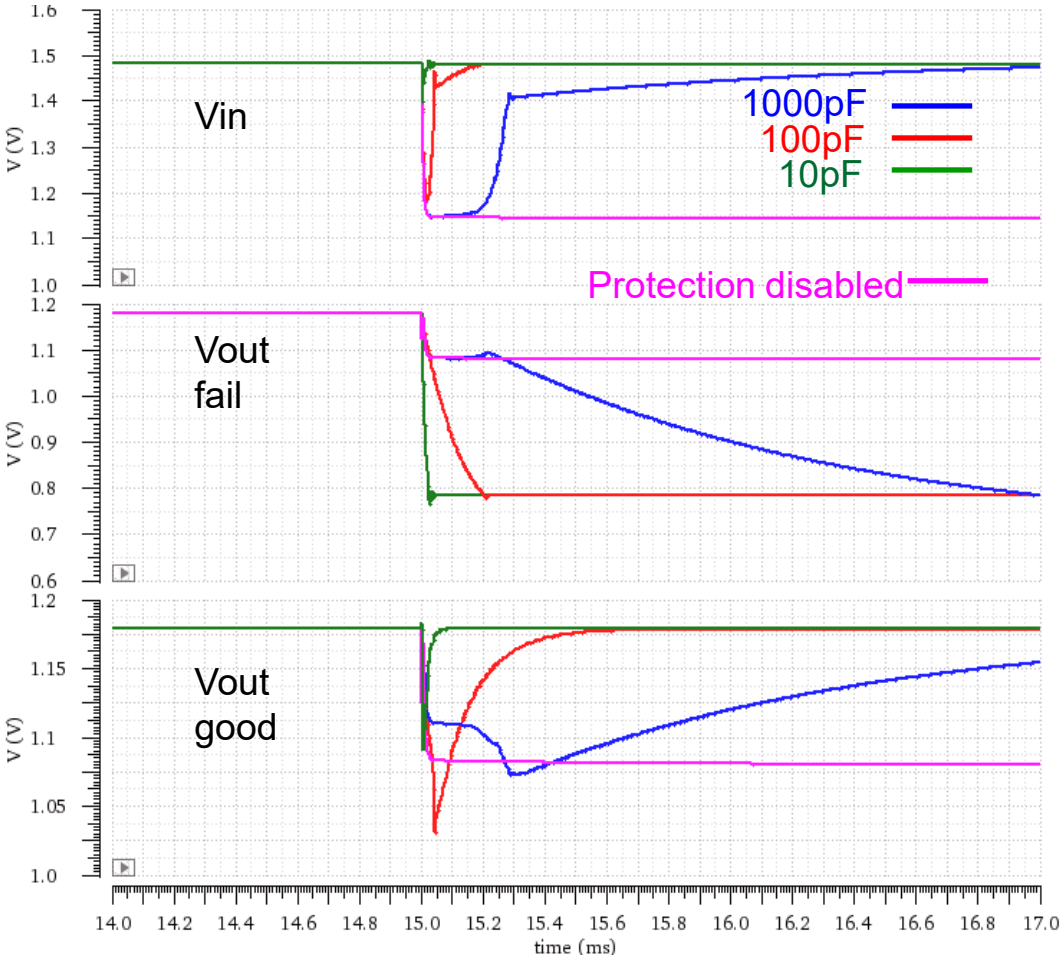
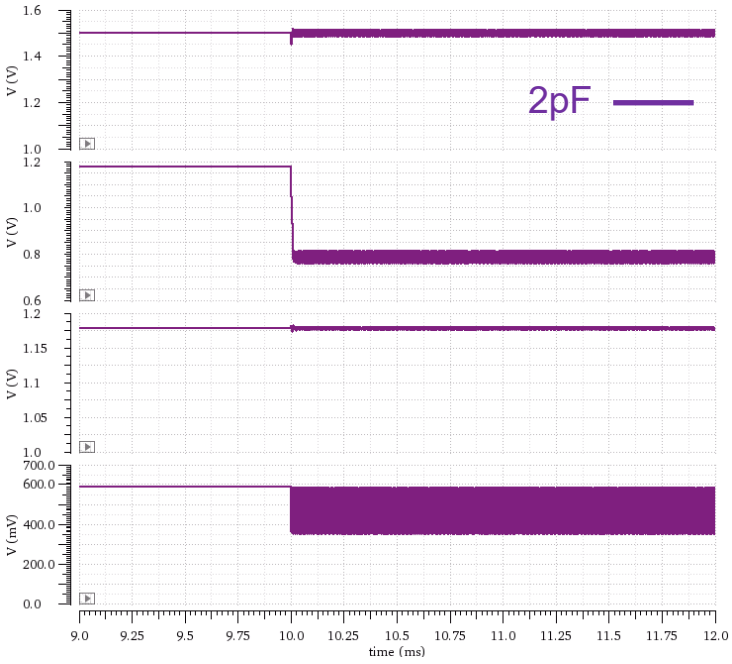


Design Challenges of the Undershunt Current Protection

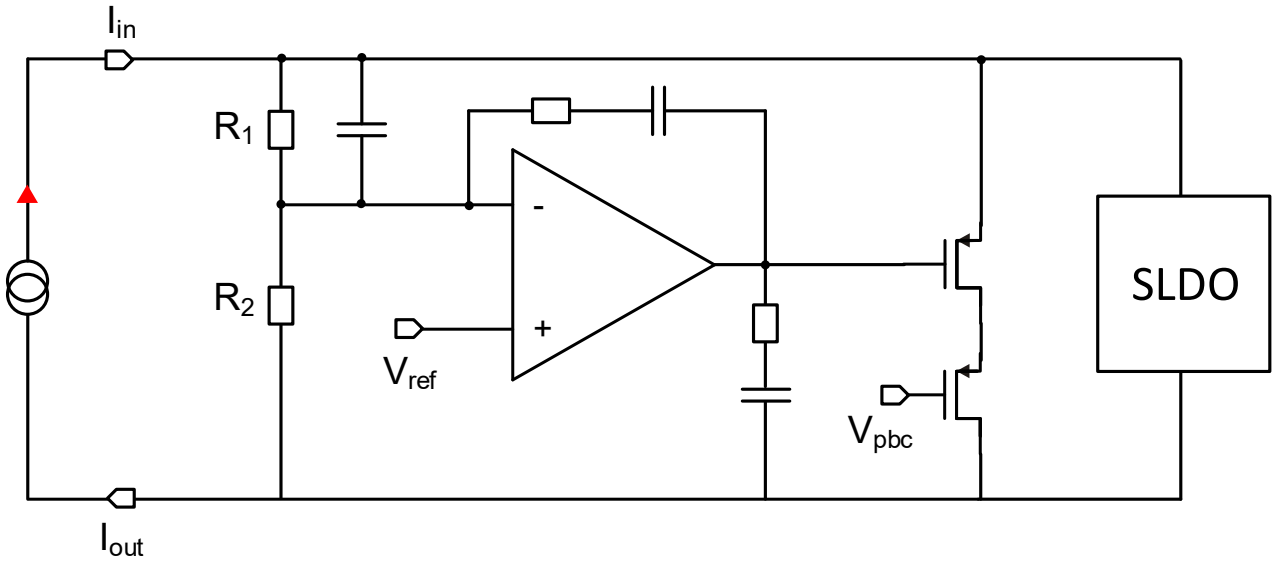
- **4 SLDO in parallel (2 chips) at room temperature:**
  - **Iin = 3.2A / Vofs = 1V (125k) / Vref = 0.6V (150k) / Rext = 625Ω / Rload = 1.6 Ω (low headroom ~6%)**
- Overload on 1 SLDO at time 15ms, from 2Ω to 1Ω (rt and ft of 10ns)



- Simulation for different Vref filter capacitor (Cstab) = **different protection speeds**
- Effective protection only for Cstab < 10pF -> possible oscillations



Protection Feature: Overvoltage Protection Voltage Clamp



- voltage clamp implemented as shunt regulator
  - operated in parallel to SLDO
- takes all excess current in case Vin =>2v
- limits the voltage to 2V
- can absorb up to 2A additional current per chip
- OVP threshold defined by untrimmed bandgap
  - voltage limit can vary +/- 5%