An Overview of On-Chip Particle Detectors for Self-Adaptive Integrated Circuits for Space

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IHP – Innovations for High Performance Microelectronics

innovations for high performance microelectronics

Leibniz Association

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Outline

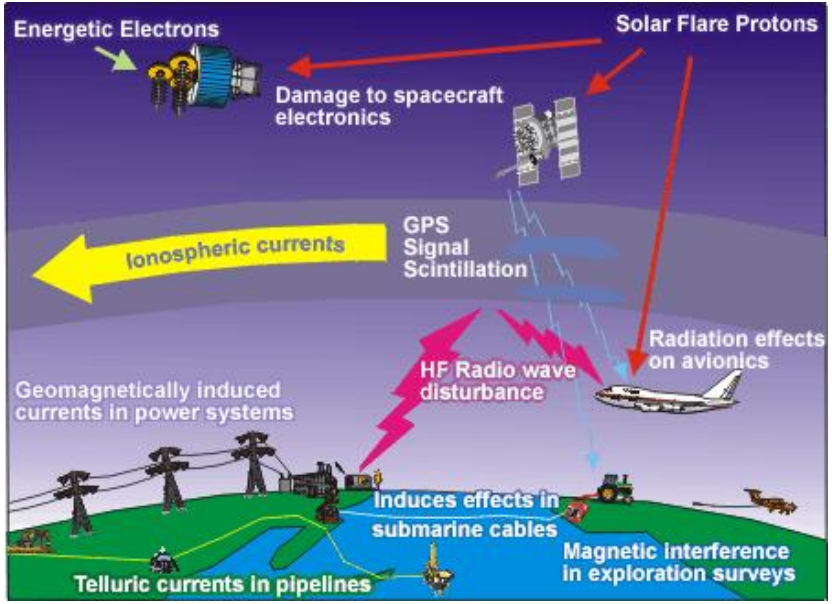
1. Background

Ionizing radiation in space

- Different types of radiation
- Variable radiation intensity
- May cause malfunction or physical damage in electronics in space and at ground

Radiation sources in space

- Radiation trapped in Earth's magnetic field (Van Allen belts)
- Galactic Cosmic Rays from deep space
- Solar Particle Events due to explosions on the Sun



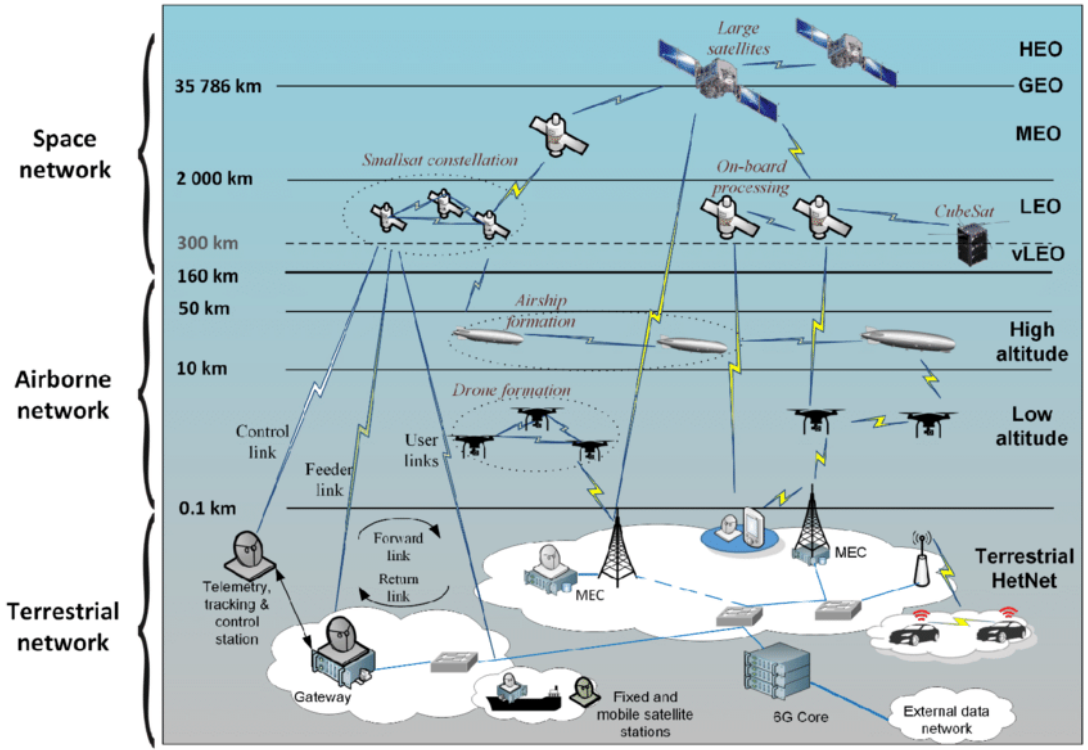
[Source: NASA]

1. Background

- **Satellites in orbit**
  - More than 9000 at the moment
  - Projections suggest over 40000 satellites by 2030

- **Satellite applications**
  - Weather forecasting
  - Earth observation
  - Navigation
  - TV/radio broadcasting
  - Wireless communications

3D wireless communication network

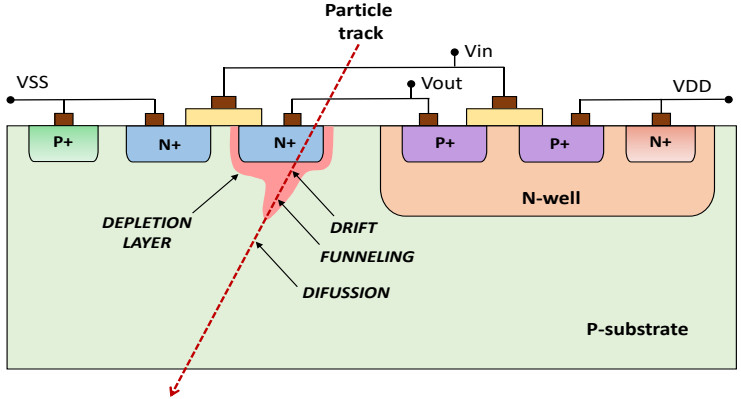


M. Hoyhtya et al., "Sustainable Satellite Communications in the 6G Era: A European View for Multi-Layer Systems and Space Safety," IEEE Access, 2022.

1. Background

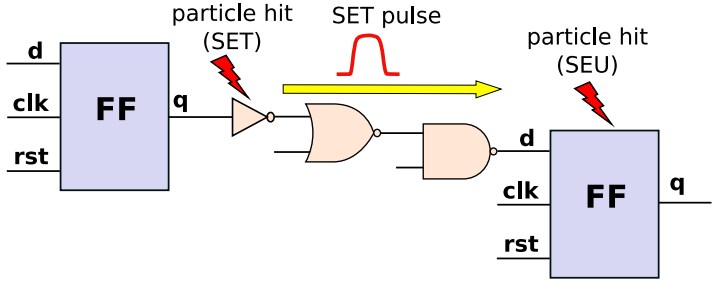
Soft errors

- Major reliability threat for integrated circuits (ICs) operated in space
- Manifested as unwanted bit flips in storage elements (flip-flops, latches, SRAM cells)
- Caused by a single high-energy particle (heavy ion, proton, neutron)



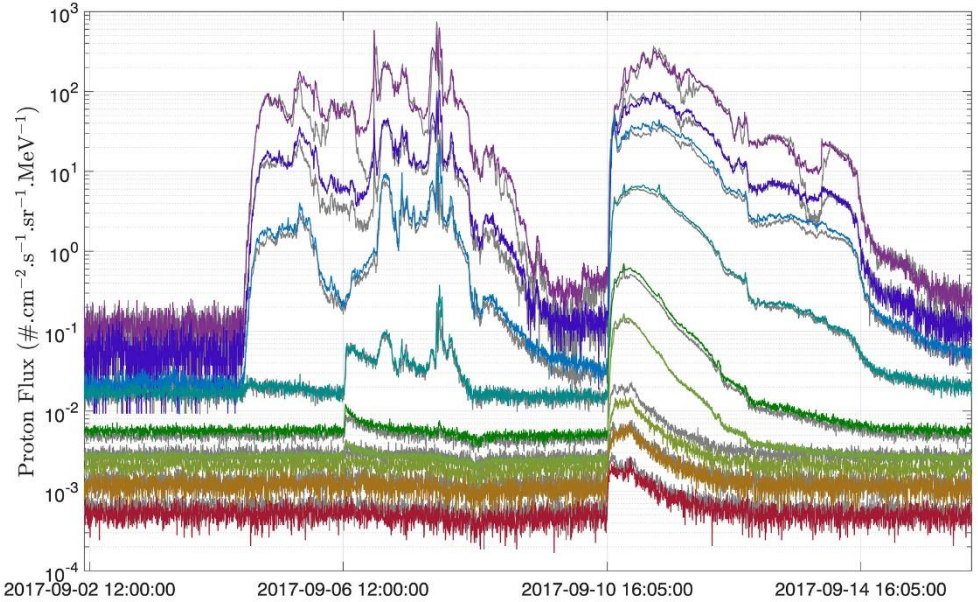
Two scenarios for soft error occurrence

- Particle strike in a storage element, resulting in a bit flip (**Single Event Upset – SEU**)
- Particle strike in a combinational gate, resulting in a voltage glitch (**Single Event Transient – SET**)



1. Background

- **Due to Solar Particle Events, the particle flux in space may increase several orders of magnitude during a period of several hours or days**



Particles with lower Linear Energy Transfer (LET) have higher flux

P. Jiggens et al., "In Situ Data and Effect Correlation During September 2017 SPE," Space Weather, 2018.

1. Background

- **Soft Error Rate (SER) –** *number of soft errors in a system, induced by SETs and SEUs in a given time interval*

$$SER = \sum_{i=1}^{N} SER_{NOMINAL}(i) \times SER_{DERATING}(i)$$

N = number of components in the system

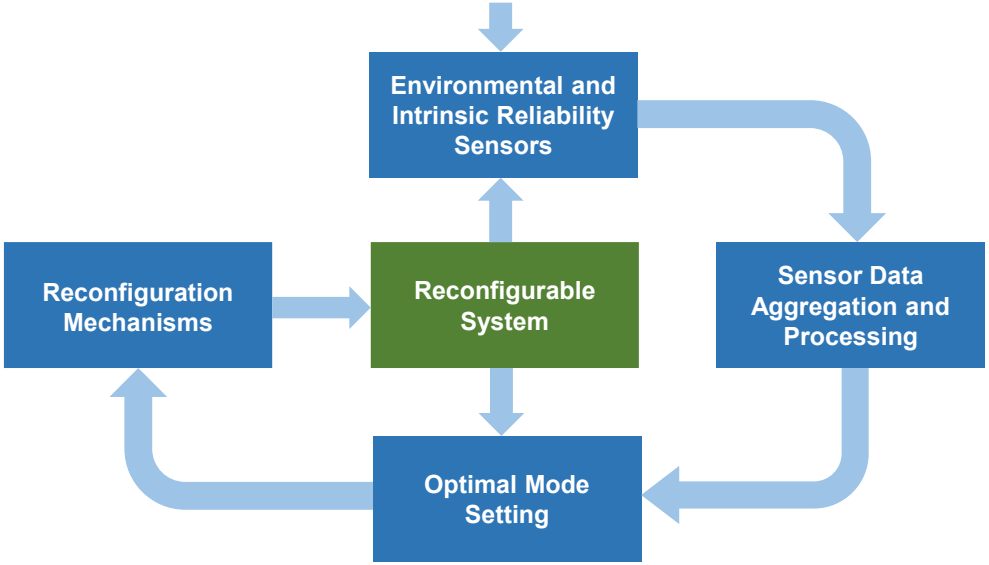
- **SER is strongly influenced by <u>particle flux and LET</u>**

$$SER_{NOMINAL} = k \cdot Flux \cdot Area \cdot e^{-Q_{CRIT}/Q_S}$$

$$SER_{DERATING} = Logical_{DER} \times \underbrace{Electrical_{DER} \times Timing_{DER}}_{\text{depend on LET}}$$

1. Background

- **Self-adaptive fault-tolerant ICs for space**
  - Fault tolerance can be activated only under critical radiation levels
  - Trade-off between performance, power consumption and radiation hardness
  - Measurement of radiation intensity (particle flux and LET) with on-chip sensors



2. State-of-the-Art Semiconductor Particle Detectors

- **Requirements for particle detectors for self-adaptive systems**
  - Ability to monitor particle flux and LET
  - Possibility of integration on the same chip with the target system
  - Low cost (low hardware and power overhead)
  - Low detection latency (fast response)
  - Immunity to false alarms, multiple errors and error accumulation

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- **Most common semiconductor particle detectors**
  - Diode-based detectors
  - SRAM-based detectors
  - Bulk built-in current detectors
  - Acoustic wave detectors
  - 3D NAND flash detectors

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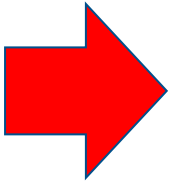
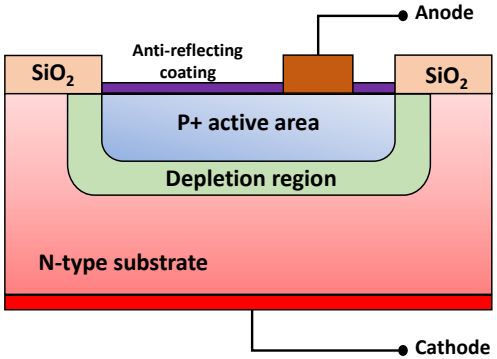


None of these detectors satisfies all requirements

2. State-of-the-Art Semiconductor Particle Detectors

Diode Detectors

- Reverse-biased *pn* junction as a particle sensor
- Pulsed-current or direct-current response
- Various implementations (e.g. strip detectors, pixel detectors)
- Commercial or custom-designed solutions

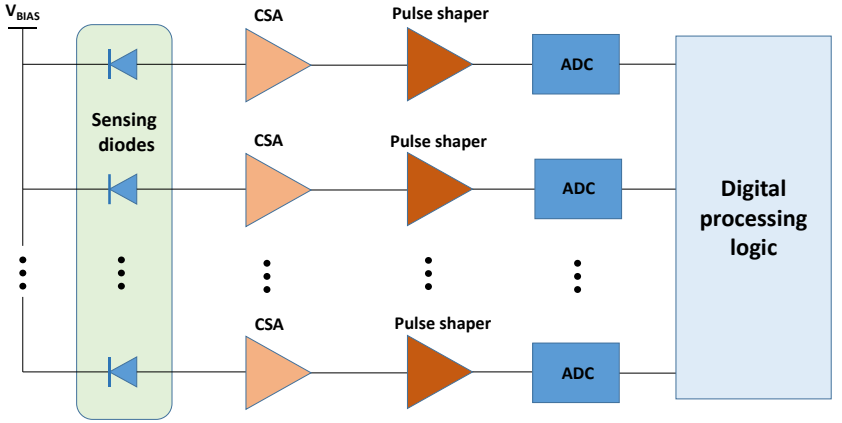


Pros:

- *Flux and LET detection*
- *High detection efficiency*

Cons:

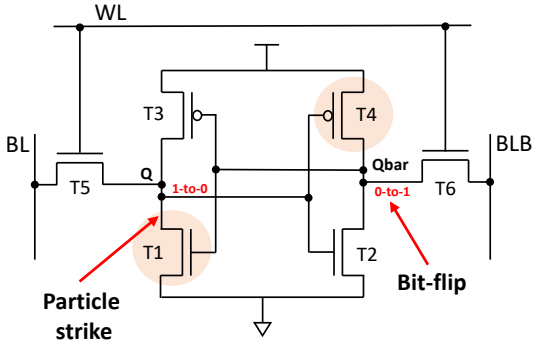
- *Mixed-signal readout*
- *Difficult on-chip integration*



2. State-of-the-Art Semiconductor Particle Detectors

SRAM Detectors

- Flux is measured in terms of SEU rate
- SEU detection with scrubbing and error detection and correction (EDAC) logic
- Stand-alone chip implementation
- Commercial SRAM chips can be used



6T CMOS SRAM cell is commonly used

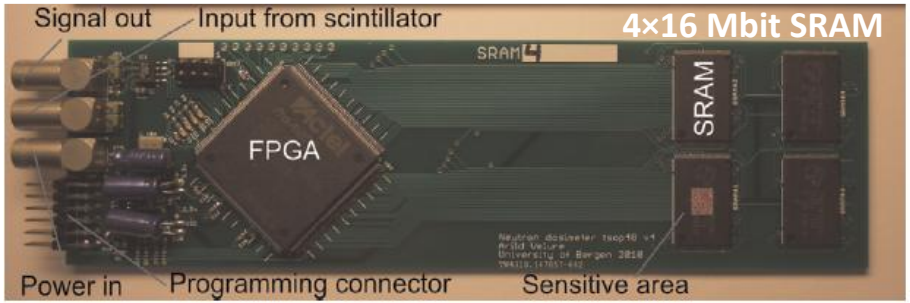
Two transistors in a 6T cell are sensitive to SEUs

Pros:

- *Fully digital processing*
- *Low cost implementation*

Cons:

- *Cannot detect particle LET*
- *Prone to multiple errors*
- *Large area overhead*
- *High latency*

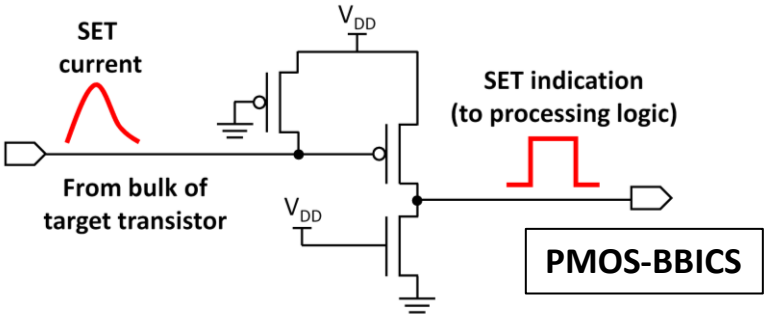


Ytre-Hauge et al., NIMPR A, 2015

2. State-of-the-Art Semiconductor Particle Detectors

Bulk Built-in Current Sensor (BBICS)

- Connected to transistors' bulk terminal
- Detection of particle-induced current pulse
- Detected current pulse is transformed into transient voltage pulse (alarm signal)



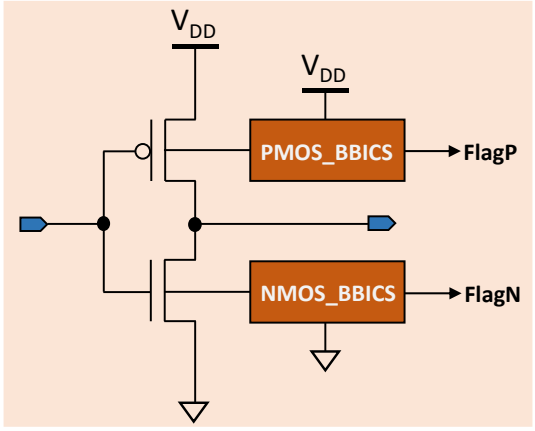
G. Wirth et al., Microelectronics Reliability, 2008

Pros:

- *Fully digital processing*
- *Detection of strike location*

Cons:

- *Sensitivity depends on the detector design*
- *Cannot detect particle LET*



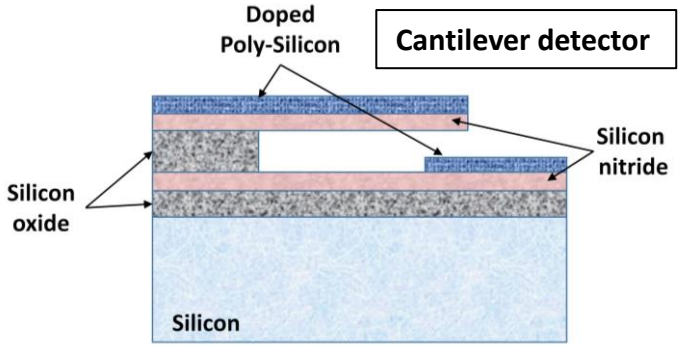
Two BBICS are required for each circuit, for PMOS bulk and NMOS bulk

Each BBICS can monitor 1000s of transistors

2. State-of-the-Art Semiconductor Particle Detectors

Acoustic Wave Detectors

- Detects acoustic waves generated in substrate by an incident energetic particle
- Cantilever-like structure is used as a detector
- Particle strike causes the change of capacitance of cantilever



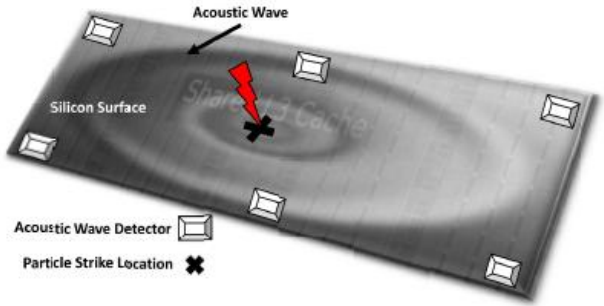
G. Upasani et al., IEEE Trans. on Computers, 2016

Pros:

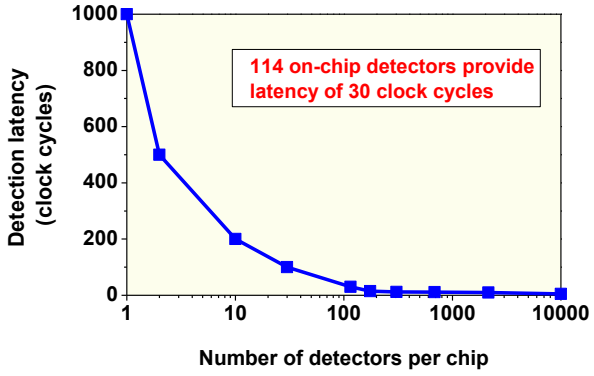
- *Detection of strike location*
- *Several on-chip sensors are sufficient*

Cons:

- *Mixed-signal readout*
- *Cannot detect particle LET*



Multiple detectors on the chip to detect the strike locations



2. State-of-the-Art Semiconductor Particle Detectors

3D NAND Flash Detectors

- Based on floating gate transistors for data storage
- Ionizing radiation causes the change of transistors' threshold voltage
- Commercially available for data storage

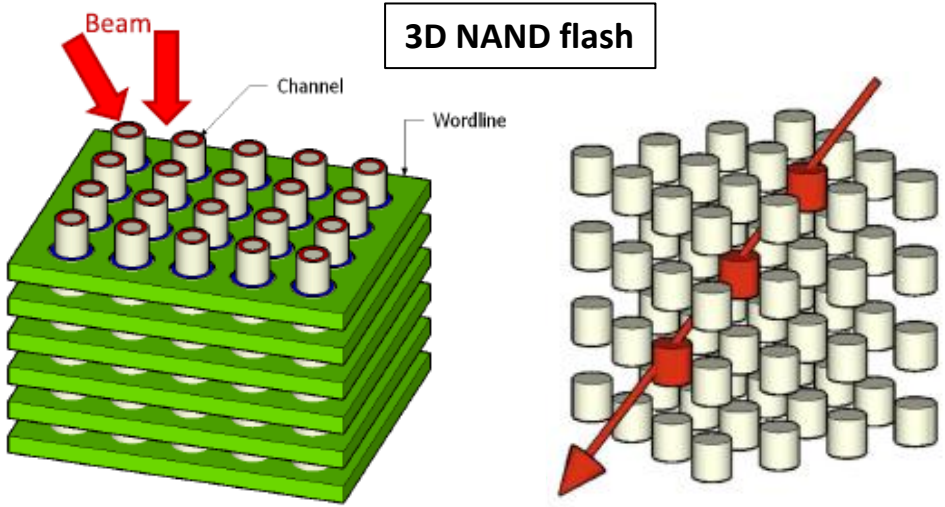
Pros:

- *Detection of flux, LET and angle of incidence*
- *Low sensitivity to multi-bit errors*

Cons:

- *Difficult on-chip integration*
- *Complex processing logic*

3D NAND flash



M. Bagatin et al., IEEE TNS, 2020

3. Particle Detectors Developed at IHP

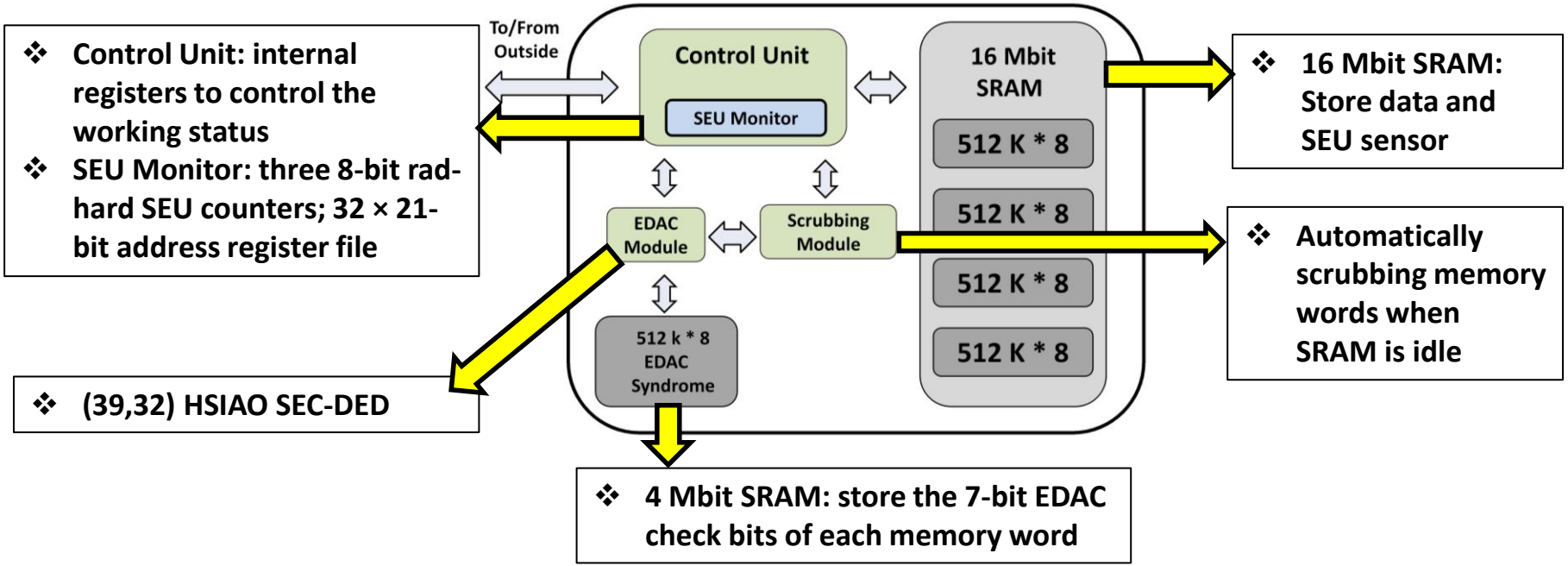
- **Three solutions for on-chip particle detection**

Sensor	Main feature
Embedded SRAM	On-chip SRAM is used as a sensor
Pulse stretching inverter chain	New sensing approach
Pulse stretching BBICS	Extension of existing BBICS

- **All proposed detectors are fully digital**
  - No need for external voltage bias
  - No need for ADC and operational amplifiers
  - Can be integrated in any chip

3.1 Embedded SRAM

- Existing memory on a chip is used for data storage and as a particle detector
- Use of standard error detection and correction methods



J. Chen et al., Electronic Circuit with Integrated SEU Monitor, European Patent Application EP 3 748 637 A1, Bulletin 2020/50.

3.1 Embedded SRAM

- **Key advantage – negligible area and power overhead**

Synthesis results for 20 Mbit SRAM	
Technology (*µm*)	0.13
Supply Voltage (*V*)	1.2
Frequency (*MHz*)	50
Total area (mm^2)	14
Total power dissipation (*mW*)	384
'Non-SRAM' part* area (mm^2)	0.0957
'Non-SRAM' part power (*mW*)	0.211

Area and power dissipation comparison between 20 Mbit SRAM and 'Non-SRAM' part

	20 Mbit SRAM	Non-SRAM part
Area (mm^2)	13.9 (99.3 %)	0.0957 (0.7%)
Power consumption (*mW*)	383 (99.9%)	0.211 (0.1%)

Area and power dissipation comparison in the 'Non-SRAM' part

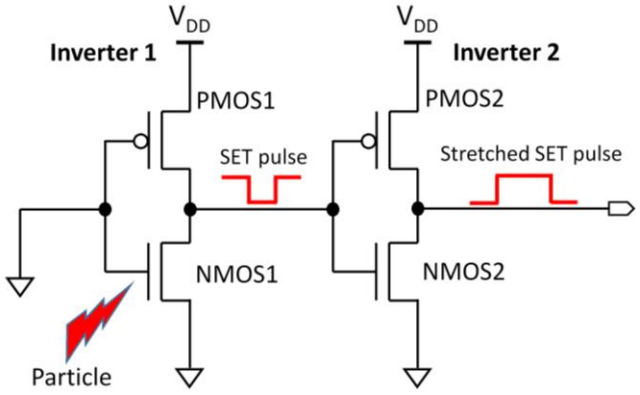
	SEU Monitor	EDAC + Scrubbing + Control Unit
Area (um^2)	95739 (84 %)	18706 (16%)
Power consumption (*mW*)	0.211 (80%)	0.054 (20%)

*: 'Non-SRAM' part contains **control unit**, **SEU monitor**, **EDAC** and **scrubbing module**

3.2 Pulse Stretching (PS) Inverter Chain

- **Two skew-sized CMOS inverters act as a sensor**
  - Off-state transistors are sensitive to particles
  - On-state transistors are restoring elements
  - Pulse stretching allows to detect low-LET particles
- **Basic operating principles**
  - SET count rate is proportional to flux
  - SET pulse width variation is proportional to LET variation
- **Transistor sizing guidelines**
  - Large off-state transistors (larger sensitive area)
  - Small on-state transistors (reduced restoring current)

Pulse Stretching Cell (PSC)



$$W_{NMOS1} > W_{PMOS1}$$

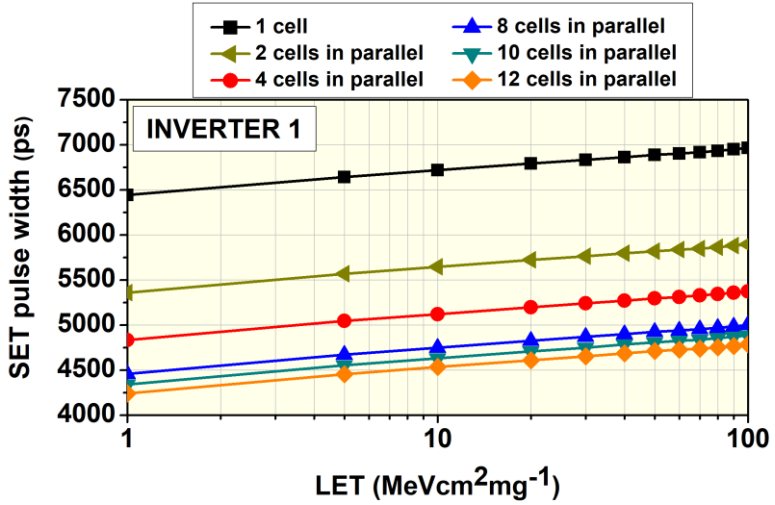
$$W_{PMOS2} > W_{NMOS2}$$

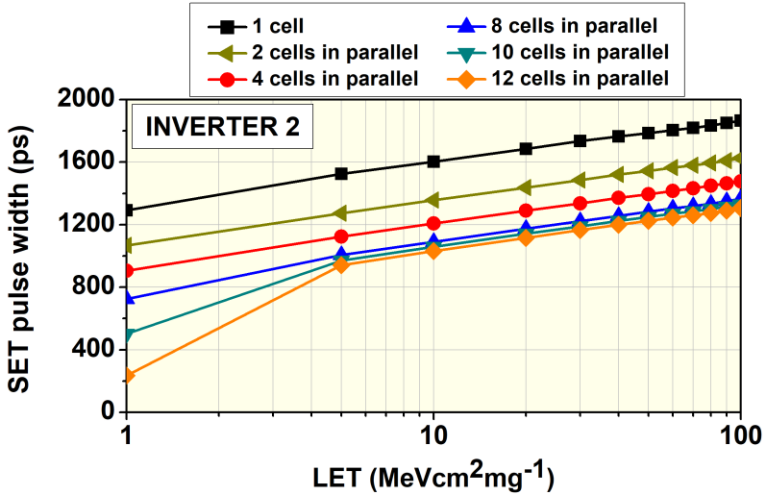
$$W_{NMOS1} = W_{PMOS2}$$

$$W_{PMOS1} = W_{NMOS2}$$

3.2 Pulse Stretching (PS) Inverter Chain

- **Simulated SET pulse width dependence on LET (for parallel PSC configuration)**
  - Increasing the number of PSCs in parallel decreases the SET pulse width
  - Up to 12 PSC in parallel ensure detectability of SET pulses
  - SET pulse width increases by 550 ps for LET from 1 to 100 MeVcm^{2}mg^{-1}



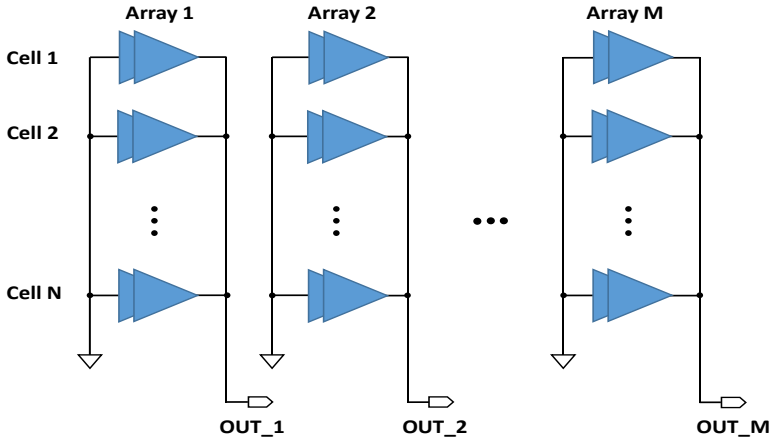


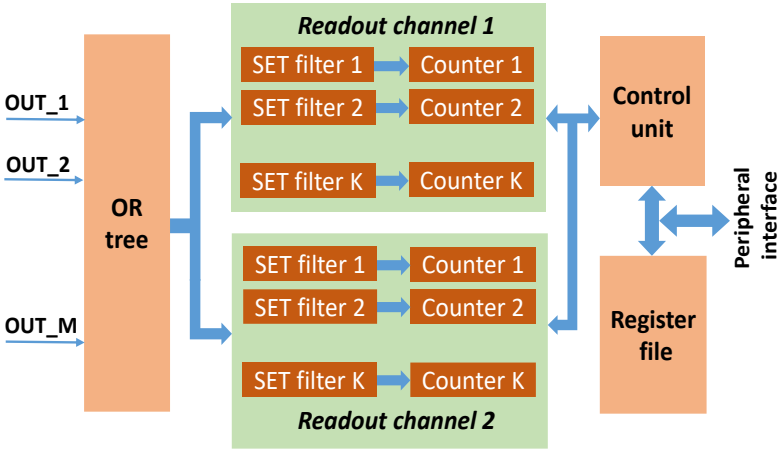
M. Andjelkovic et al., Monitoring of Particle Count Rate and LET Variations with Pulse Stretching Inverters, IEEE TNS, 2021.

3.2 Pulse Stretching (PS) Inverter Chain

Digital readout circuit

- Multiple parallel PSC arrays are connected to an OR-tree
- Detected SETs are filtered and grouped in several pulse width ranges
- Counters store the number of detected SETs in each width range
- Each SET pulse width range corresponds to a unique LET range

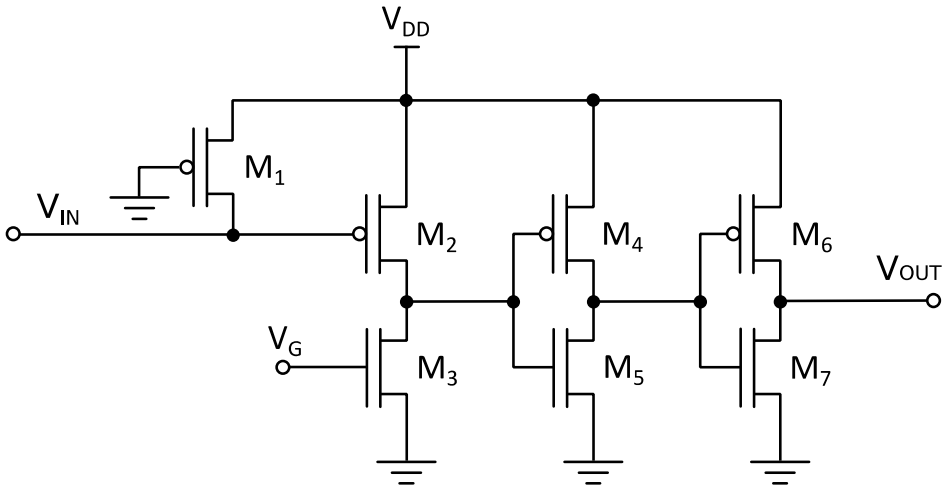




3.3 Pulse Stretching BBICS (PS-BBICS)

Modification of standard BBICS

- Two-inverter pulse stretcher is added to extend short SETs
- SET pulse width can be measured, enabling to estimate particle LET

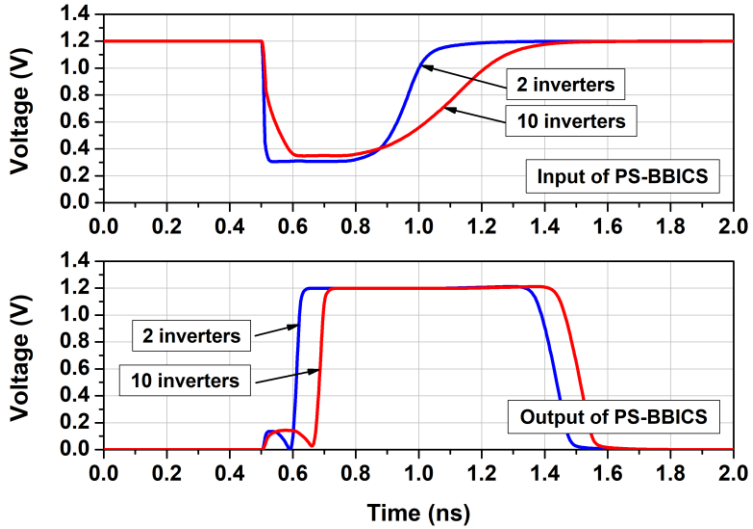


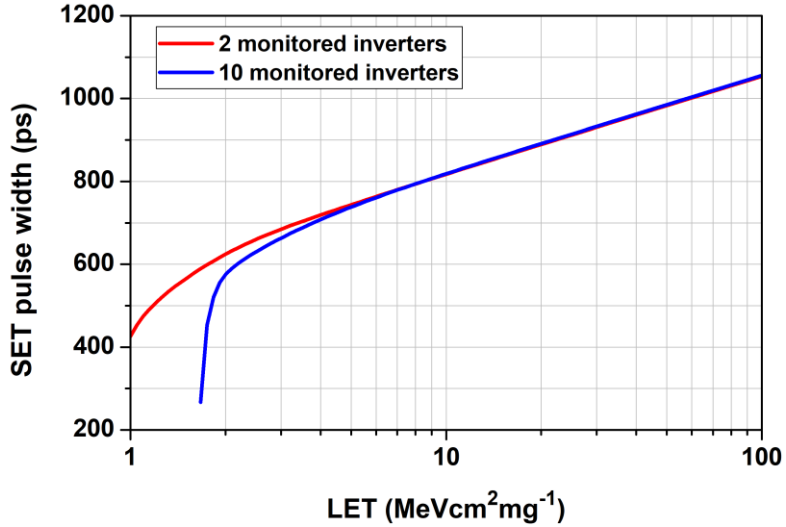
$$W_{M_4} = W_{M_7}$$
$$W_{M_5} = W_{M_6}$$
$$W_{M_5} > W_{M_4}$$
$$W_{M_6} > W_{M_7}$$

M. Andjelkovic et al., PS-BBICS: Pulse Stretching Bulk Built-in Current Sensor for On-chip Measurement of Single Event Transients, Microelectronics Reliability, 2023.

3.3 Pulse Stretching BBICS (PS-BBICS)

- **SET pulse width as a function of LET, for 2 and 10 load inverters**
  - For LET > 4 MeVcm^{2}mg^{-1}, the SET pulse width is independent of the number of monitored inverters



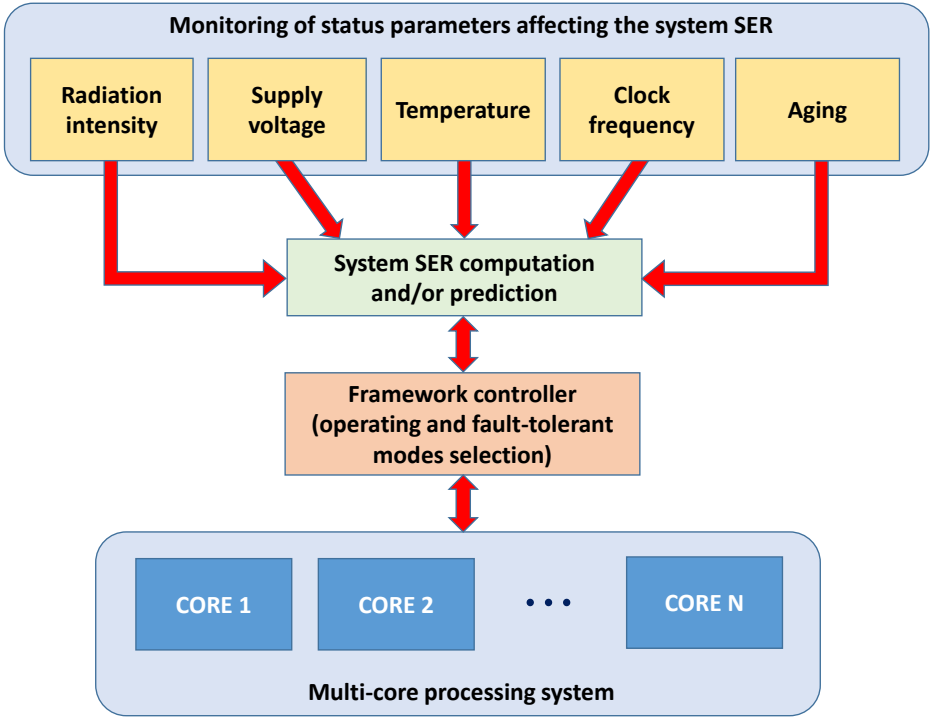


4. Comparison of Particle Detectors

Type of detector	Readout method	Hardware overhead	Detection latency	Prob. of false alarms	Multiple errors	LET detection
BBICS	Digital	< 30 %	< 10 clock cycles	Medium	No	No
Acoustic wave detector	Mixed-mode	< 20 %	< 100 clock cycles	Medium	No	No
Diode detector	Mixed-mode	> 100 %	100s clock cycles	Low	No	Yes
Stand-alone SRAM	Digital	> 100 %	> 1000 clock cycles	Low	Yes	No
3D NAND flash	Mixed-mode	> 50 %	100s clock cycles	Low	No	Yes
Embedded SRAM	Digital	< 5 %	> 1000 clock cycles	Low	Yes	No
PS inverter chain	Digital	< 20 %	< 10 clock cycles	Low	No	Yes
PS-BBICS	Digital	< 20 %	< 10 clock cycles	Low	No	Yes

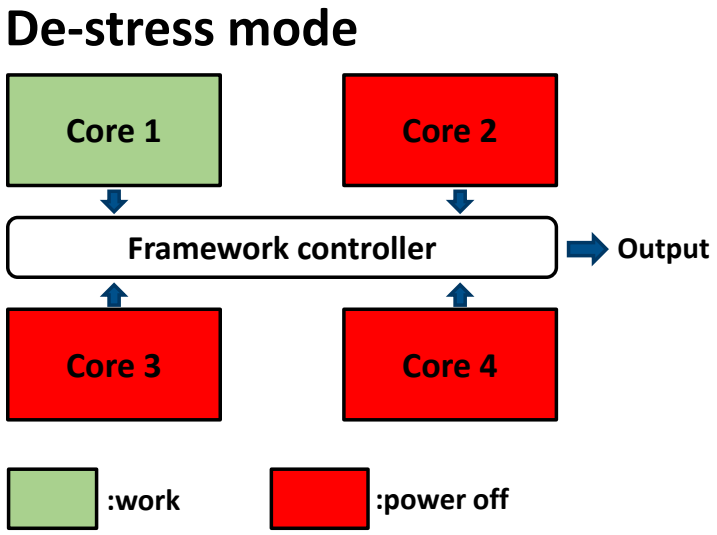
5. Use Case: Self-Adaptive Quad-Core Processing System

- **Multiprocessing (multi-core) system**
  - Inherent hardware redundancy
  - Operating modes are selected by reconfiguring the cores
- **On-chip sensors enable real-time SER monitoring**
- **Three operating modes:**
  - De-stress (low-power) mode
  - High performance mode
  - Fault-tolerant (rad-hard) mode



5. Use Case: Self-Adaptive Quad-Core Processing System

- **Operating modes in a quad-core processing system**
  - **De-stress (low power) mode**
    - One or more cores operate, while others are switched off
  - High performance mode
    - All cores operate in parallel, i.e. execute different tasks
  - Core-level fault tolerant mode
    - *Dual Modular Redundancy (DMR)*
    - *Triple Modular Redundancy (TMR)*
    - *Quad Modular Redundancy (QMR)*



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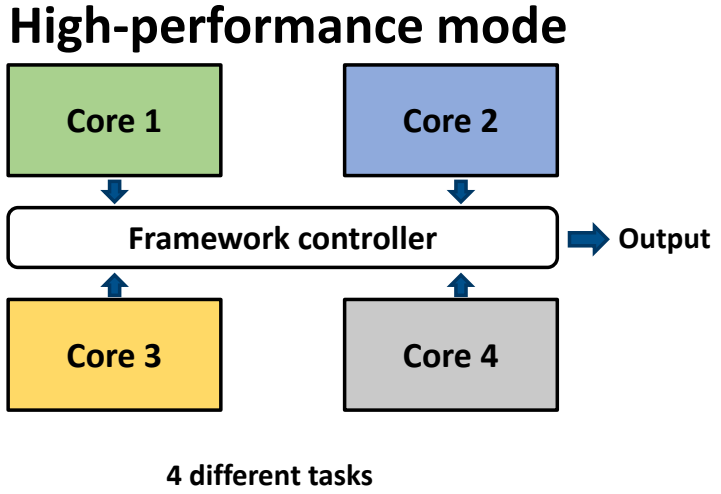

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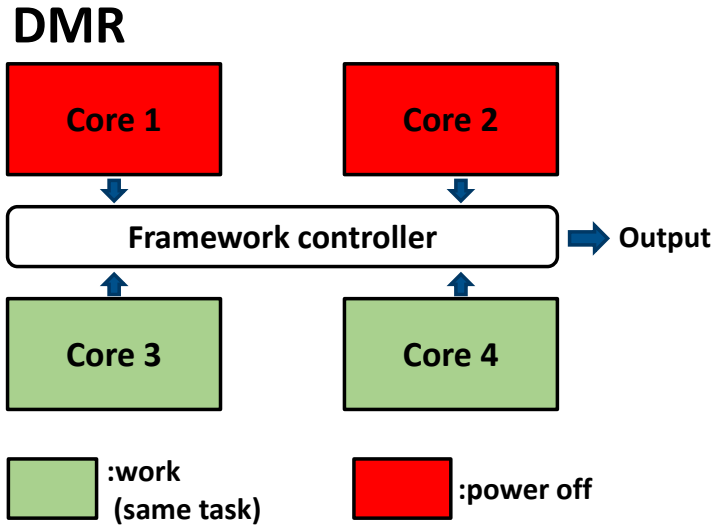

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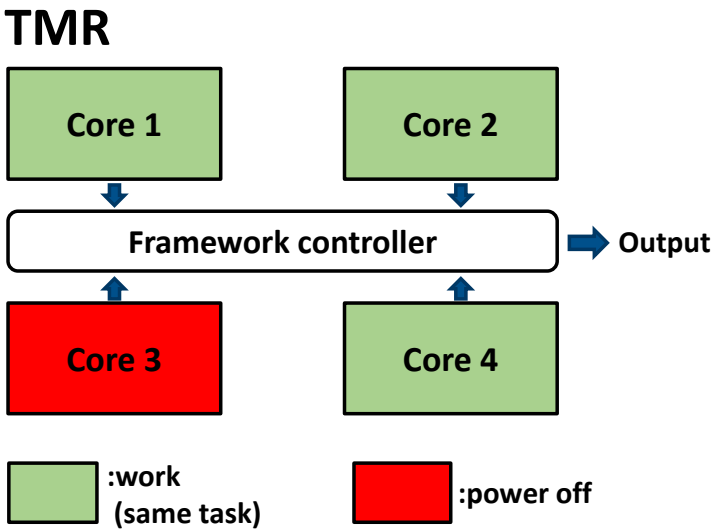

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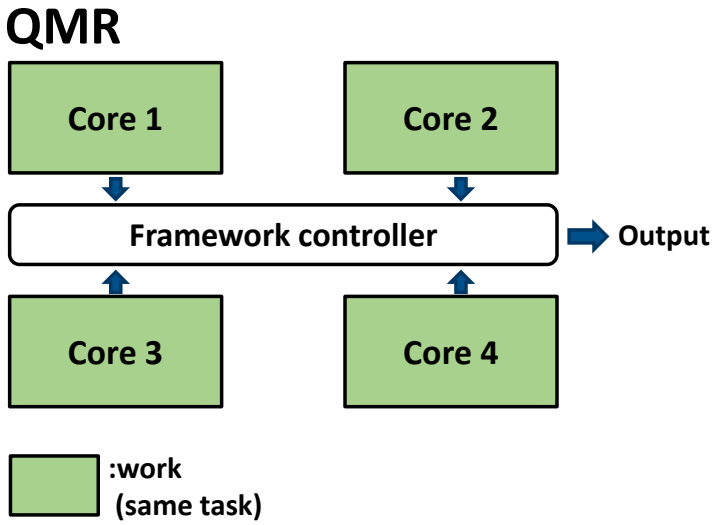
    - *Triple Modular Redundancy (TMR)*
    - *Quadruple Modular Redundancy (QMR)*

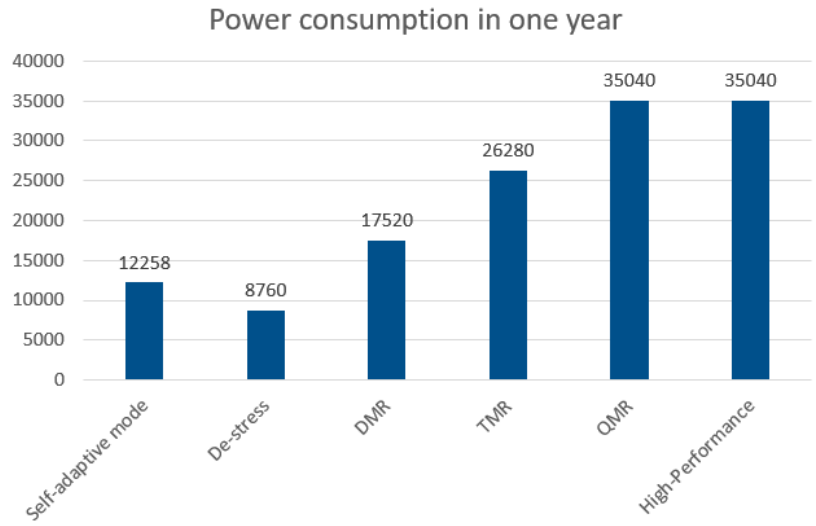


5. Use Case: Self-Adaptive Quad-Core Processing System

- **Case study: Self-adaptive quad-core system**
  - Self-adaptive mode switching: configuring the least amount of core level redundancy depending on the current SERs measured by detector
  - Power consumption in a year is lower than individual DMR, TMR and QMR configurations

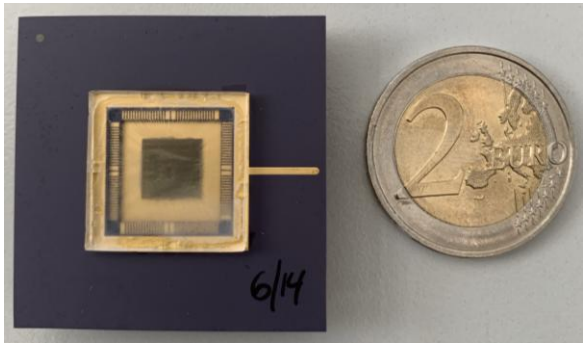
SER (*upsets/(bit*day)*)	Operating Mode	Duration Time/Year* (hours)
$< 10^{-8}$	High-Performance De-Stress	5460
$10^{-8} \sim 10^{-7}$	DMR	3120
$10^{-7} \sim 10^{-6}$	TMR	162
$> 10^{-6}$	QMR	18

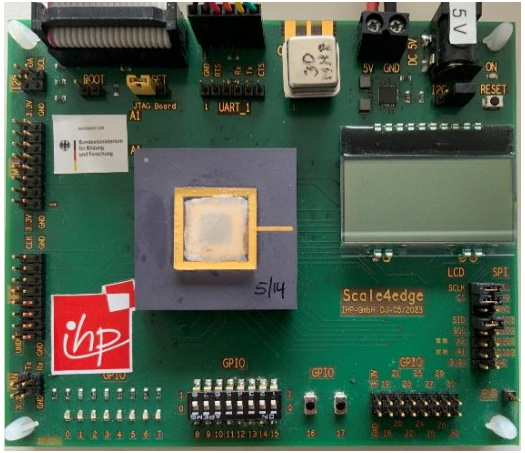
*: merge of SERs under different solar conditions into a one-year average

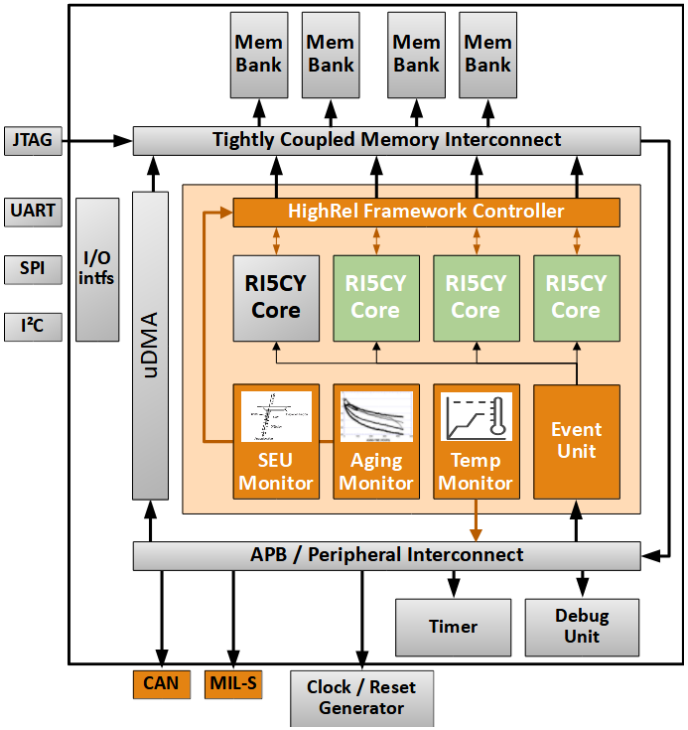


5. Use Case: Self-Adaptive Quad-Core Processing System

- **TETRISC SoC**
  - Fabricated in IHP 130 nm technology
  - Extended PULPissimo platform (4 RISCY cores)
  - On-chip sensors: temperature, aging, soft error, SRAM particle detector







M. Ulbricht et al., The TETRISC SoC – A Resilient Quad-Core System based on the ResiliCell Approach, Microelectronics Reliability, 2023.

6. Summary

- Self-adaptive multiprocessing provides trade-off between performance, power consumption and fault-tolerance
- Particle detection is a key requirement for self-adaptive fault-tolerance in space
- Existing particle detectors cannot provide optimal performance for on-chip particle detection
- Three fully-digital particle detectors are proposed
- A self-adaptive quad-core processor with embedded SRAM as a particle detector has been developed

Thank you for your attention!

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