Low-cost AI-based Error Prediction

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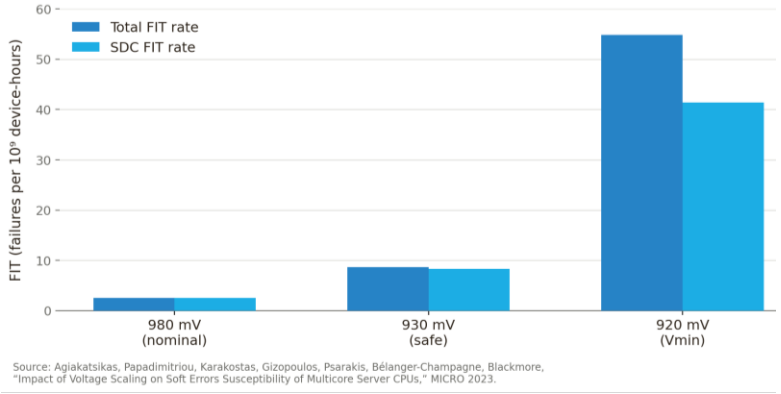
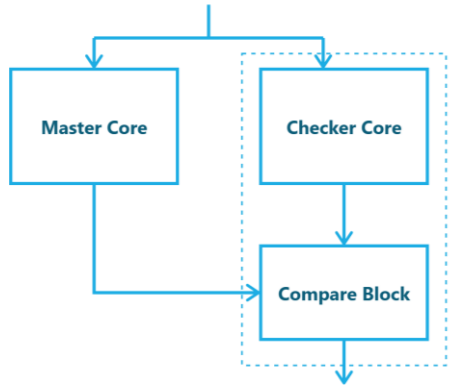
Motivation

- Timing errors are rising under process variation and voltage over-scaling (VOS) in nanometer nodes



- Classic approaches (Triple Module Redundancy, Dual-core Lockstep):
  - act only after errors occur
  - cost ≥2× area / ~100% overhead.



Proposed approach

- Alternative solution is error prediction, enabling actions before errors occur and minimizing potential impact

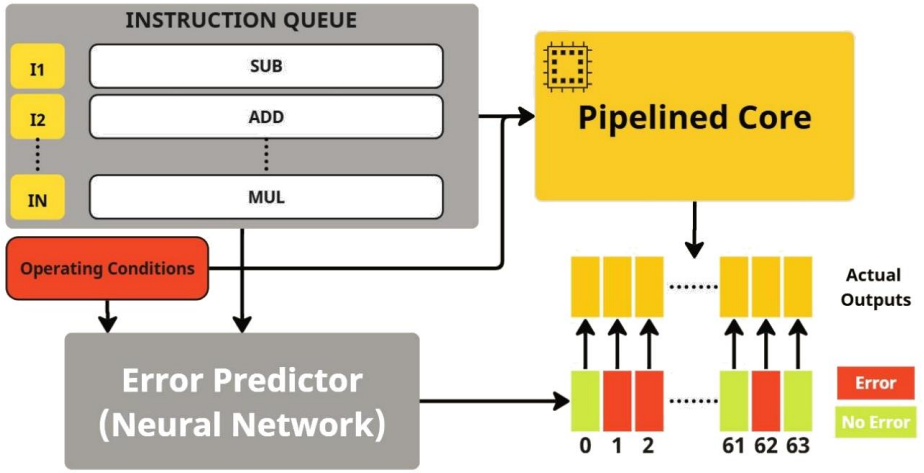
- Existing AI-based predictors are only starting to be explored and come at a high cost

PhD Focus: Implementation of low-cost AI-based error prediction and error mitigation mechanisms on hardware

Recent Work - Bit Error Prediction Model

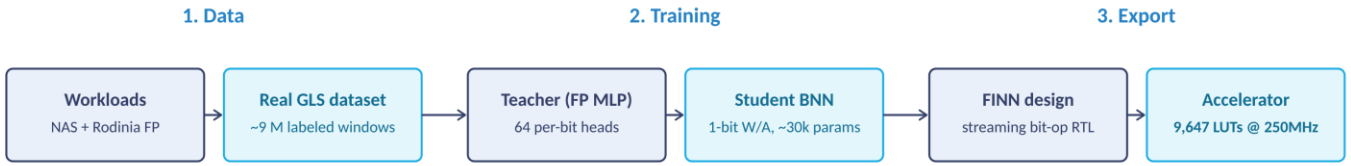
- *ePredBitNet*: a compact ML-based error predictor, enabling:
  - Selective correction that protects only the vulnerable bits
  - Field-aware mitigation for exponent bits
  - Workload-aware bit error mitigation

- Target: OpenRISC mor1kx “Marocchino” FPU
  - FPU32/FPU64



ePredBitNet

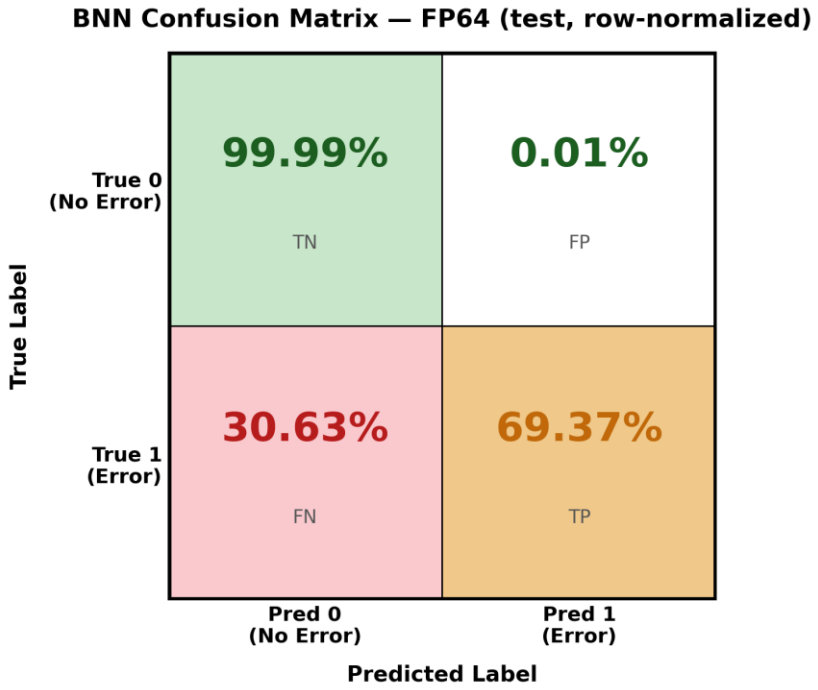
- MLP D→64→64→64, distilled to Binary NN



- Trained using dataset of ~9M instruction windows
  - Extracted from NAS and Rodinia workloads
  - Split 60/20/20

- Implemented in AMD FPGA at 250 MHz

Results



- Near-zero false positives (0.01%)
- Bit-level accuracy 99.76-99.81%
- Hardware implementation
  - Adds ~28% LUTs to the Core
  - Uses 70% less LUTs vs DCLS & 85% less LUTs vs TMR

Ongoing work – Next Steps

- Develop new instruction-aware error datasets for RISC-V
- Explore various AI Architectures for accurate error prediction
- Explore Methods (Pruning, Quantization) for implementing low-cost error prediction
- Combine error prediction models in RISC-V CPUs

Thank you!

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