Gate-Level Techniques for Mitigation of Single Event Transients (SETs) in Combinational Circuits

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Outline

1. **Motivation**
2. **State-of-the-Art Solutions for SET Mitigation**
3. **Overview of Gate-Level SET Mitigation Techniques**
4. **Comparison of Gate-Level SET Mitigation Techniques**
5. **Combined Use of Multiple Gate-Level SET Mitigation Techniques**
6. **Conclusion**

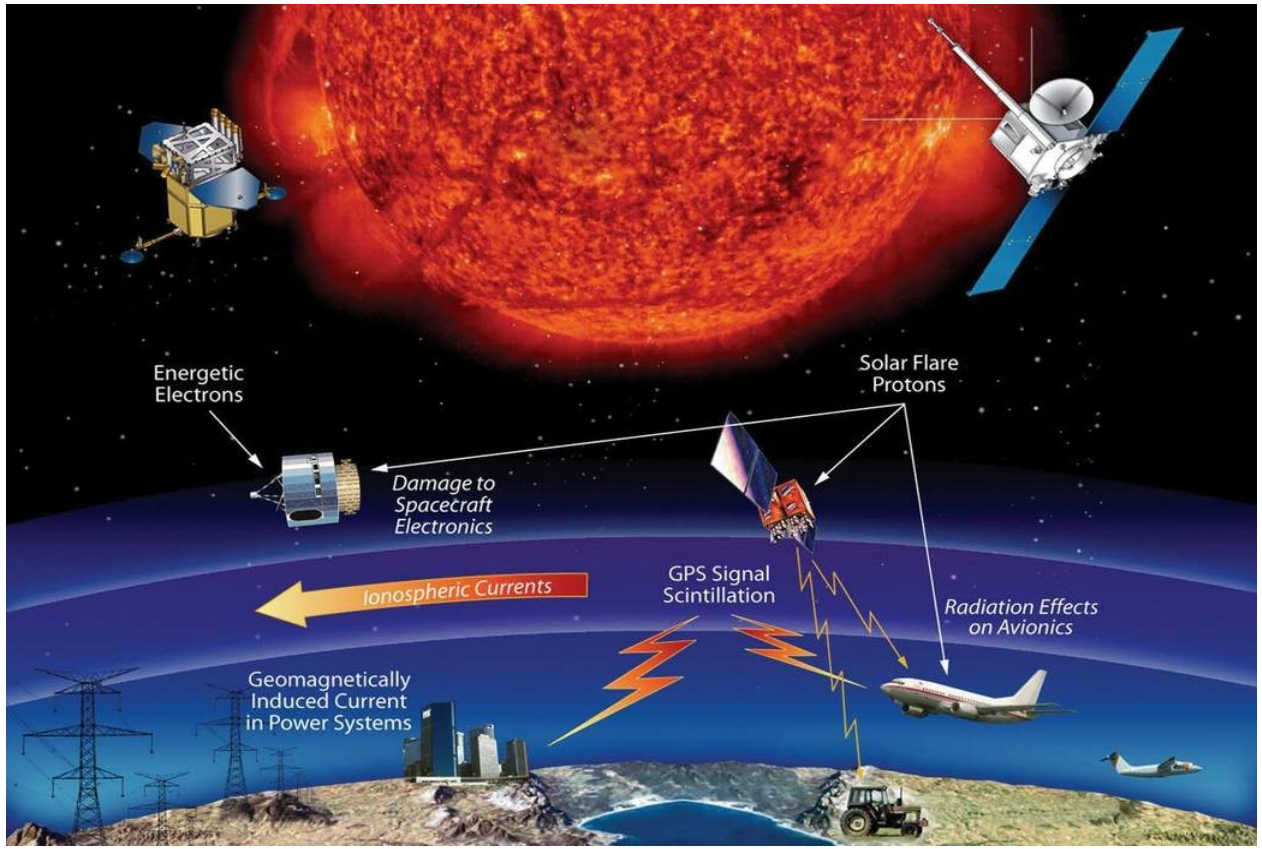
1. Motivation

Ionizing radiation in space

- Different types of radiation (gamma, x-rays, energetic particles)
- May cause malfunction or physical damage in electronics in space and at ground

Radiation sources in space

- Radiation trapped in Earth's magnetic field (Van Allen belts)
- Galactic Cosmic Rays from deep space
- Solar Particle Events due to explosions on the Sun



[Source: NASA]

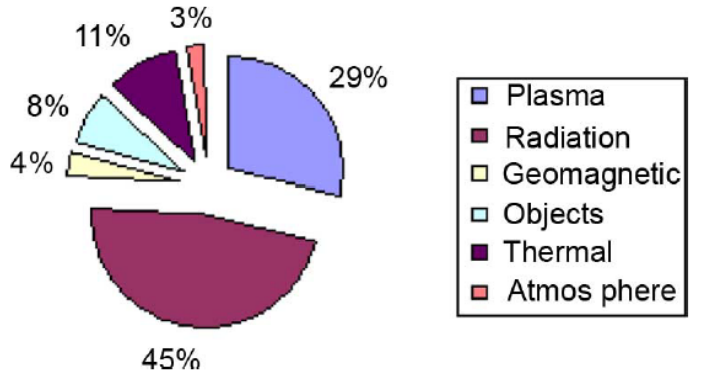
1. Motivation

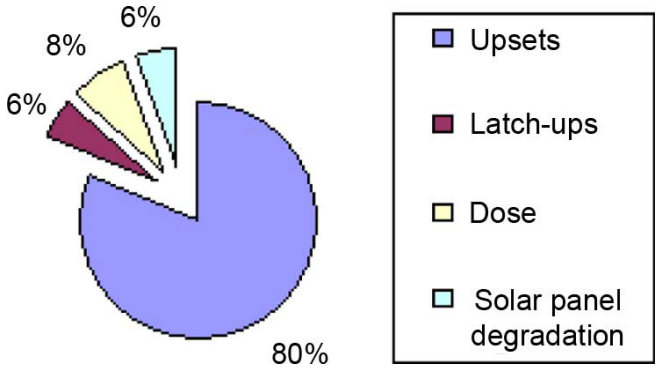
Soft errors

- Manifested as bit-flips, resulting in data loss and system malfunction
- Caused by energetic particles such as heavy ions, neutrons, protons
- Major cause of faults in ICs used in space missions

Over 40 % of all anomalies in space missions caused by environmental factors have been due to ionizing radiation

Over 80 % of radiation-induced anomalies in space missions have been caused by soft errors



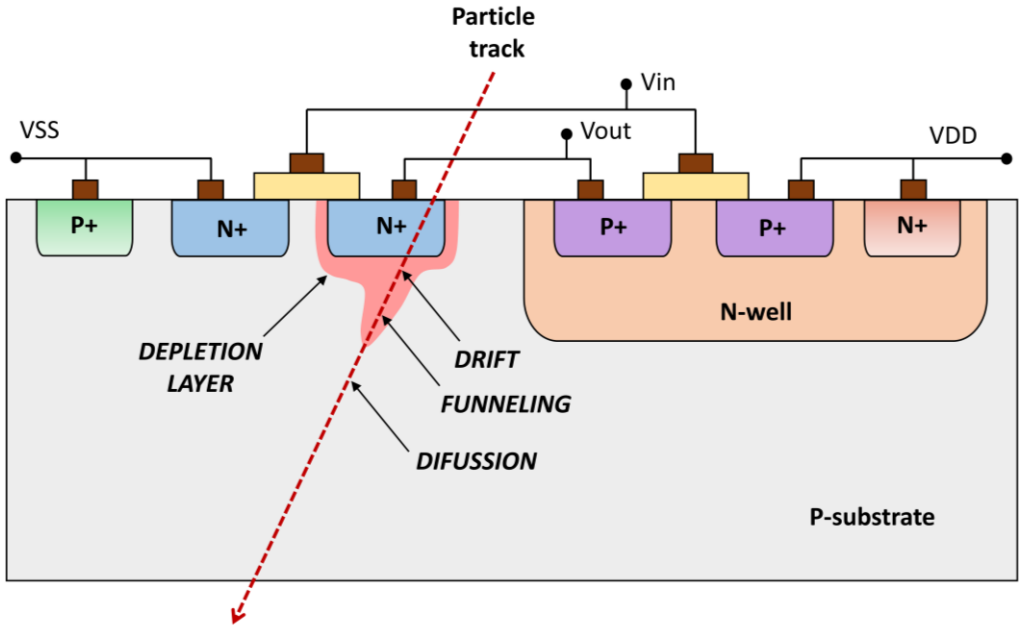


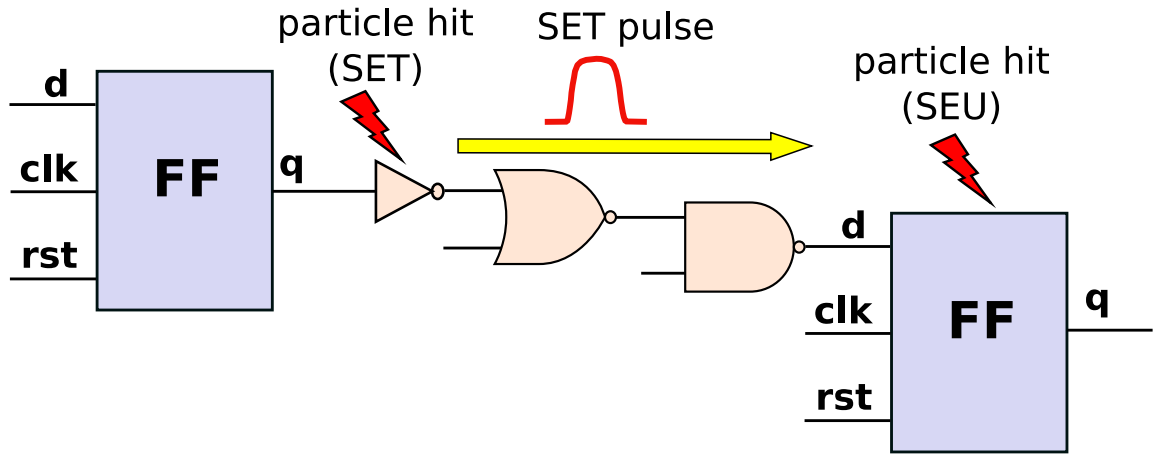
Source: **R. Ecoffet, Overview of In-Orbit Radiation Induced Spacecraft Anomalies, IEEE Transactions on Nuclear Science, 2013.**

1. Motivation

How soft errors occur?

- Particle hits a storage element, resulting in a bit-flip (**Single Event Upset - SEU**)
- Particle hits a combinational element, resulting in a voltage glitch (**Single Event Transient - SET**), which may propagate to one or more storage elements and cause one or more bit-flips

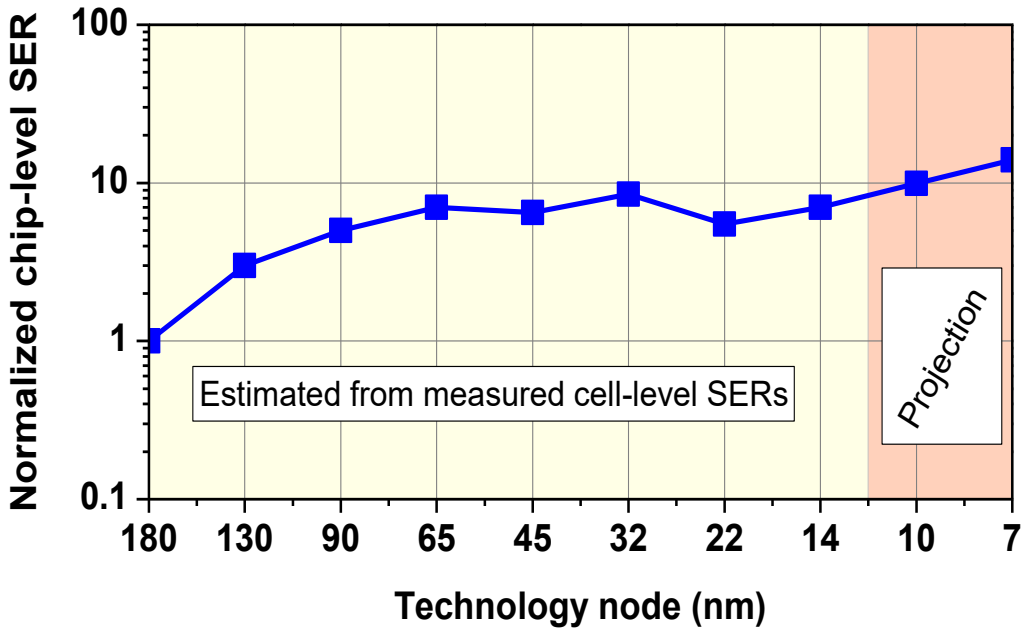




1. Motivation

Technology scaling effects

- Soft Error Rate (SER) of ICs increases with technology scaling due to increase of IC complexity
- With technology scaling, soft errors have become relevant also for terrestrial electronics



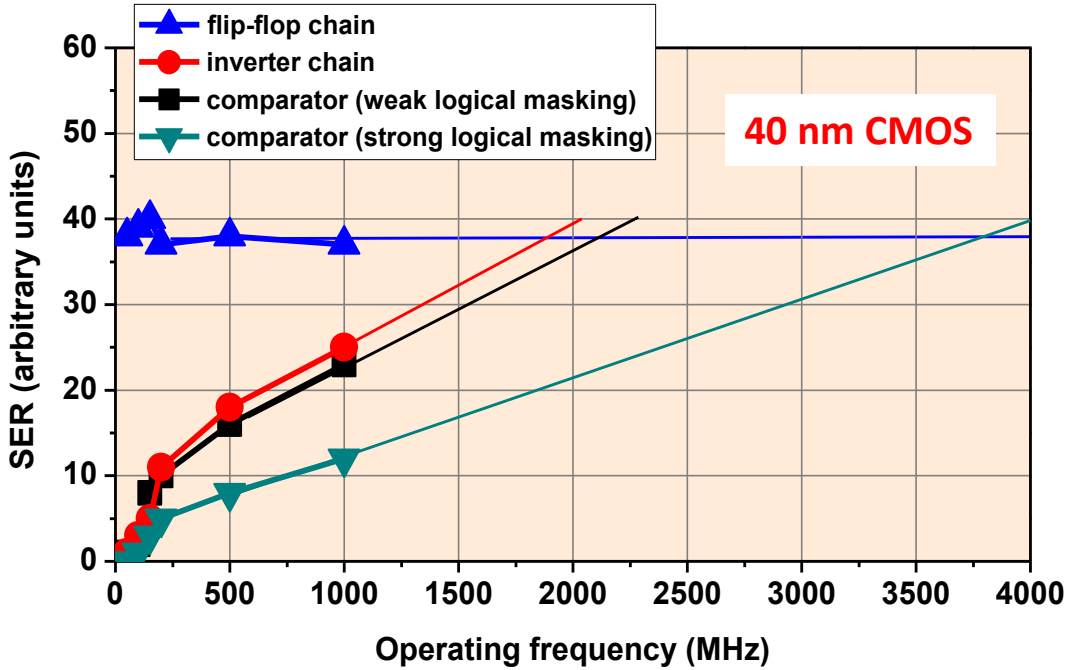
Source: **K. Ljilja, "Environment and Devices, SER – Modeling Neutrons and Heavy Ion SER, From Planar CMOS to FINFET," Short Course, NSREC, 2016.**

1. Motivation

Contribution of SETs to the total SER of an IC increases with technology scaling

- As operating frequency increases, SET latching probability increases
- As supply voltage decreases, SET generation probability increases
- As logic path length decreases, logical and electrical masking probabilities decrease

SETs may be particularly critical at clock frequencies of several GHz



Source: **N. Mahatme et al., "Comparison of Combinational and Sequential Error Rates for a Deep Submicron Process," IEEE TNS, 2011.**

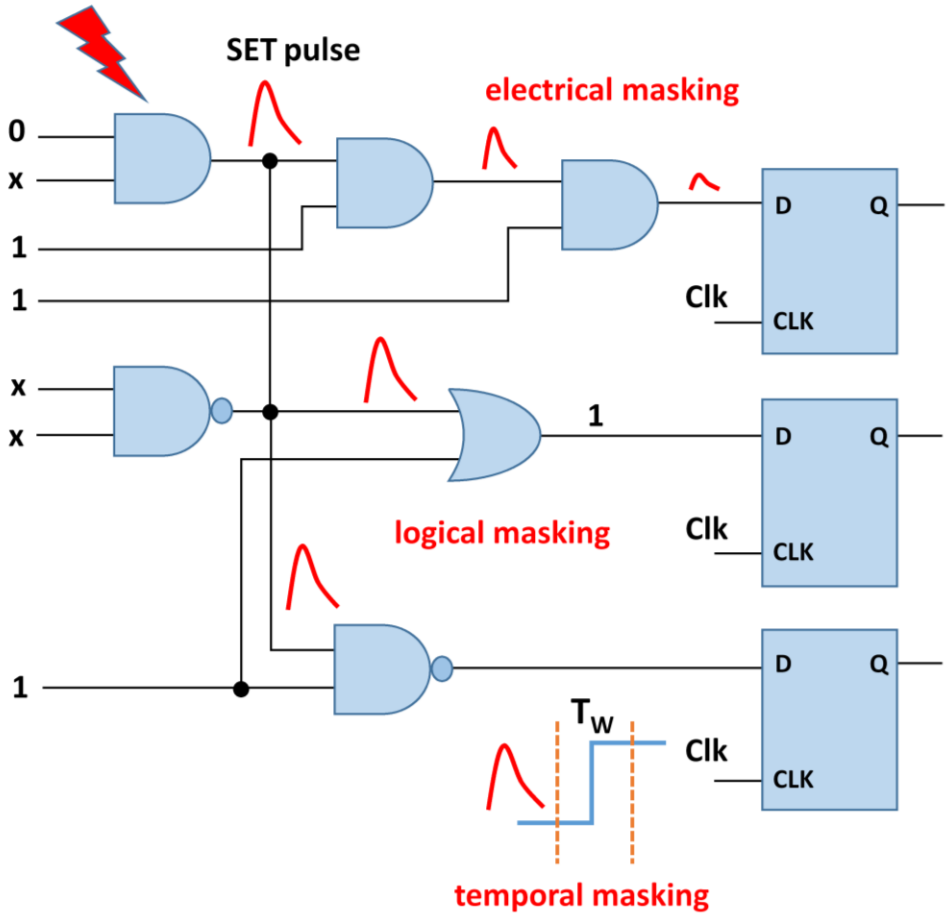
1. Motivation

SET generation

- If a particle deposits more charge than the critical charge of a circuit node, a SET pulse will be formed
- Generated SET pulse width depends on particle energy (LET) and design/operating/technology parameters

SET propagation

- SETs longer than propagation delay of logic gates may propagate through the circuit
- SETs may be masked by 3 masking effects: electrical, logical and temporal masking
- SET pulse width may increase during propagation due to Propagation-induced Pulse Broadening (PIPB)



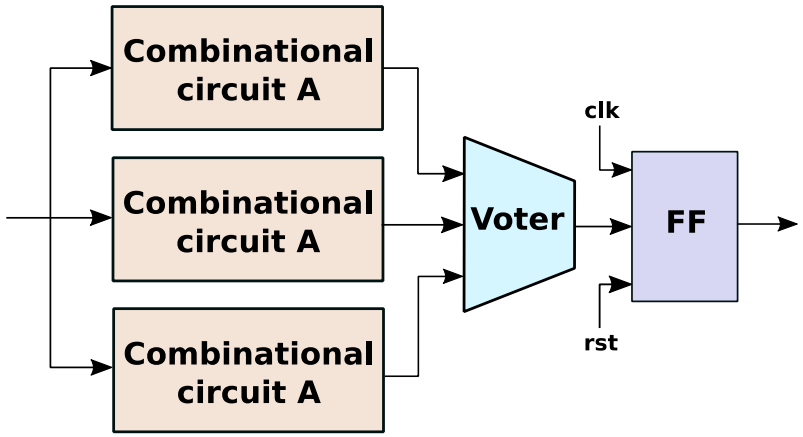
2. State-of-the-Art Solutions for SET Mitigation

- **SET mitigation should be considered from the beginning of rad-hard IC design**
  - Original design should be modified to improve tolerance to SETs, i.e., to reduce the probability that an SET will result in a soft error
- **SET mitigation means adding redundancy**
  - Different types of redundancy can be added at different abstraction layers
  - Redundancy results in increase of circuit area, power consumption and delay
  - Mitigation scheme depends on hardware platform: ASIC or FPGA
- **SET mitigation can be static or dynamic**
  - Static mitigation mechanisms are fixed, i.e., cannot be changed during runtime
  - Dynamic mitigation mechanisms can be changed during runtime

2. State-of-the-Art Solutions for SET Mitigation

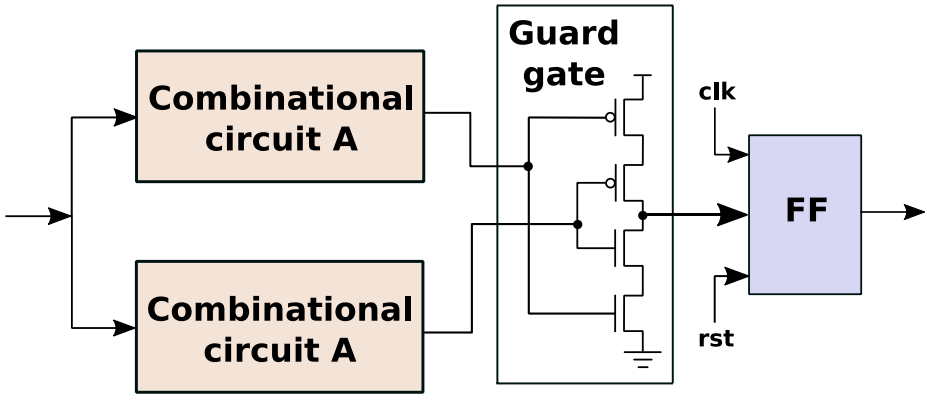
SET mitigation by spatial redundancy

Triple Modular Redundancy (TMR)



If an SET occurs in one combinational circuit, system will still work correctly

Dual Modular Redundancy (DMR) with a guard gate as a voter

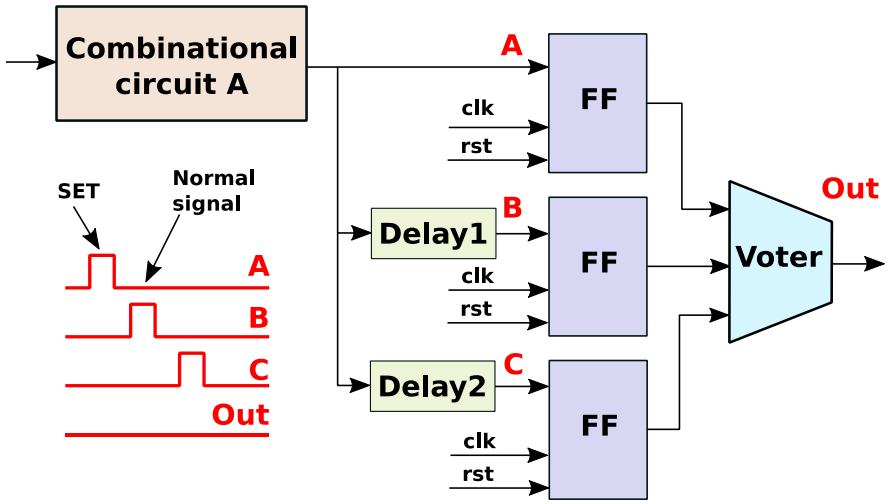


Guard gate will mask SETs coming from one circuit

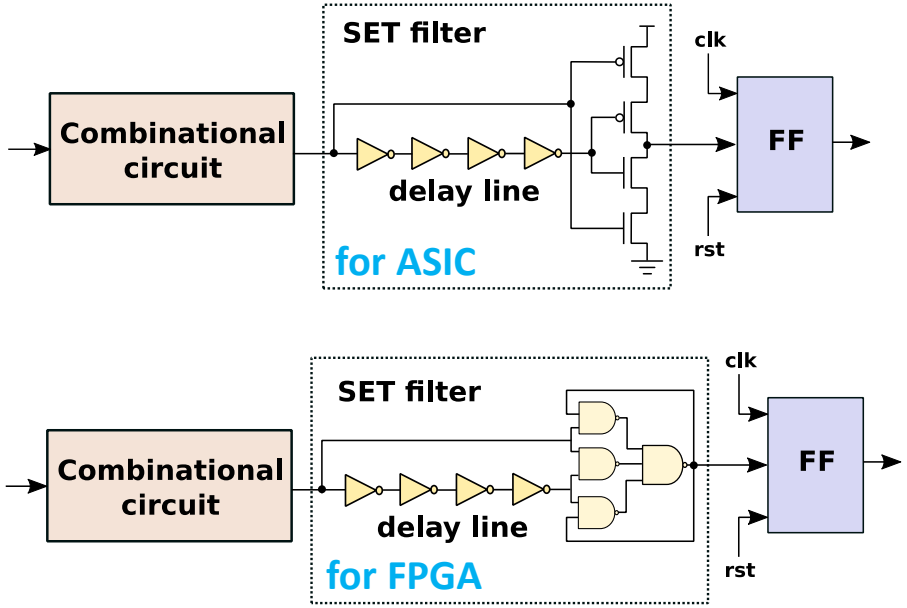
2. State-of-the-Art Solutions for SET Mitigation

SET mitigation by temporal (time) redundancy

Inserting delay in data line
(or in clock line)

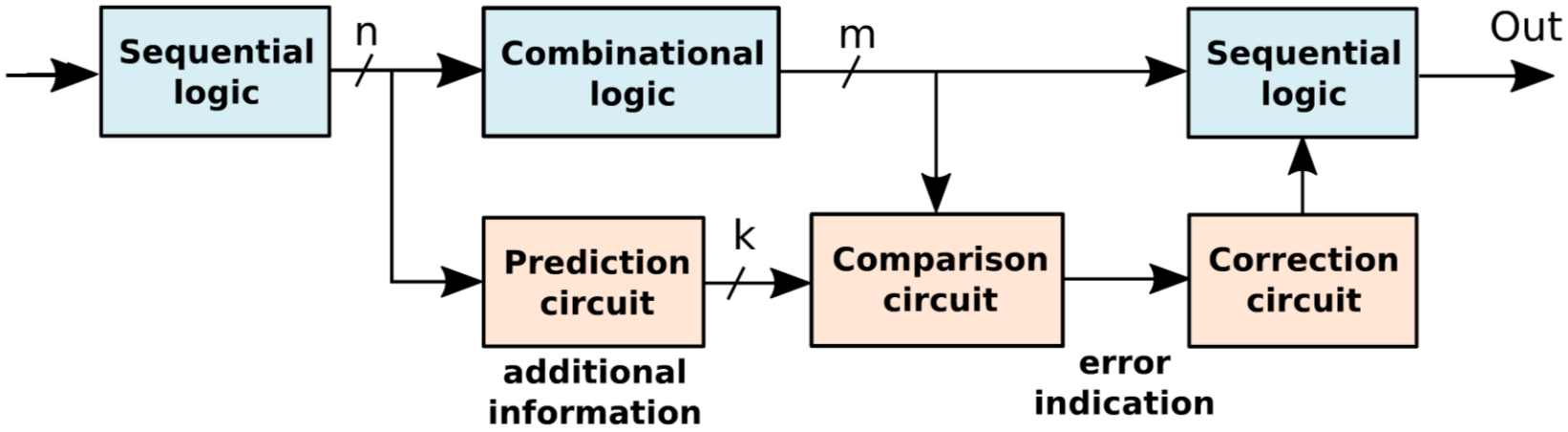


Inserting SET filter at circuit outputs
(SETs shorter than propagation delay of delay line will be masked)



2. State-of-the-Art Solutions for SET Mitigation

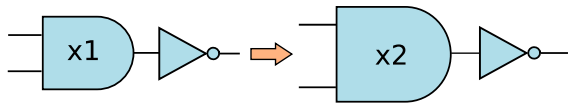
- **SET mitigation by information redundancy (error detection and correction)**
  - Errors are detected in combinational logic, and correction is applied in sequential logic
  - Lower area overhead compared to DMR and TMR



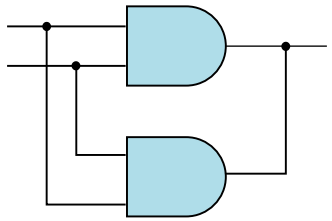
2. State-of-the-Art Solutions for SET Mitigation

Gate-level (in-circuit) SET mitigation

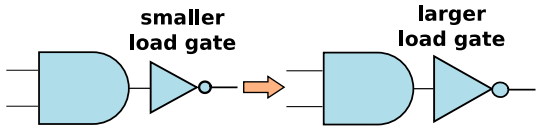
Gate Upsizing (GU)



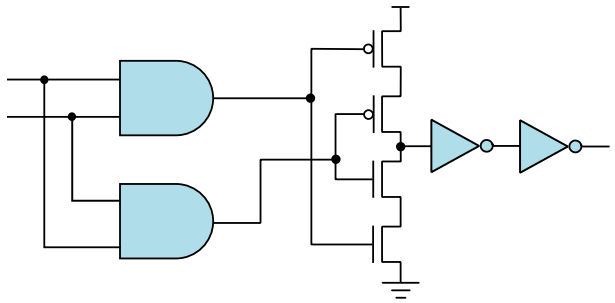
Gate Duplication (GD)



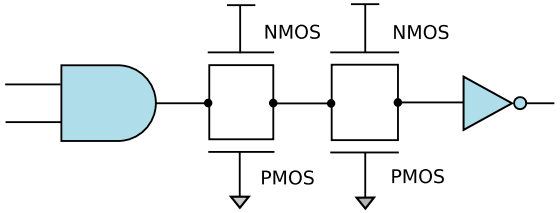
Load Upsizing (LU)



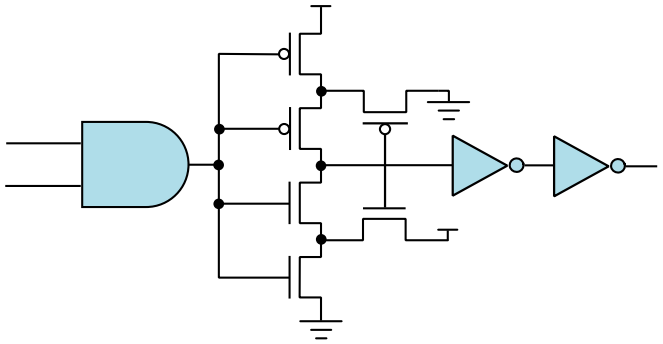
Guarded DMR (GDMR)



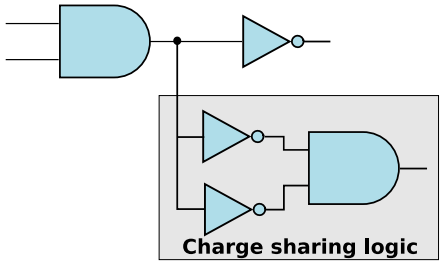
Transmission Gates (TG)



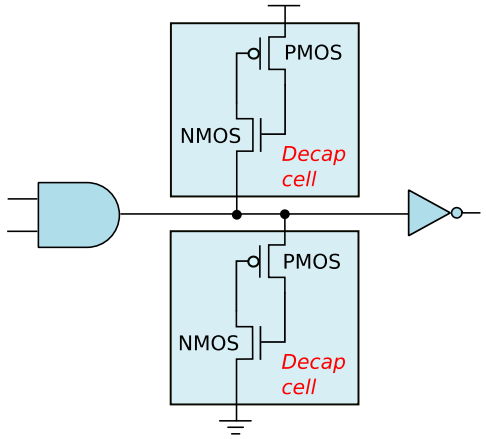
Schmitt Trigger (ST)



Charge Sharing Logic (CSL)



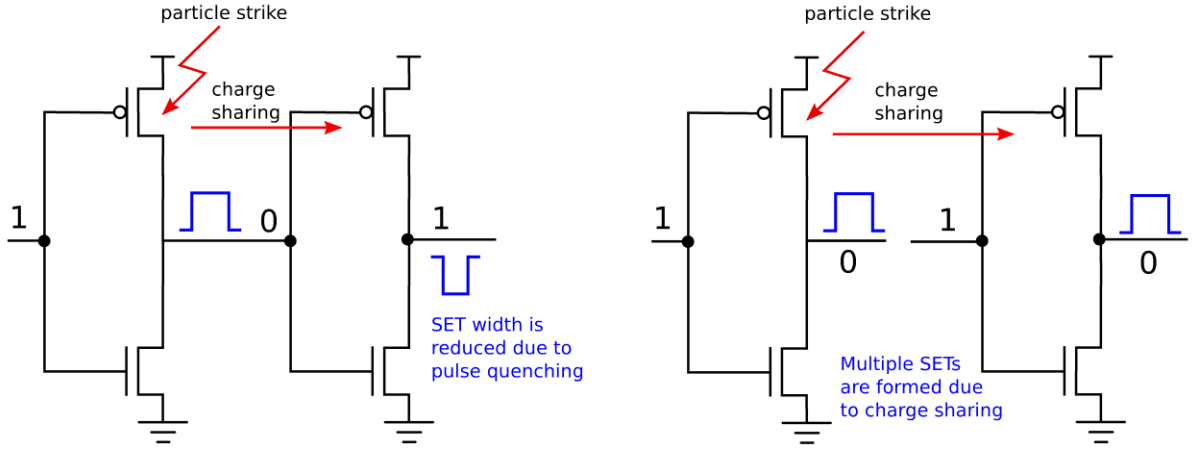
Decoupling Cells (DECAP)



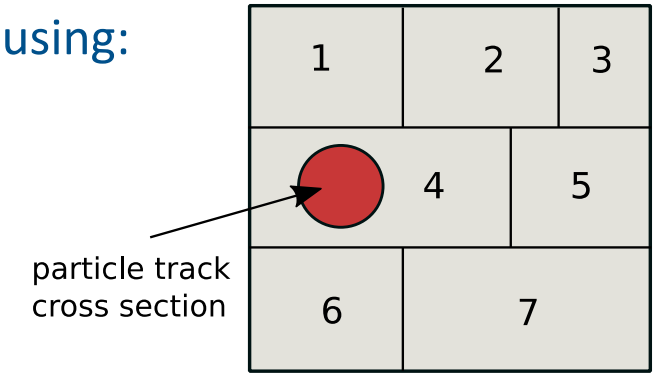
2. State-of-the-Art Solutions for SET Mitigation

Layout-based SET mitigation

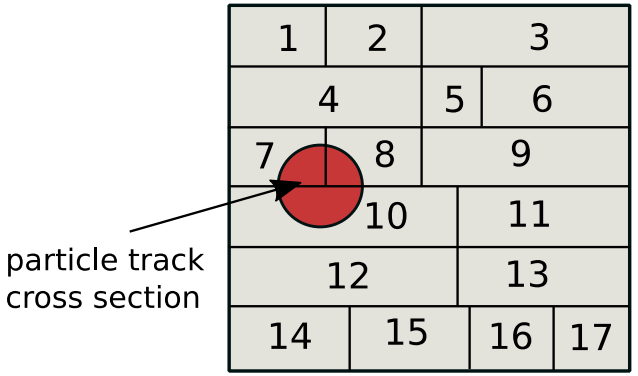
- In scaled technologies, a single particle may hit multiple transistors, causing:
  - **Multiple SETs** (possibly resulting in multiple soft errors)
  - **SET pulse quenching** (suppression of SET pulse)
- SET mitigation approaches:
  - Increasing space between cells which are prone to multiple SETs
  - Placing cells which can result in quenching as close as possible



In older CMOS technologies, a particle may hit one cell



In newer CMOS technologies, a particle may hit multiple cells

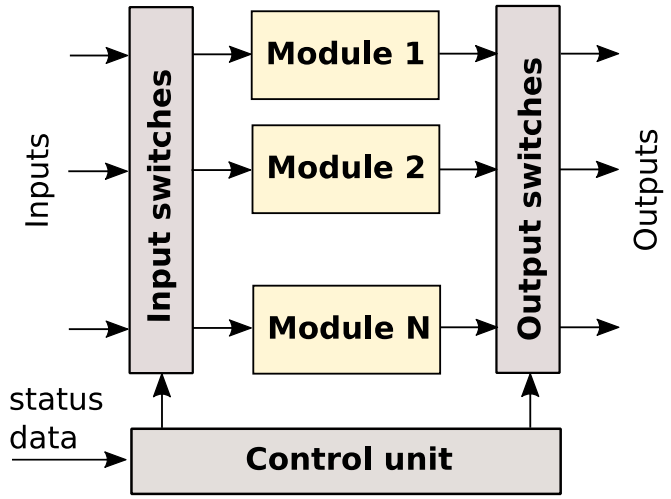


2. State-of-the-Art Solutions for SET Mitigation

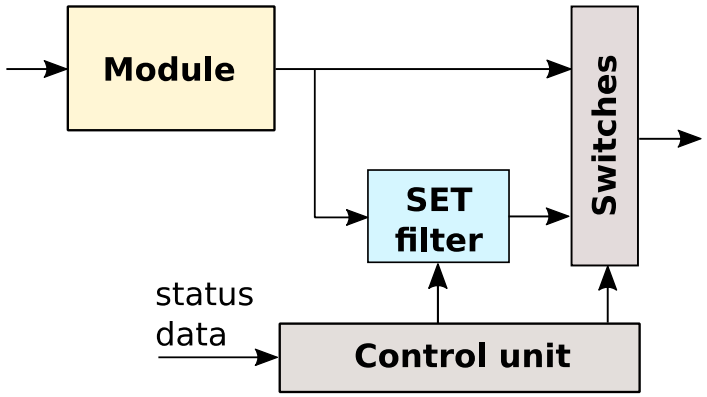
Adaptive/dynamic/reconfigurable/tunable SET mitigation

- Due to changing radiation intensity in space, static mitigation approaches are not optimal
- Adaptive techniques allow a trade-off between performance, power consumption and fault-tolerance
- Adaptive techniques can be activated under high radiation intensity (detected with radiation sensors)

Reconfigurable N-modular redundancy



Reconfigurable SET filtering



3. Overview of Gate-level SET Mitigation Techniques

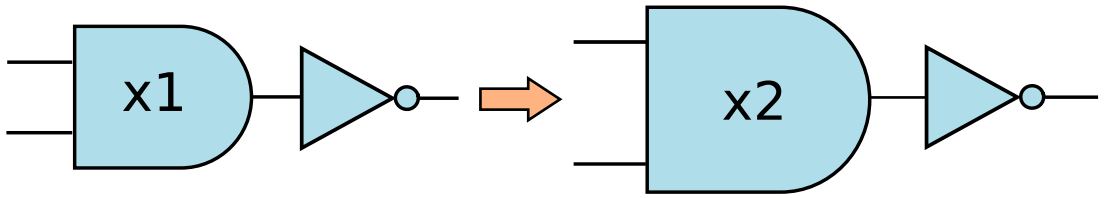
- **Due to masking effects, not all combinational gates in a circuit will contribute to soft error rate**
  - Selective hardening of a small subset of gates in a circuit can significantly improve the soft error rate of a circuit with minimum area and power overhead

- **Enhancing the SET robustness of standard cells without modifying the cell design**
  - Replacing one gate with another having better SET tolerance
  - Duplication or triplication of standard cell
  - Insertion of redundant logic at the output of the cell

3. Overview of Gate-level SET Mitigation Techniques

Gate Upsizing

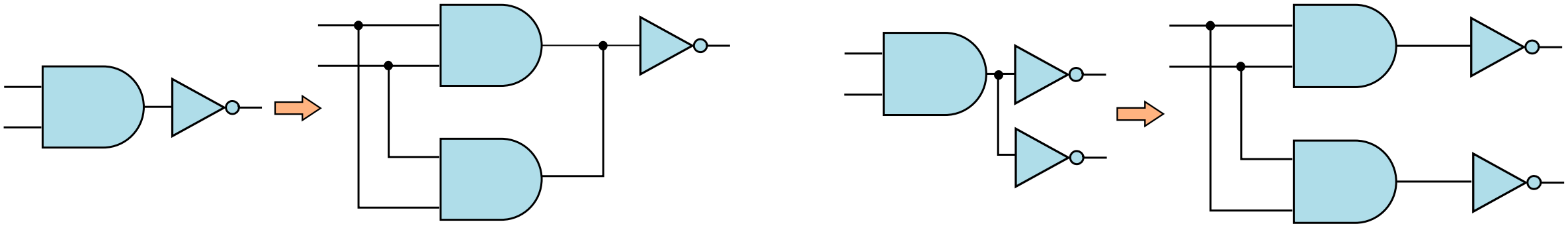
- Replacing a smaller gate with a larger gate of the same type
- Larger gates have larger critical charge and are thus more robust to particle strikes
- Critical charge of all nodes increases proportionally to gate (transistor) size
- Drawback: reduced SET filtering capability, unless the gate is significantly upsized (e.g. x20)



3. Overview of Gate-level SET Mitigation Techniques

Gate Duplication

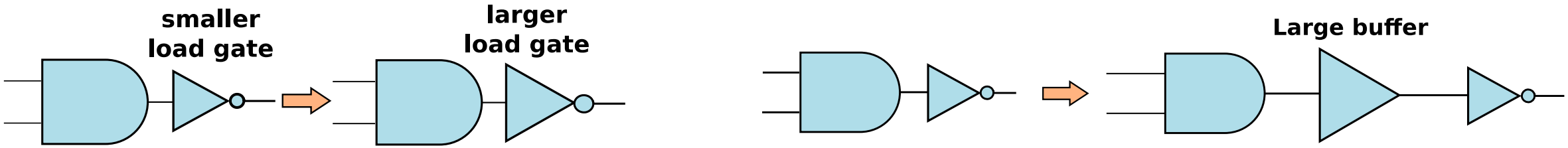
- Two gates of the same type are connected at inputs (and possibly outputs)
- Effect on SET mitigation is similar as gate upsizing
- Could be used instead of gate upsizing if large gates are not available in the standard cell library
- Could be useful in reducing SET propagation probability in branching nodes



3. Overview of Gate-level SET Mitigation Techniques

Load Upsizing

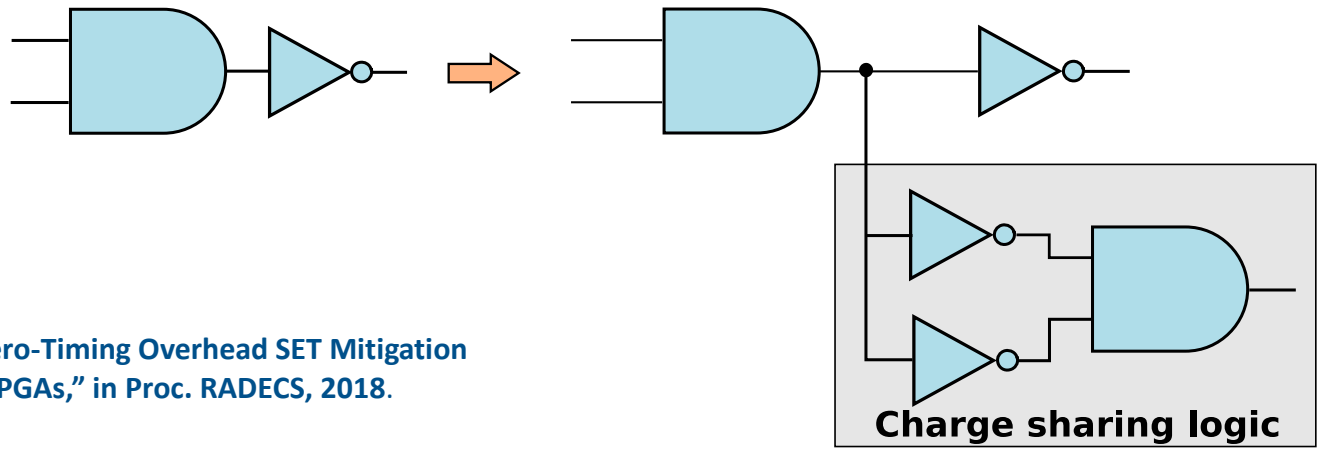
- Replacing a smaller load gate with a larger load gate of the same type
- Critical charge at the output node of target gate is increased
- If load gate is significantly larger than target gate, short SETs could be filtered
- Load can be upsized by inserting a large buffer (can be considered as a separate technique)



3. Overview of Gate-level SET Mitigation Techniques

Charge Sharing Logic

- A “dummy” logic is added to the output of a target gate
- Added logic can be composed of any logic gates
- Output of added logic is floating (does not affect the circuit functionality)
- Applicable to both ASIC and FPGA

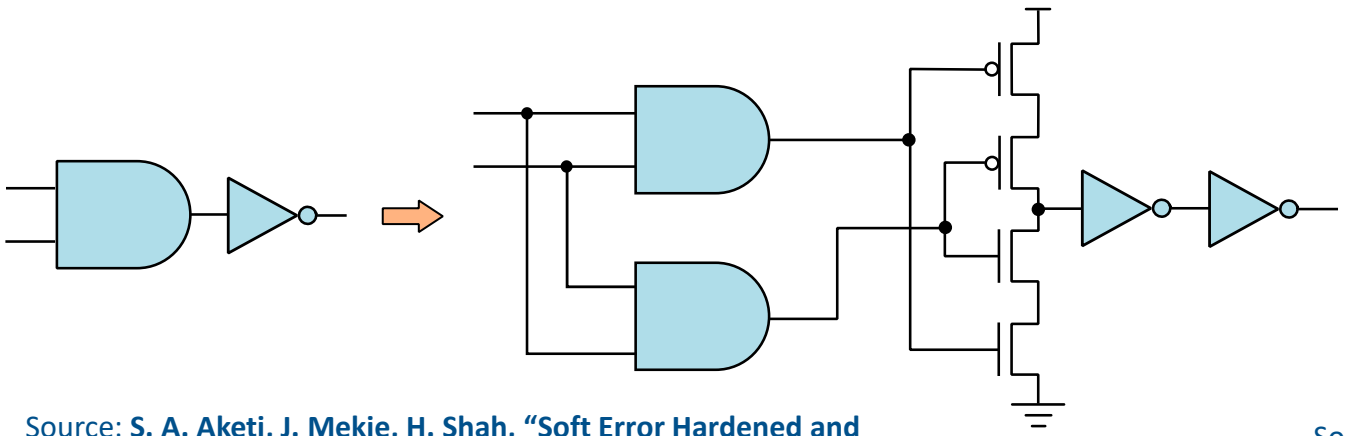


Source: **S. Azimi et al., “A Zero-Timing Overhead SET Mitigation Approach for Flash-Based FPGAs,” in Proc. RADECS, 2018**.

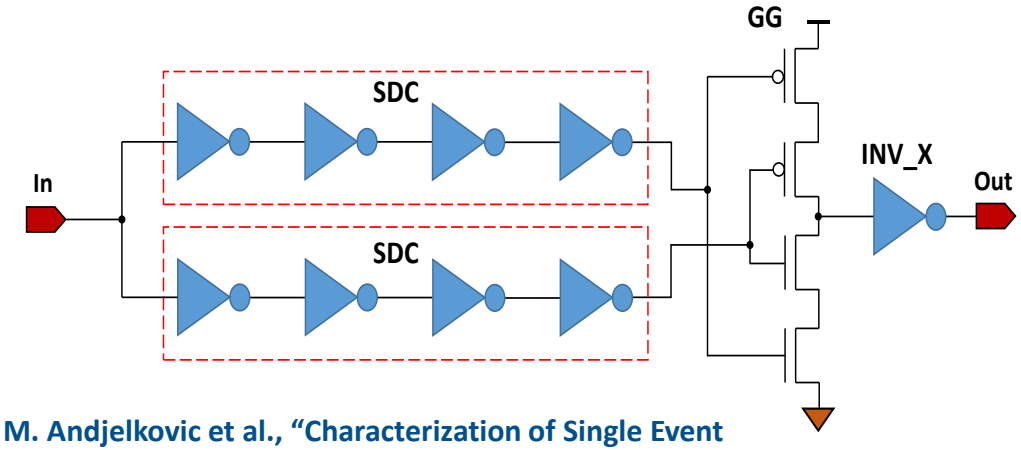
3. Overview of Gate-level SET Mitigation Techniques

Guarded Dual Modular Redundancy

- A target gate is replicated and both gates are connected to a guard gate
- An inverter has to be added to maintain the signal polarity
- Main disadvantage – large area overhead
- Suitable for some specific logic gates, such as standard delay cells (SDC)



Source: **S. A. Aketi, J. Mekie, H. Shah, "Soft Error Hardened and Multiple Error Tolerant Guarded Dual Modular Redundancy Technique," in Proc. VSLID, 2018.**

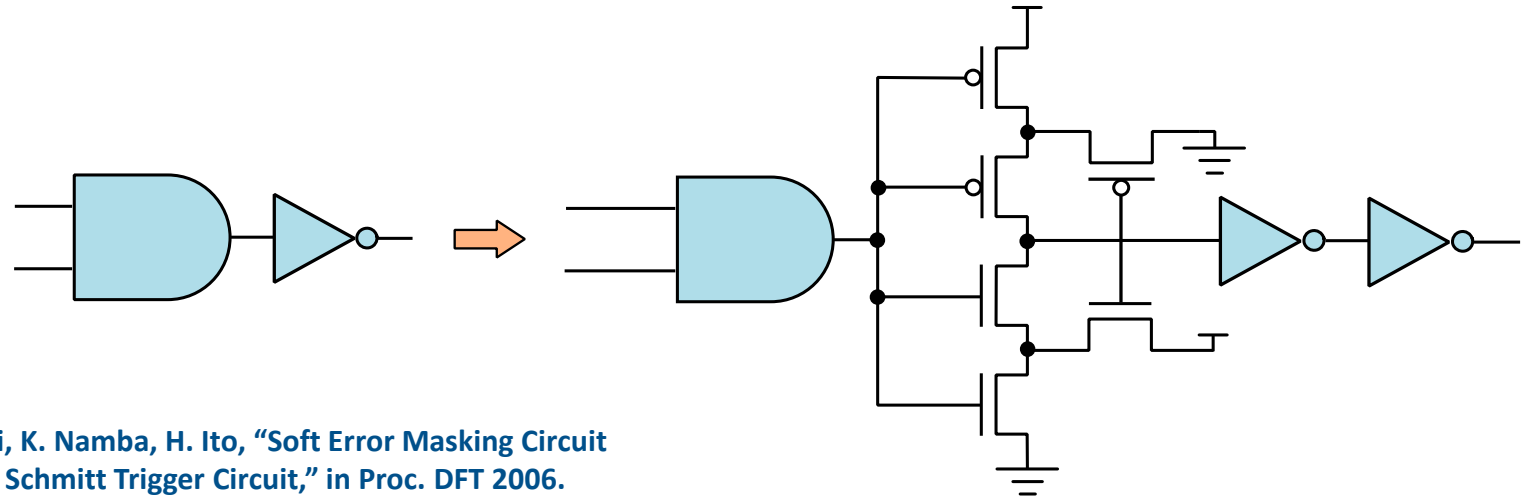


Source: **M. Andjelkovic et al., "Characterization of Single Event Transient Effects in Standard Delay Cells," in Proc. ICECS, 2020.**

3. Overview of Gate-level SET Mitigation Techniques

Schmitt Trigger

- A circuit with hysteresis property
- Can filter a wide range of noise signals
- Composed of 6 transistors plus an inverter to maintain the signal polarity
- Main disadvantage – large area and power overhead

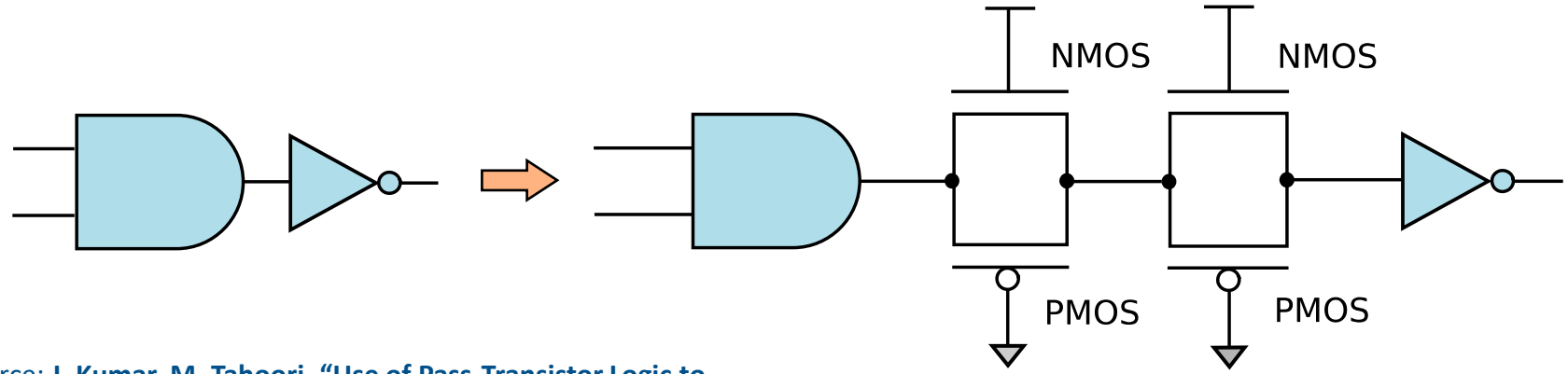


Source: **Y. Sasaki, K. Namba, H. Ito, "Soft Error Masking Circuit and Latch Using Schmitt Trigger Circuit," in Proc. DFT 2006.**

3. Overview of Gate-level SET Mitigation Techniques

Transmission Gates

- NMOS and PMOS transistors connected in parallel act as a switch
- If gates of NMOS and PMOS are at fixed level ensuring that both transistor are on, this structure will act as a SET filter
- Multiple transmission gates connected in series enhances the SET suppression



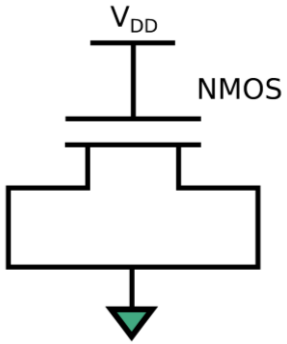
Source: **J. Kumar, M. Tahoori, "Use of Pass-Transistor Logic to Minimize the Impact of Soft Errors in Combinational Circuits," in Proc. SELSE, 2005.**

3. Overview of Gate-level SET Mitigation Techniques

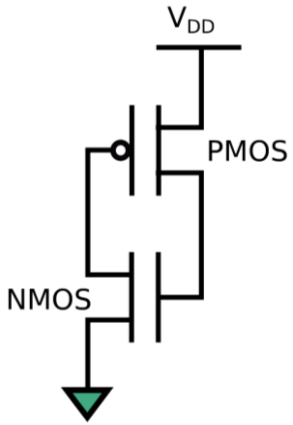
Decoupling Cells

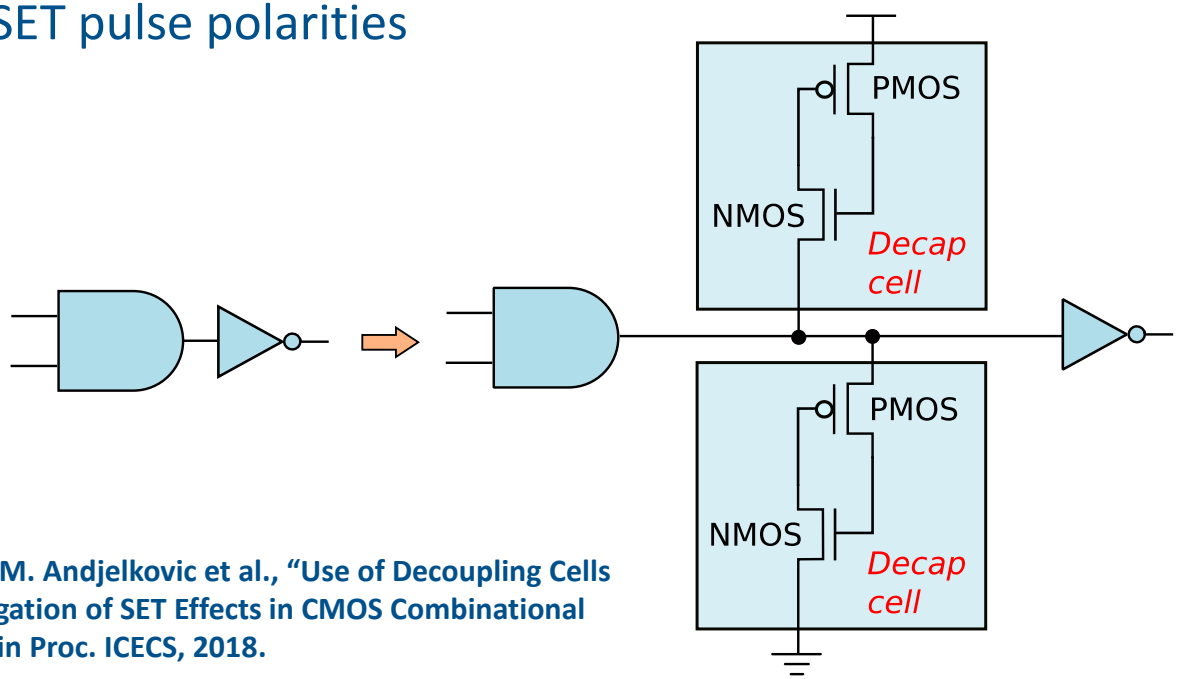
- Composed of one or two transistors arranged as a capacitor
- Available as standard cells, used for power supply noise filtering
- Two decoupling cells are needed to suppress both SET pulse polarities

1-transistor decoupling cell



2-transistor decoupling cell





Source: **M. Andjelkovic et al., "Use of Decoupling Cells for Mitigation of SET Effects in CMOS Combinational Gates," in Proc. ICECS, 2018.**

4. Comparison of Gate-level SET Mitigation Techniques

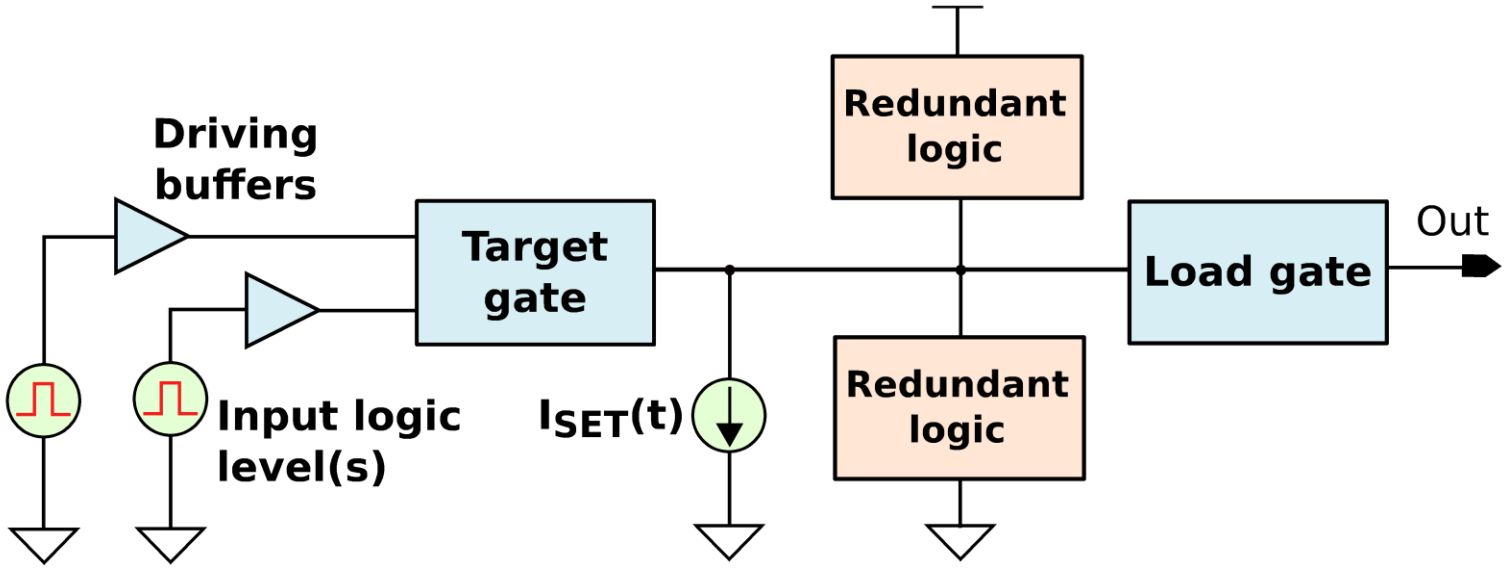
Analysis methodology

- Analysis was done with electrical simulations using Cadence Spectre tool
- Target standard cell library: IHP's 130nm standard cell library
- Analyzed cells: INV, BUF, NAND2, NOR2, AND2, OR2, XOR2, XNOR2
- Nominal supply voltage and temperature have been used in all simulations
- 3 SET parameters have been studied:
  - *Critical charge*
  - *Generated SET pulse width*
  - *Propagated SET pulse width*

4. Comparison of Gate-level SET Mitigation Techniques

Analysis methodology – SET generation

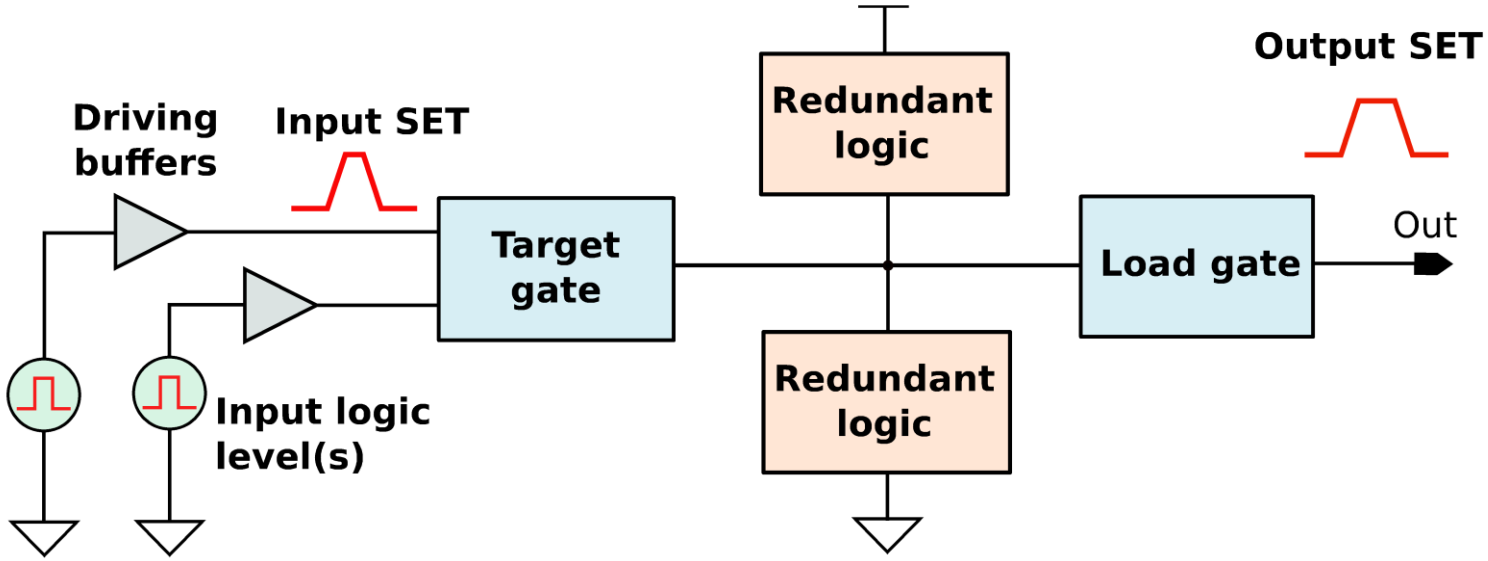
- Double-exponential current source is used to determine critical charge
- Bias-dependent current model is used to determine generated SET pulse width



4. Comparison of Gate-level SET Mitigation Techniques

Analysis methodology – SET propagation

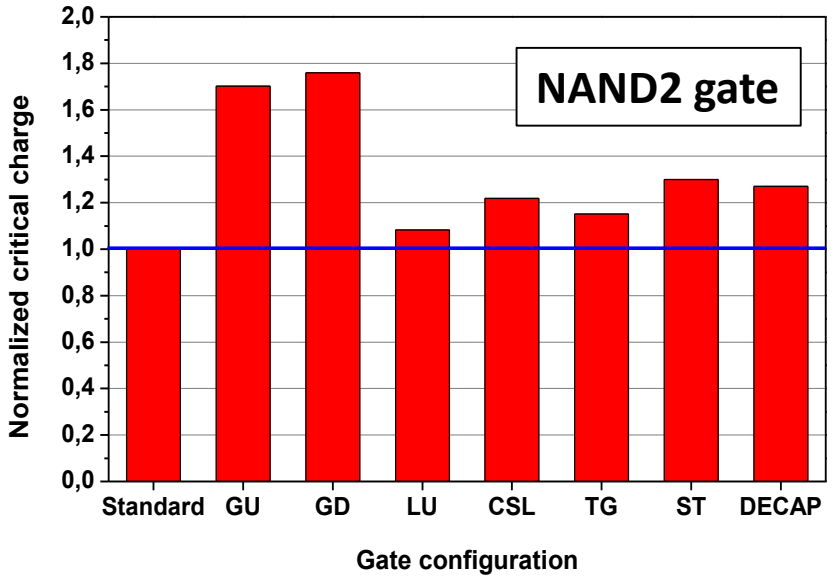
- Trapezoidal voltage pulse was used to evaluate SET propagation

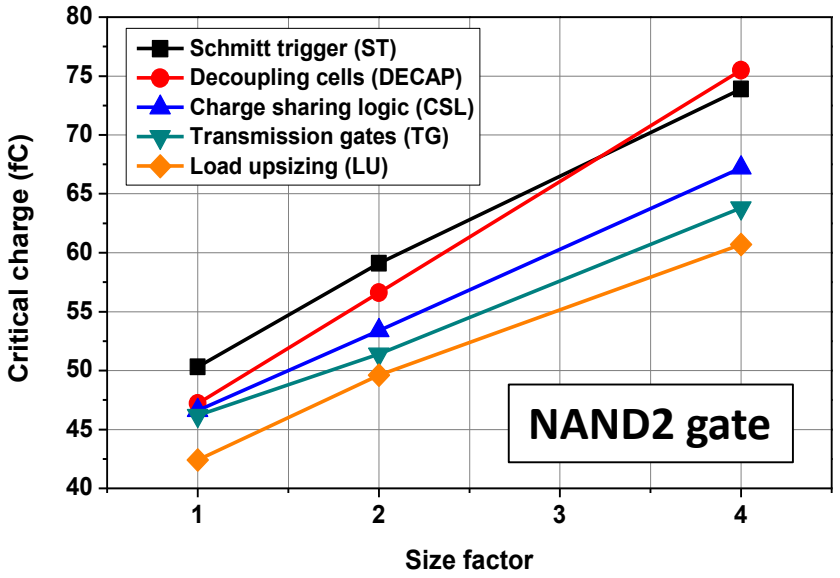


4. Comparison of Gate-level SET Mitigation Techniques

Critical charge comparison

- Gate upsizing and gate duplication have best effect on critical charge increase
- For techniques based on insertion of additional logic, critical charge of the target node increases linearly with the size of transistors in added logic

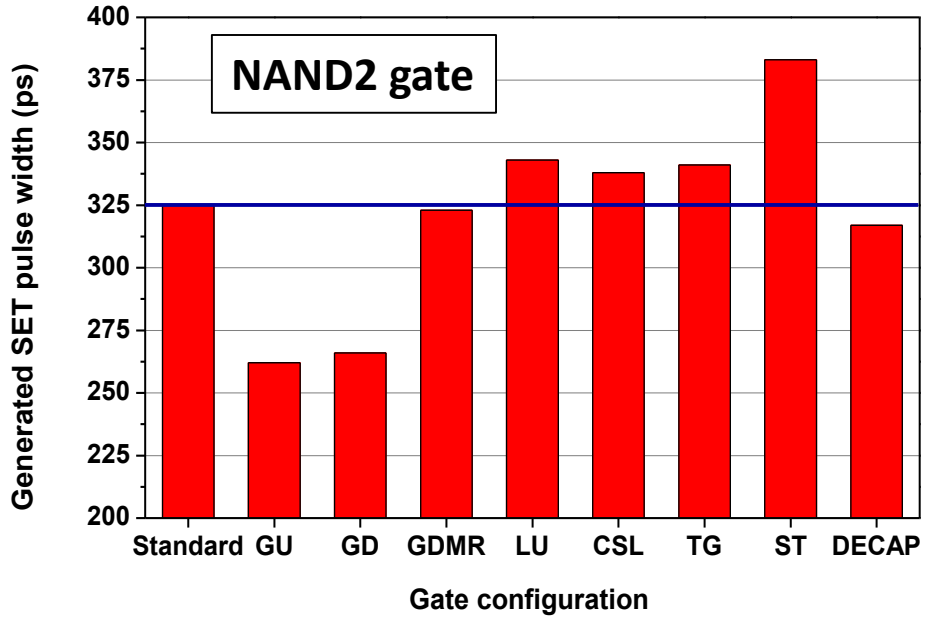




4. Comparison of Gate-level SET Mitigation Techniques

Generated SET pulse width comparison

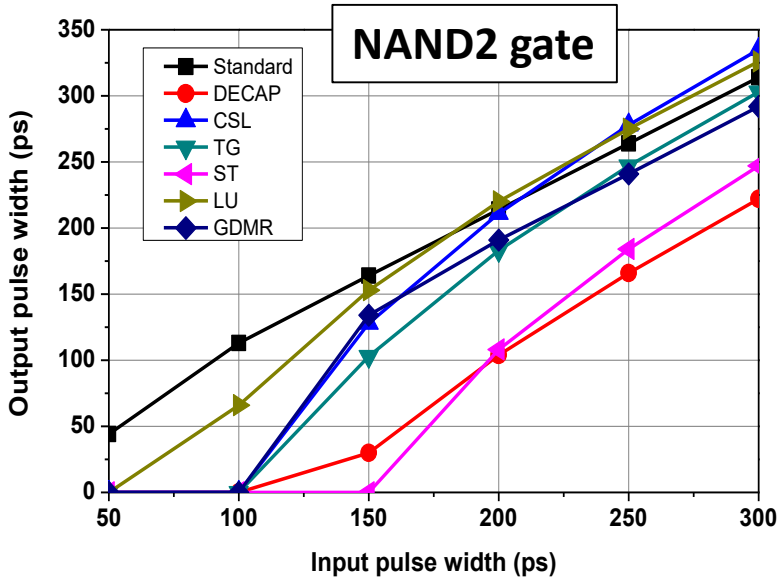
- Gate upsizing and gate duplication lead to reduction of generated SET pulse width
- Techniques based on insertion of redundant logic lead to an increase in the generated SET pulse width, which is not desirable – this effect is due to added capacitance

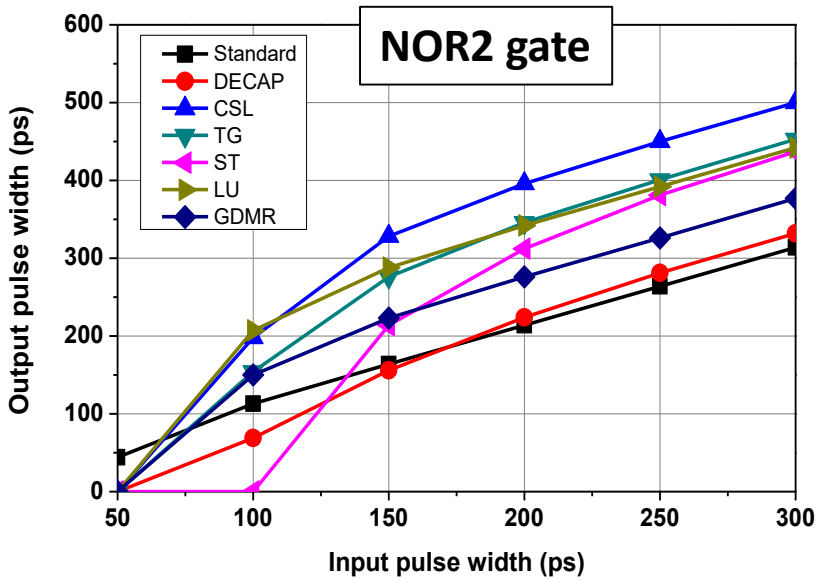


4. Comparison of Gate-level SET Mitigation Techniques

Propagated SET pulse width comparison

- Better SET filtering can be achieved with larger transistors in added logic
- SETs up to 200 ps can be suppressed or completely filtered
- Impact of added logic differs depending on the target gate





4. Comparison of Gate-level SET Mitigation Techniques

Area overhead per gate

Cell configuration	Normalized area							
	INV	BUF	NAND2	AND2	NOR2	OR2	XNOR2	XOR2
Standard cell with x1 size	1	1	1	1	1	1	1	1
GU	1.15	1.15	1.28	1.28	1.13	1.13	1.27	1.27
GD	1.47	1.58	1.57	1.63	1.57	1.63	1.73	1.73
GDMR	2.94	2.95	2.92	2.97	2.92	2.97	2.99	2.99
LU	1.15	1.15	1.14	1.13	1.14	1.13	1.09	1.09
CSL	1.99	1.86	1.86	1.76	1.86	1.76	1.55	1.55
TG	1.99	1.86	1.86	1.76	1.86	1.76	1.55	1.55
ST	2.5	2.3	2.3	2.1	2.3	2.1	1.8	1.8
DECAP	1.99	1.86	1.86	1.76	1.86	1.76	1.55	1.55

Gate upsizing and load upsizing introduce minimum area overhead

Techniques with larger number of additional transistors introduce larger area overhead

4. Comparison of Gate-level SET Mitigation Techniques

Delay overhead per gate

Cell configuration	Delay (ps)							
	INV	BUF	NAND2	AND2	NOR2	OR2	XNOR2	XOR2
Standard cell with x1 size	73	103	85	128	75	106	109	145
GU	74	99	89	119	80	103	110	153
GD	77	104	89	130	79	109	112	148
GDMR	173	181	189	203	176	184	220	244
LU	78	112	96	134	81	110	114	142
CSL	88	133	109	155	90	136	133	196
TG	105	149	128	173	109	152	151	210
ST	156	165	180	189	159	168	206	232
DECAP	84	123	143	174	104	151	171	252

Gate upsizing, gate duplication and load upsizing introduce minimum delay overhead

Techniques with larger number of additional transistors introduce larger delay overhead

4. Comparison of Gate-level SET Mitigation Techniques

Power overhead per gate

Cell configuration	Normalized power							
	INV	BUF	NAND2	AND2	NOR2	OR2	XNOR2	XOR2
Standard cell with x1 size	1	1	1	1	1	1	1	1
GU	1.02	1.06	1.13	1.21	1.18	1.22	1.25	1.26
GD	1.06	1.10	1.15	1.23	1.21	1.23	1.27	1.29
GDMR	2.82	2.89	2.94	2.95	2.94	2.95	2.94	2.94
LU	1.12	1.13	1.15	1.19	1.17	1.19	1.20	1.20
CSL	1.86	1.87	1.89	2.02	2.01	2.02	2.05	2.05
TG	1.92	1.94	1.97	1.99	1.98	2.01	2.03	2.03
ST	2.65	2.68	2.72	2.75	2.72	2.73	2.73	2.72
DECAP	1.89	1.92	1.95	1.96	1.95	1.96	1.96	1.94

Gate upsizing, gate duplication and load upsizing introduce minimum power overhead

Techniques with larger number of additional transistors introduce larger power overhead

4. Comparison of Gate-level SET Mitigation Techniques

- **SET Mitigation Efficiency (SME) per logic gate (SET mitigation cost)**

$$SME\ (SET\ metric, overhead\ metric) = \frac{SET\ sensitivity\ metric\ change}{Overhead\ metric\ change}$$

SET sensitivity metric change – change in critical charge, generated SET pulse width or propagated SET pulse width after applying a SET mitigation technique

Overhead metric change – change in area, delay or power consumption after applying a SET mitigation technique

5. Combined Use of Multiple SET Mitigation Techniques

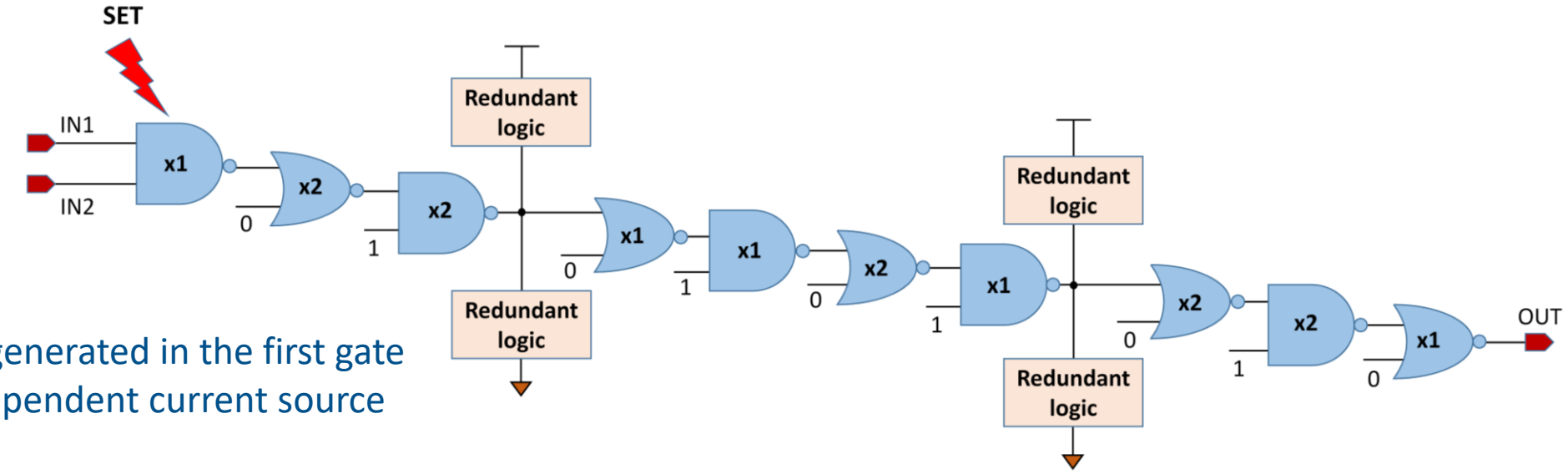
- **A single gate-level SET mitigation technique would not be sufficient for a real circuit**
  - There is no a single technique that is suitable for all standard cells
  - Some techniques have weak impact on SET generation or SET propagation
  - Some techniques introduce large area/delay/power overhead

- **Solution for SET mitigation in a combinational circuit – combination of multiple techniques**
  - To exploit the best features of multiple techniques
  - To achieve optimal SET mitigation with minimum cost (overhead)

5. Combined Use of Multiple SET Mitigation Techniques

Case study: SET mitigation in a 10-gate NAND-NOR path

- An SET pulse is injected in the first gate using bias-dependent current source
- Gate upsizing is most effective for enhancing the SET robustness of first gate
- Additional techniques are applied to enhance the SET filtering across the path



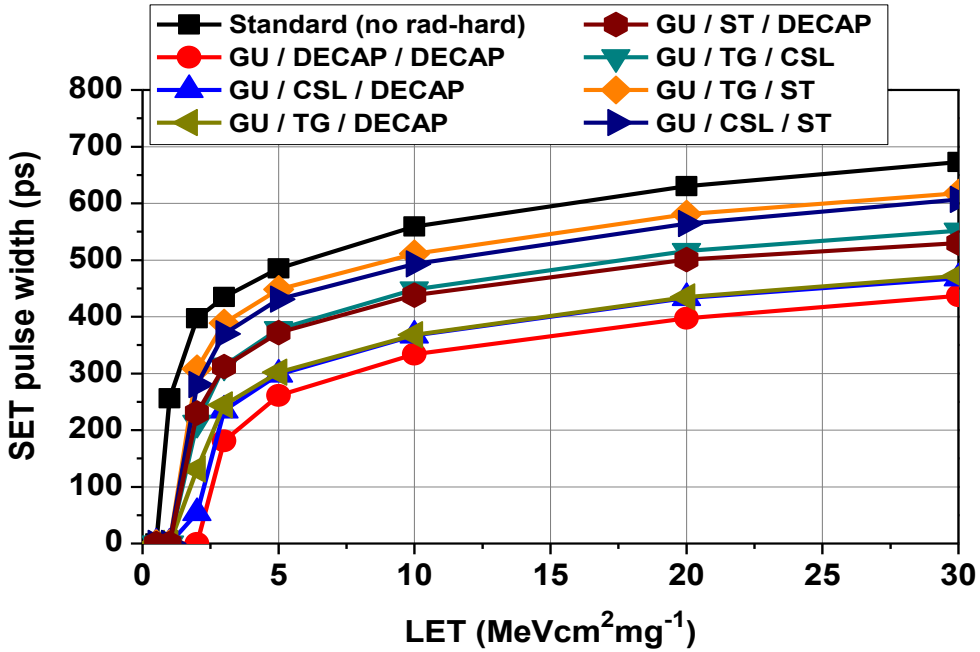
SET pulse is generated in the first gate using bias-dependent current source

5. Combined Use of Multiple SET Mitigation Techniques

Case study: SET mitigation in a 10-gate NAND-NOR path

- Use of multiple techniques can reduce the SET pulse width by 50 % or more
- Best combination of techniques depends on the target combinational path

Path configuration	Output SET pulse width for LET of 30 MeVcm^{2}mg^{-1} (ps)	Propagation delay of the path (ps)
Logic path without hardening	673	471
GU / DECAP / DECAP	437	660
GU / CSL / DECAP	468	657
GU / TG / DECAP	472	649
GU / ST / DECAP	530	771
GU / TG / CSL	552	652
GU / CSL / ST	607	732
GU / TG / ST	618	744



6. Conclusion

- **SET mitigation has to be applied when designing chips for space missions**

- **Gate-level SET mitigation techniques**
  - Each technique has certain benefits but also limitations
  - Gate upsizing is the best technique for reducing SET generation probability
  - Techniques based on insertion of redundant logic are suitable for SET propagation suppression
  - Combination of multiple techniques is required for optimal SET suppression

- **Possible research directions**
  - More detailed analysis of all gate-level techniques, considering a wider range of standard cells and multiple technologies, as well as real irradiation conditions
  - Setting up an approach for selection of an optimal combination of SET mitigation techniques

References

Publications on comparative analysis of gate-level SET mitigation techniques (results shown in this presentation have been published in references 1 and 3):

1. M. Andjelkovic, M. Krstic, “Comparison of Gate-Level Techniques for Mitigation of Single Event Transients in Combinational Logic,” LASCAS 2025.
2. H. Kessler et al., “Single Event Transient on Combinational Logic: An Introduction and their Mitigation,” Journal of Integrated Circuits and Systems, 2022.
3. M. Andjelkovic, “Characterization, Modeling and Mitigation of Single Event Transient Effects in Standard CMOS combinational Cells,” PhD Thesis, University of Potsdam, 2021.
4. L. Zimpeck, “Circuit-level Approaches to Mitigate the Process Variability and Soft Errors in FinFET Logic Cells,” PhD Thesis, Federal University of Rio Grande do Sol and University of Toulouse, 2019.
5. S. Sayil, “A Survey of Circuit-level Soft Error Mitigation Methodologies,” Analog Integrated Circuits and Signal Processing, 2018.
6. V. Sharma, A. Rajawat, “Review of Approaches for Radiation Hardened Combinational Logic in CMOS Silicon Technology,” IETE Technical Review, 2017.

Thank you for your attention!

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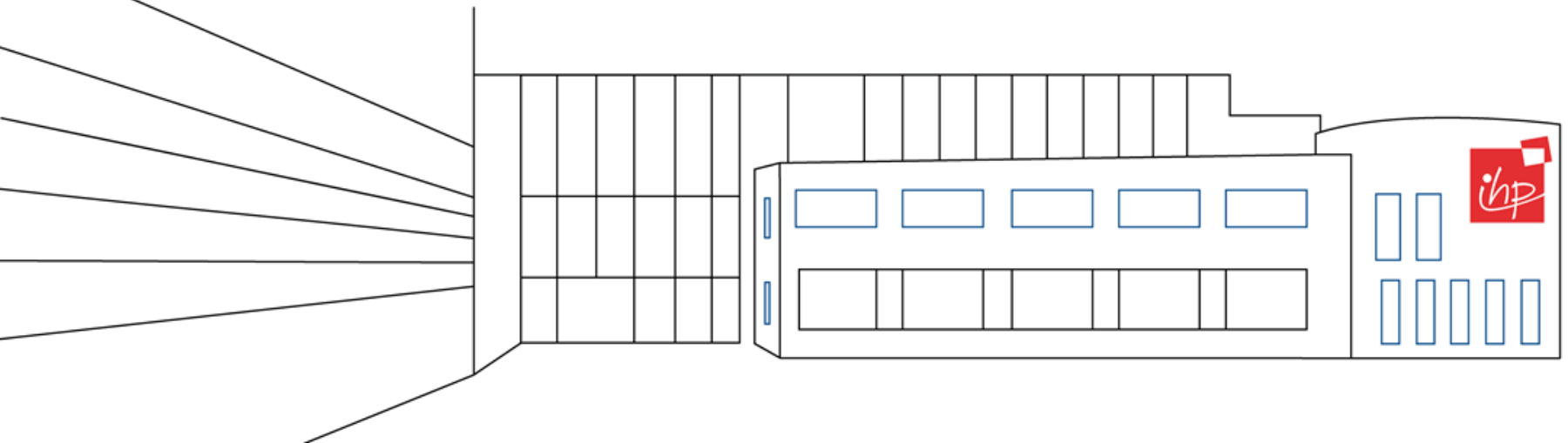

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