Open Source EDA

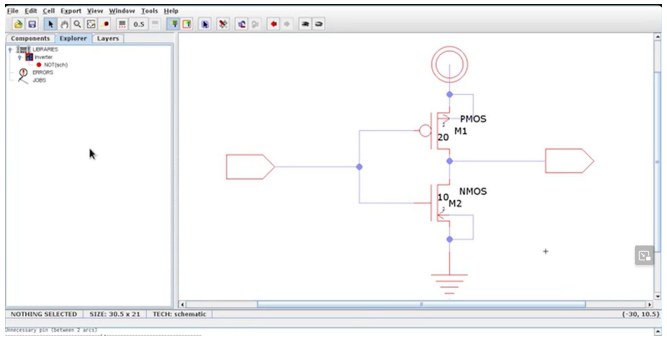
Symbiotic EDA

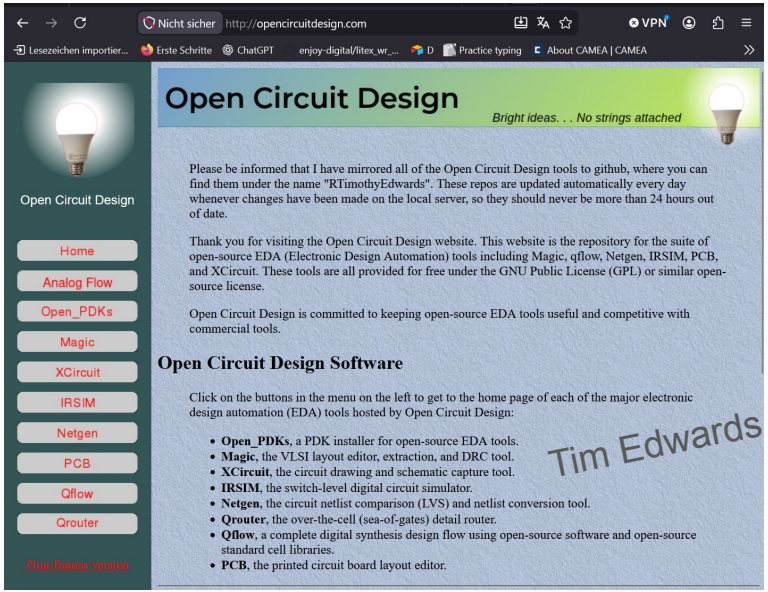
The past of open-source chip design tools

All started in Berkeley, CalTech, Larry Nagel, Carver Mead, Lynn Conway

Community-driven EDA development was a
fragmented set of academic and community tools.

Magic, Netgen, GNUCap, Qrouter, IRSIM
Xyce
Electric VLSI
Xschematic
ngspice





Why using “shitty” open source EDA …

…. when industry standard tools from Cadence and Synopsys are available for very cheap from Europractice?

Access to tools is essential for learning, but …

One in four employees in the semiconductor industry is over the age of 55. The number of applicants for related STEM degree programmes continues to decline and dropout rates remain high.

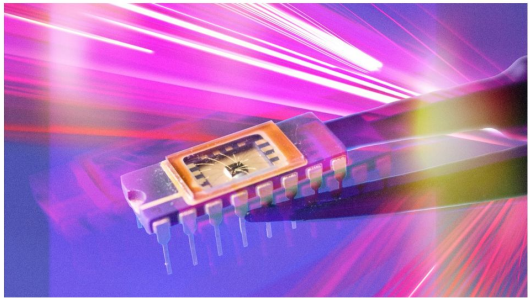
“We need to improve if we are to meet this enormous additional demand.”

The BMBF flagship project “**skills4chips**” is intended to achieve this in close cooperation with other initiatives.

Chip Design Germany, 28 European Chip Competence Centers, …

…many academics have difficulty to access proprietary tools.

- administrative process
- cost of membership
- qualification to administer tools



First chip ever to be fabricated from Bosnia and Herzegovina, designed at the Faculty of Electrical Engineering, University of Banja Luka

We fabricated the first IC designed in B&H

Aleksandar Pajkanovic
University Professor & RISC-V CPU Design Engineer | Bridging Academia and Industry

June 5, 2023

In 2019, supported only by friends from Austria and US, I dared to take a shot at a chance you get once in a life time.

About two weeks ago, an article swooped around 30 internet portals in Bosnia and Herzegovina. Three televisions with country-wide frequency reported on the same matter. These articles and reports **were about science and technology**, not politics or terrible accidents. So, what was ***it, what was so important*** that both the media and the public reacted in such a supportive manner?

Freedom to learn

EDUCAÇÃO NA INDÚSTRIA: MICROELETRÓNICA

Ampliando o Acesso ao Desenho de *Chips*: Desafios na Disponibilidade de Ferramentas EDA e o Aumento de Ecossistemas em Código Aberto

Expanding Access to Chip Design: Challenges in EDA Tool Availability and the Rise of Managed Open-Source Ecosystems

Por Juan Moya · By Juan Moya

doi. 10.5281/zenodo.19332658

Juan Moya

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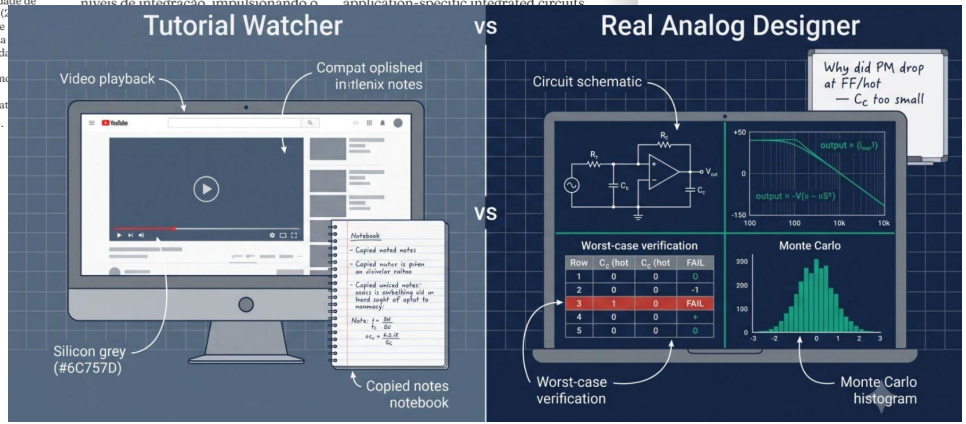
doutorado pela Universida
Industrial de Santander.
Atualmente trabalha com
investigador em pós-
doutoramento no Internat
Iberian Nanotechnology

Os sistemas eletrónicos estão cada vez mais incorporados em aplicações do nosso dia-a-dia, particularmente em dispositivos *wearable* e inteligentes utilizados para monitorização fisiológica em tempo real e de longo prazo, e processamento de dados [1–3]. Estas soluções inteligentes requerem *form factors* extremamente pequenos, baixo consumo de energia e elevados níveis de integração, impulsionando o

Electronic systems are becoming increasingly embedded in everyday applications, particularly smart wearable devices used for real-time , long term physiological monitoring and data processing [1–3]. These intelligent solutions require extremely small form factors, low power consumption and high levels of integration, driving the development of application-specific integrated circuits



Deepak Sharda · 2.
asic & micro-arch @vicharak
11 Std. • Bearbeitet •

Vernetzen

Just submitted my first ASIC for tapeout - 🥳

Well second , but first one where i have done the complete flow myself.

a dual-core programmable I/O coprocessor on GlobalFoundries 180nm.
The design is a port of **bunnie huang** BIO (Betrusted I/O) coprocessor to the GF180MCU 5V process, targeting **wafer.space** shuttle Run 2.

Two PicoRV32 RISC-V cores, 4 KB of foundry SRAM across 8 hard macros, 32 bidirectional GPIO, clock gating, and an SPI slave interface ,all in a half-width die slot (1936 × 5122 µm).

The hardest part wasn't the RTL. It was fitting 8 SRAM macros (each 432 × 485 µm) into a 1052 µm wide core area.
Every placement I tried , side-by-side, 2×2 cluster, top-and-bottom , staggered left right , hit routing congestion. The SRAM blocks consumed 82% of the die width when placed in parallel.

However latter suggestion's from **Leo Moser** and @Mike Bell helped me fix it .

Some bugs only showed up in gate-level simulation: the ICG (integrated clock gate) would deadlock on power-up because flip-flops initialize to random values in silicon, gating the clock before the core could reset.

Freedom to use your own design work (like in a University spin-out)

ETH zürich

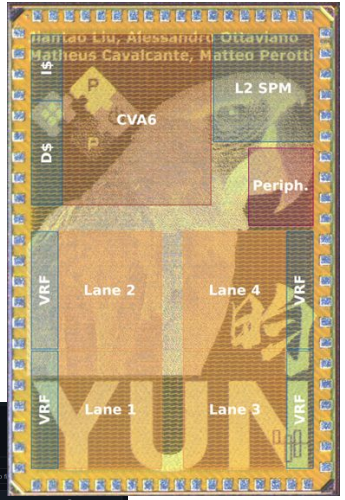
RISC-V Silicon at Scale in Academia:

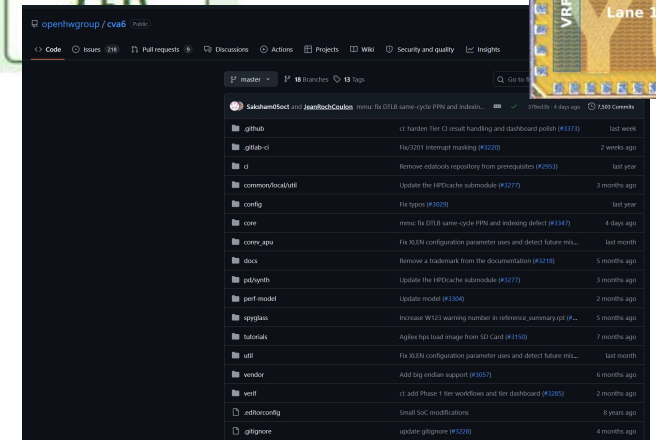
Designing "BIG" Open-Source Chips on

Yichao Zhang[1], Frank K. Gürkaynak[1], Lorenzo Leone[1], Angelo Garofalo[2], and Luca Benini[1,2]

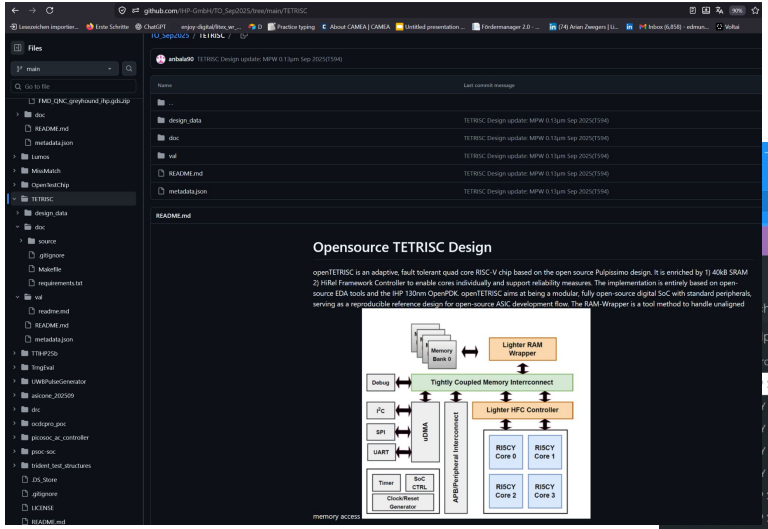
[1]Integrated Systems Laboratory, ETH Zurich
[2]Department of Electrical, Electronic, and Information Engineering, University of Bologna

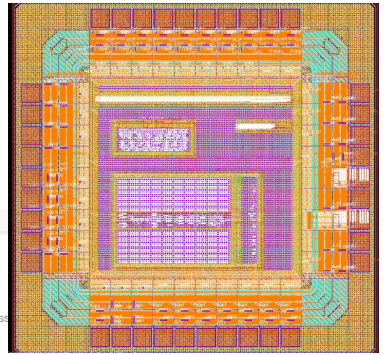
70 +	down to 7nm	up to 432	1 Billion +
Chip Tapeouts	Advanced Node	RISC-V Cores	Transistors

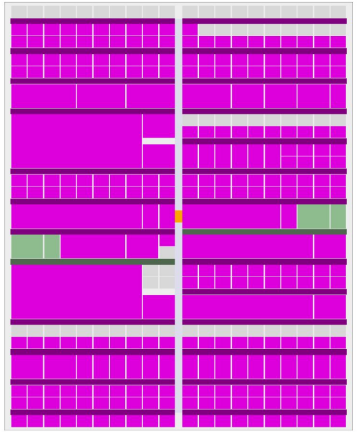




Freedom to show-off your design experience

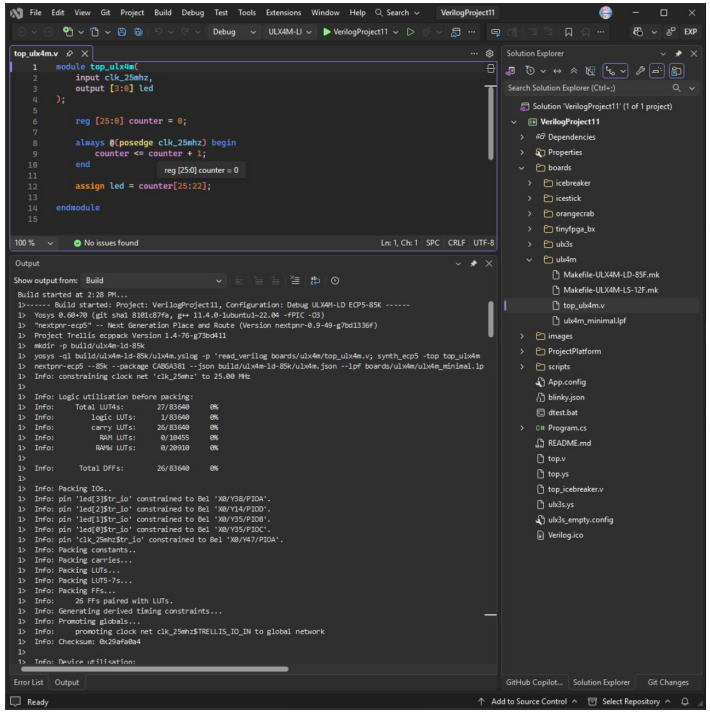


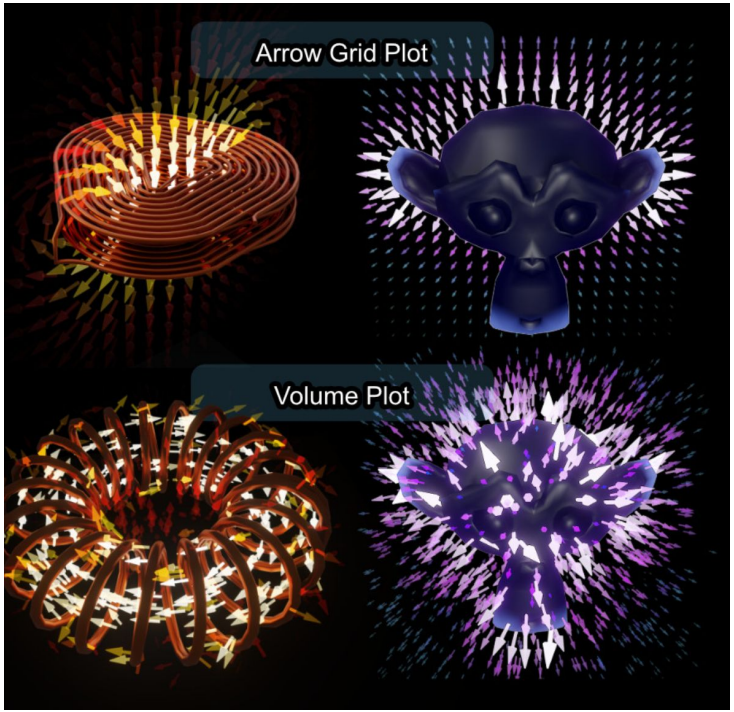




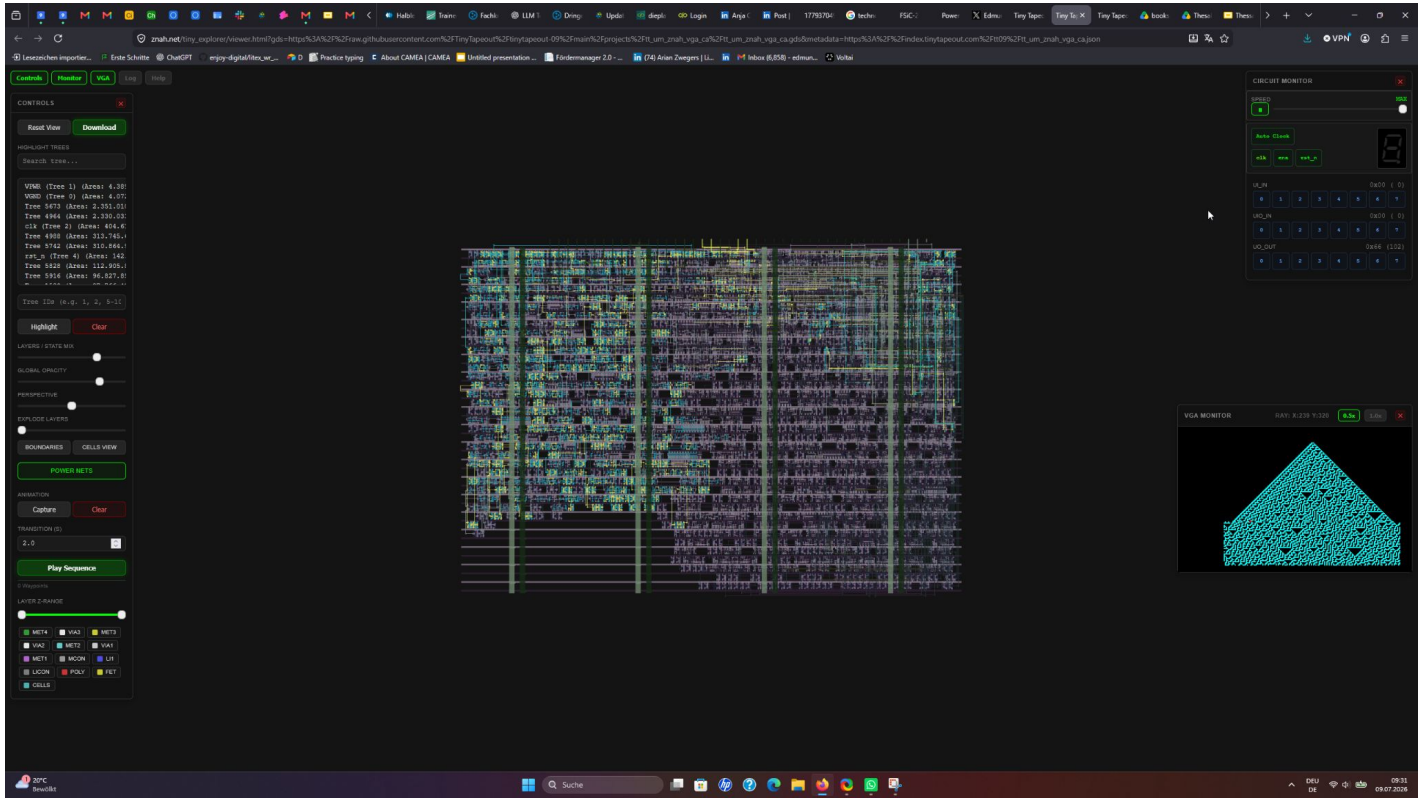
Freedom to innovate and integrate:

Visual Studio as IDE for FPGA, including bitstream generation,
Blender as a EMsimulation studio





Freedom to innovate and integrate



Freedom to innovate and integrate

Agentic AI

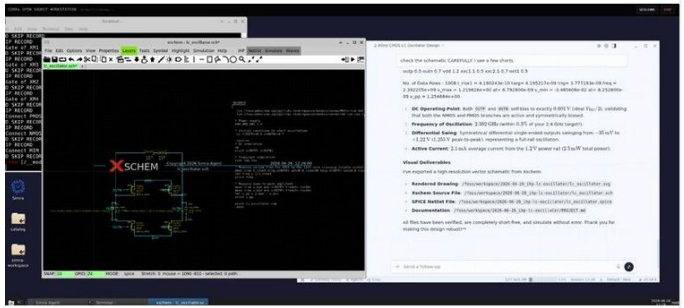
Holger Nießner reposted this

Harald Pretl • 2nd
Professor, IC designer, researcher, educator.
2w •

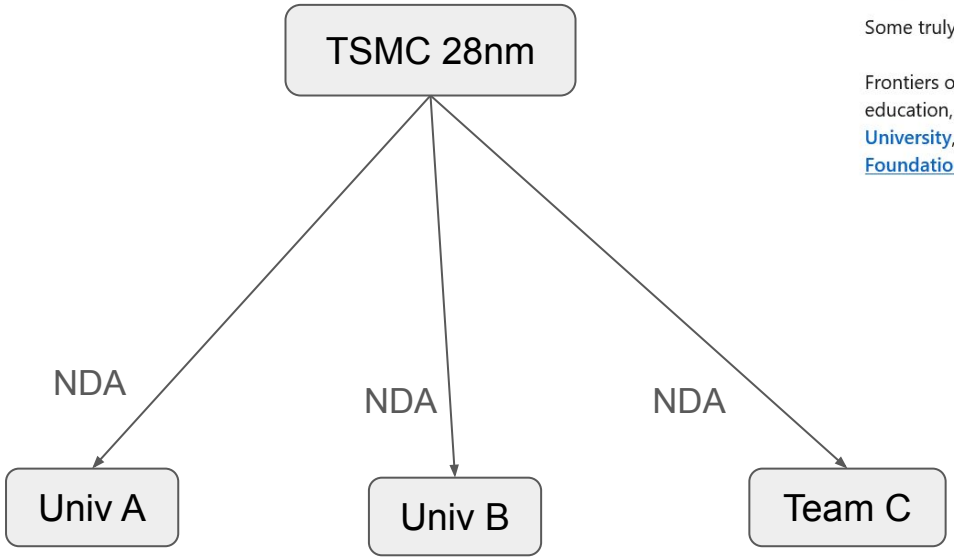
+ Follow

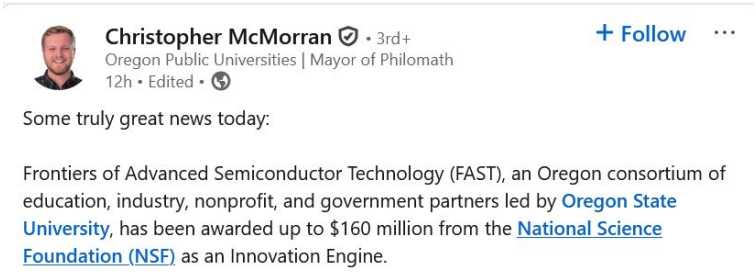
I think I looked into the future of EDA for chip design. Dr. Amir Mabhout gave my team early access to https://www.simratech.com, and I just spent some time with it. From a simple text prompt like "We use the IHP PDK. Build a simple CMOS LC oscillator for a frequency of 2.4GHz. Design it in Xschem, and we want to use ngspice for simulation. The simulation should cover DC and TRAN." I got a working (although super basic) Xschem schematic and a running simulation.

Sure, the schematic is very simplistic and far from perfect, but I guess it hints at the future, and I can further prompt it to get exactly what I want. BTW, SimraTech is using our IIC-OSIC-TOOLS image. 😀

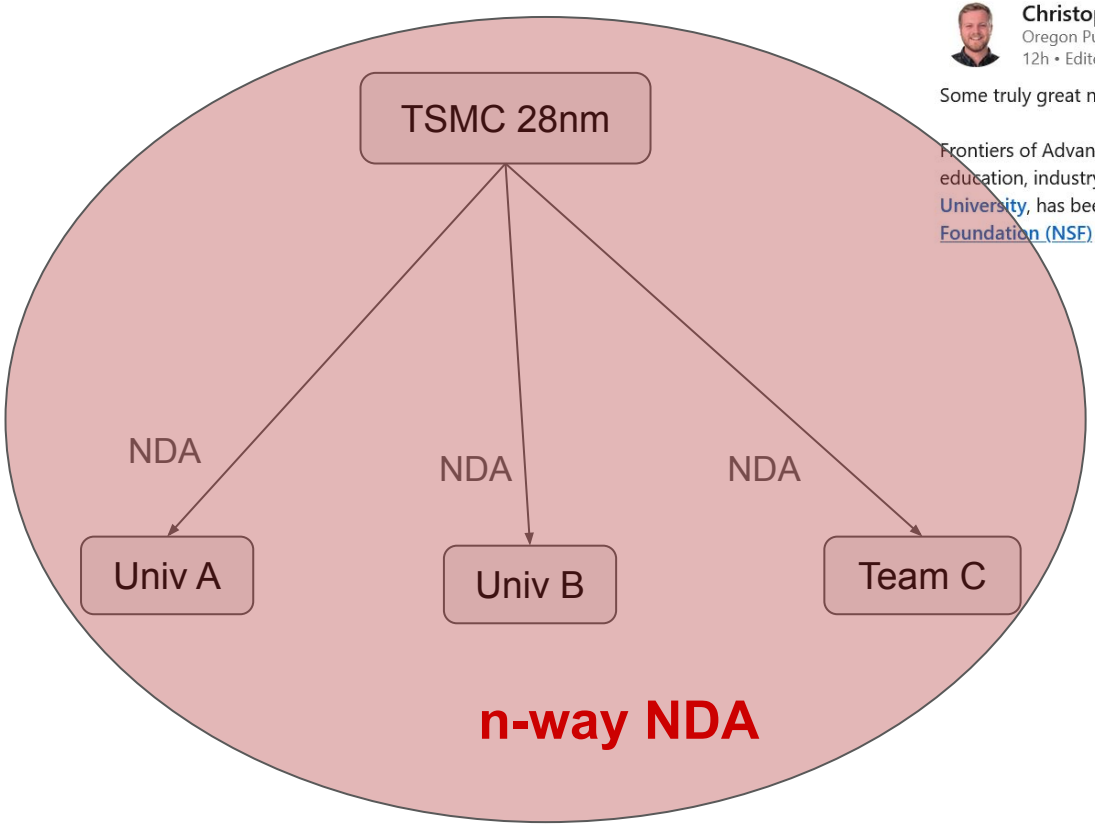


Freedom to collaborate





Freedom to collaborate



Christopher McMorran • 3rd+
Oregon Public Universities | Mayor of Philomath
12h • Edited •

+ Follow ···

Some truly great news today:

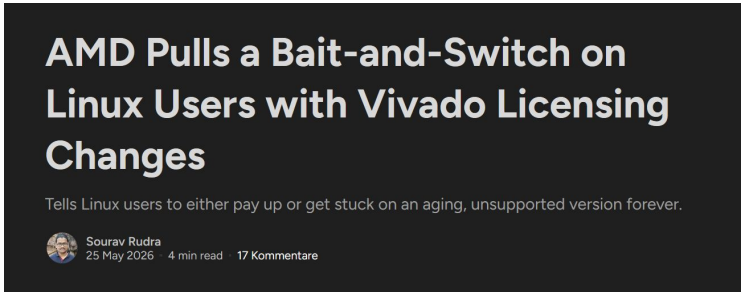
Frontiers of Advanced Semiconductor Technology (FAST), an Oregon consortium of education, industry, nonprofit, and government partners led by Oregon State University, has been awarded up to $160 million from the National Science Foundation (NSF) as an Innovation Engine.

Reproducible design environment, long-term accessibility

Look at your own “chip design” from 15 years ago? Your PhD work?

Is that old installation still working with the current license server?
Do you have still have a valid license for that old installation image?

Collaborate with other research institutions
which uses a different set of tool versions?



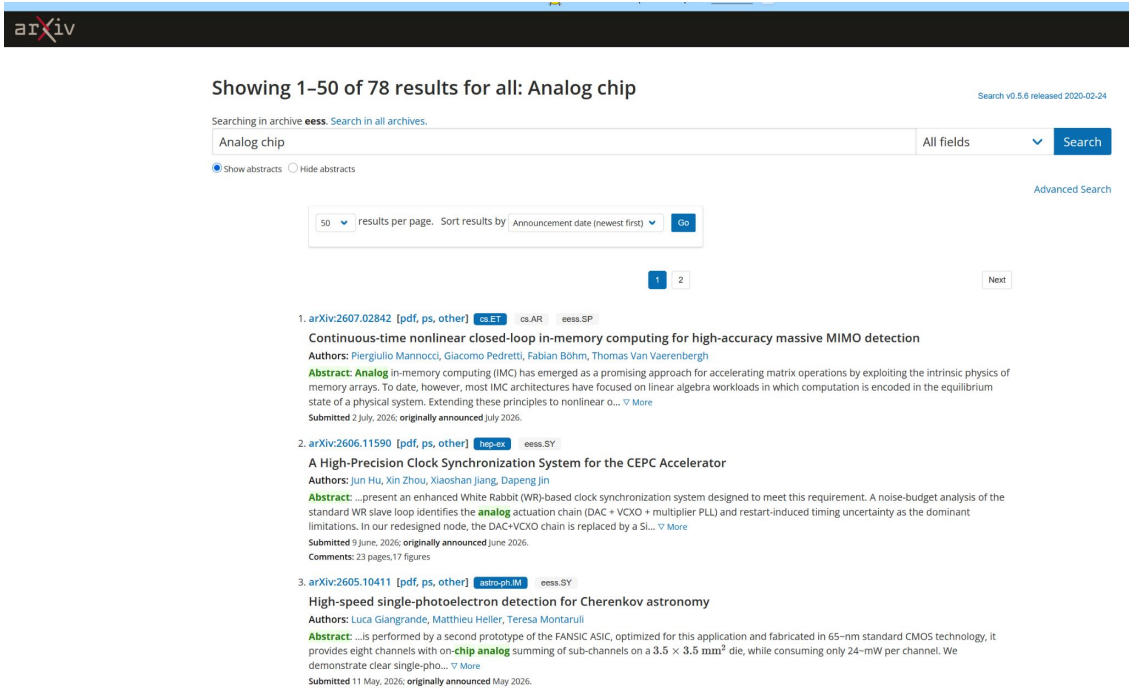
Freedom to explore

Ilia Greenblat • 1st
freelance VLSI Designer
1w •

I used to call my tools - Poor man's EDA. Teams with unlimited budgets don't need to read any further. Recenty I changed my mind, now i call them: Thrifty startup flows. Because the idea is to do full chip development with Coffee (and Falafel) being the largest budget item and do it from MaMad (not even the Parking space). We are not there yet. Open source synthesis, Place & Route and many other must-use tools in ASIC development are not production tapeout quality.
Having said that, using free tools can advance Your project to be Cadence/Synopsys ready, where the expensive license usage becomes minimal.
Simulation, Verification, CDC, LINT, Coverage - all can be served with free open source.

Transparency and inspectability

Do you publish research results or marketing material?



the present of open-source chip design tools

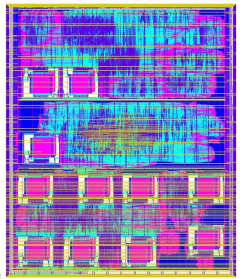
The release of open Process Design Kits in 2020 has changed this landscape by enabling public access to manufacturable semiconductor technologies.

SkyWater Sky130A
GlobalFoundries gf180mcuD
IHP-SG13G2

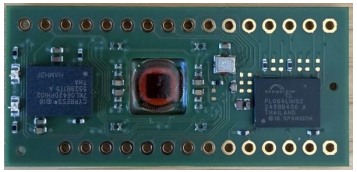
Initiatives such as Efabless, ChipFoundry, Tiny Tapeout, IEEE PICO, UNIC-CASS,ChipPractice, and the IEEE Open Silicon Initiative have connected open design infrastructure with training, mentoring, community participation, and tape-out opportunities.

What can you design today with open source EDA tool today?

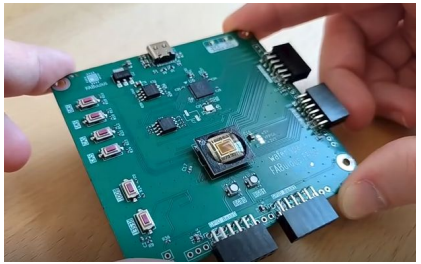
RISC-V SoC
SKY130 10mm²



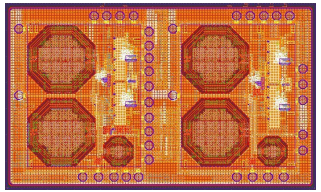
Zephyr SoC
HyperRAM, Flash in XIP mode.
GPIO, UART, I2C, SPI, programmable I/Os



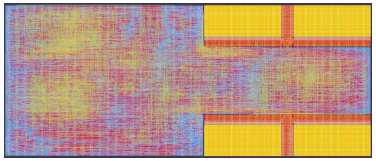
FPGA
GF 180nm 500 LUT



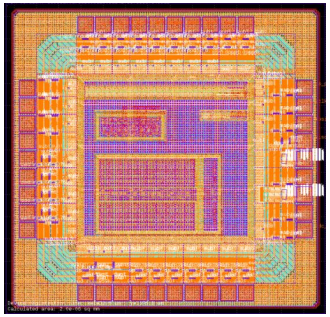
RF circuits
Programmable Phase
Low Noise Amplifier
IHP 130nm BiCMOS

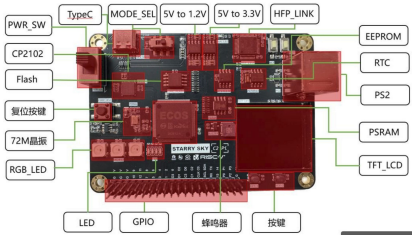


Linux capable SoC
IHP130 BiCMOS



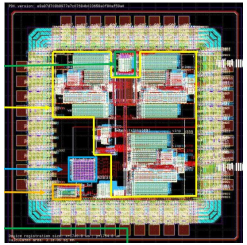
mixed signal circuits
ADC with SPI





PicoRV32
55nm

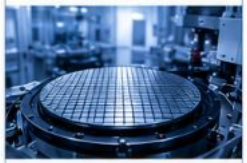
mixed signal circuits
programmable INA
IHP 130nm BiCMOS



What can you design with open source EDA tool today?

1. LOGIC FABS

Manufacture processors and logic chips used in computing and AI applications.



TECHNOLOGY NODES

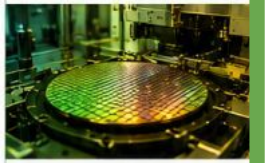
2nm / 3nm / 5nm / 7nm / 14nm and beyond

APPLICATIONS

- CPUs, GPUs, AI chips
- Smartphones
- PCs & Laptops
- Data Centers
- Networking

2. MEMORY FABS

Produce memory chips like DRAM and NAND that store the world's data.



TYPES

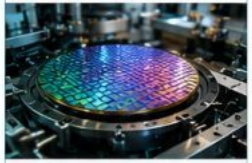
DRAM (Volatile)
NAND Flash (Non-Volatile)

APPLICATIONS

- Smartphones
- Servers & Data Centers
- SSDs
- AI Systems

4. ANALOG & MIXED-SIGNAL FABS

Design and manufacture chips that interface with the real world.



WHAT THEY MAKE

Power management ICs, Data converters, Amplifiers, Interface ICs, Sensors

APPLICATIONS

- Power Management
- Sensors
- Audio / Video
- Industrial Automation
- Medical Devices

5. POWER SEMICONDUCTOR FABS

Manufacture devices that control and convert electrical power.

KEY DEVICES

MOSFETs, IGBTs, Diodes, Thyristors, Power ICs

APPLICATIONS

- Electric Vehicles
- Solar Inverters
- Charging Stations
- Power Supplies
- Industrial Drives
- Grid Infrastructure

7. MEMS FABS

Create microscopic mechanical structures on silicon.

PRODUCTS

Accelerometers, Gyroscopes, Pressure Sensors, Microphones, Micro Mirrors, RF MEMS

APPLICATIONS

- Smartphones
- Wearables
- Automotive (ADAS)
- Drones
- Industrial Sensors

8. PHOTONICS FABS

Manufacture chips that manipulate light for communication and sensing.

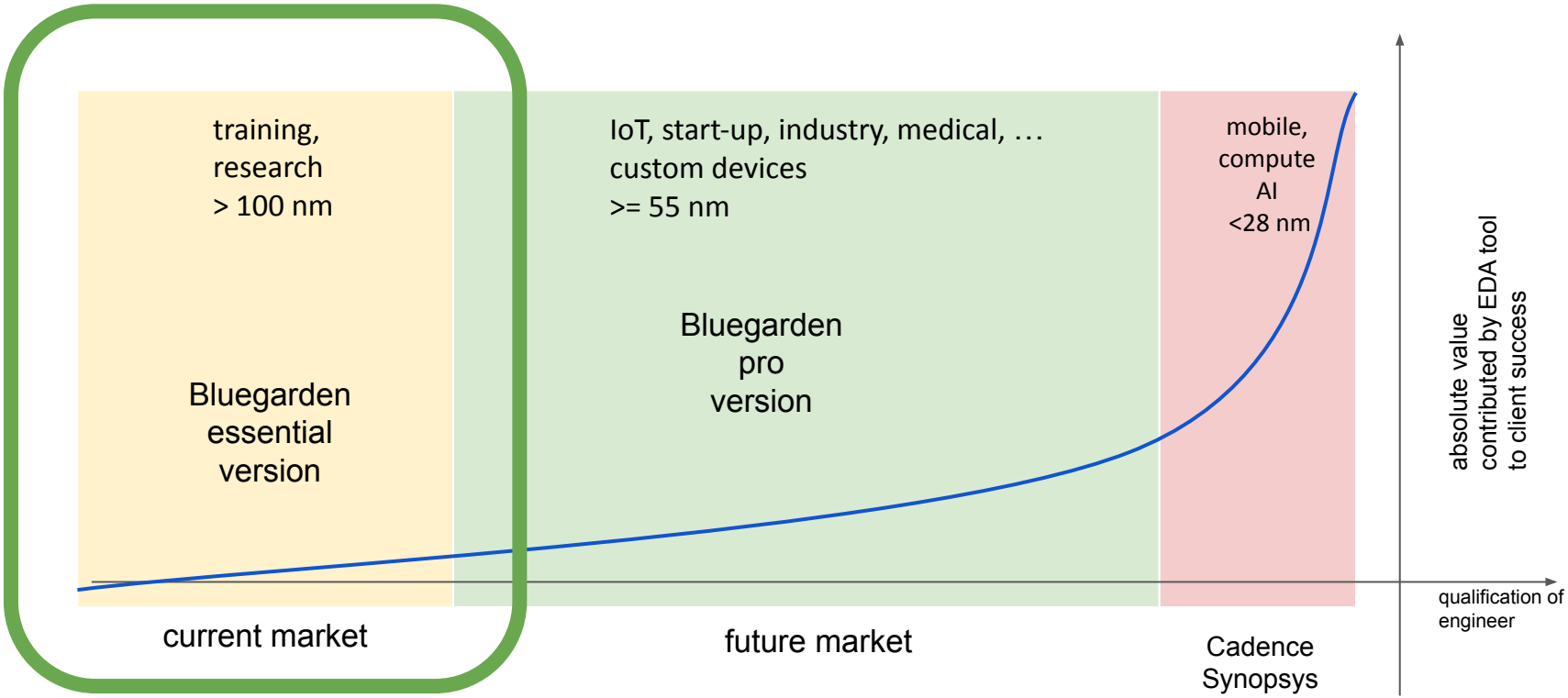
KEY PRODUCTS

Optical Transceivers, Silicon Photonics, Lasers, Modulators, Detectors, Waveguides

APPLICATIONS

- Optical Communication
- AI Data Centers
- Quantum Technologies
- LiDAR & Sensing
- High-Speed Interconnects

Tools for application domain experts using mature nodes



the future use of open-source chip design tools

Practical chip design requires

- reproducible toolchains
- maintained environments
- workflow integration
- verification infrastructure
- user support
- test and validation infrastructure
- …

Managed open-source design environments
toward a more practical ecosystem for education,
prototyping, and early-stage semiconductor development.

how to deploy open source EDA tools

github action driven pipeline Tiny Tapeout	Cloud based chip design generator Chipflow Chipinventor	popular pre-built docker images IIC-OSIC_Tools	managed custom docker images deployed in the cloud Symbiotic EDA	managed custom docker images deployed on workstation Symbiotic EDA	self install OpenROAD
ease of use very low barrier of entry	commercial supported pre-tested dependable	large community free of cost	commercial supported flexible on tools pre-tested	commercial supported flexible on tools pre-tested	flexibility autonomy
basic function inflexible	fixed design flow, tools and processes depending on cloud provider lock-in cost	predetermined tool selection and versions and timeline	depending on external cloud provider high latency security cost	cost	requires a wide spectrum of own expertise own effort

how to deploy open source EDA tools

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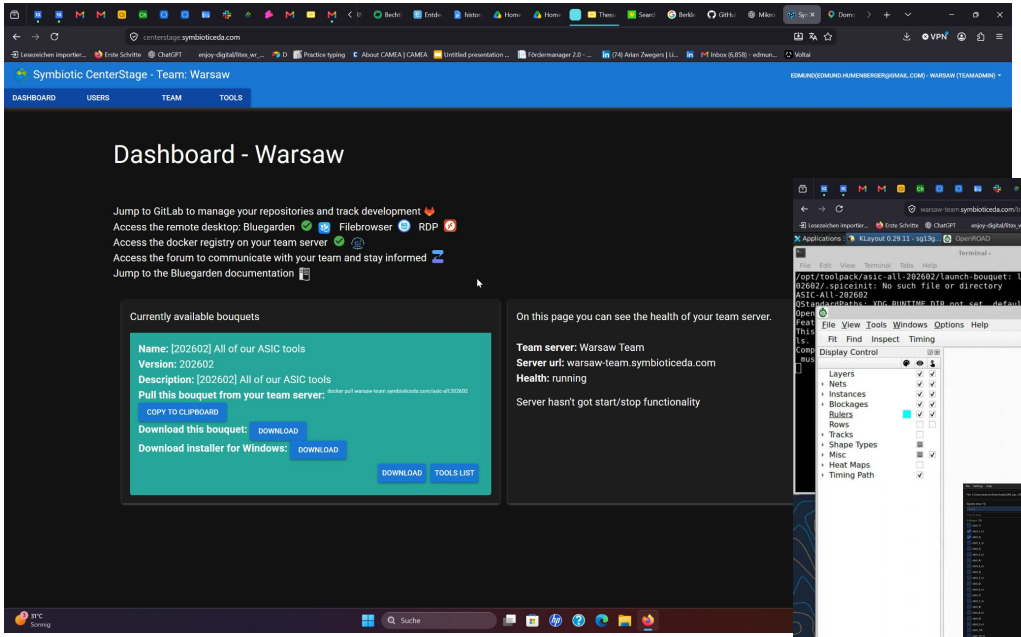
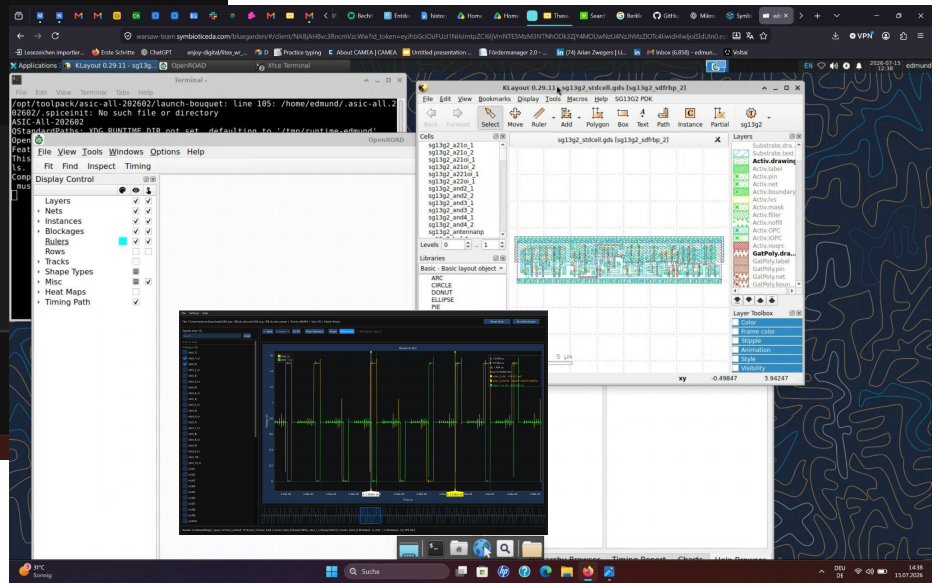
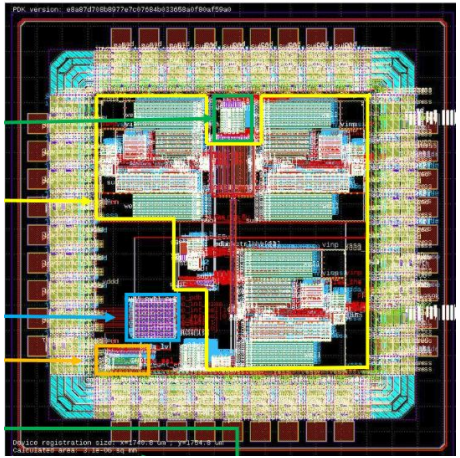
Open source EDA can deliver an environment for experimental and commercial EDA tools





Accelerated innovation though open collaboration



Acknowledgements

- It took help from a lot of people to get this project over the line!
- Special thanks to the following:
  - Nlnet for funding the project
  - Alonso for doing such a great job implementing / verifying the digital
  - Iulian Oancea for providing layout guidance and developing the char board
  - Herman Krzysztof for performing regular pre-fab checks on blocks throughout the layout process
  - Roel Jordans for allowing us to use his level shifter IP
  - Stefan Schippers for creating xschem and for updating it according to the demands of this project
  - Holger Vogt / Dietmar Warning for developing ngspice and for addressing various queries I had throughout this project
  - Martin Köhler for creating the align plugin for klayout (and also the move quickly / pad plugins)
  - Yacine Sotehi for fixing the IHP density checker script and implementing the power via insertion script
  - Harald Pretl for introducing us to SERMA
  - Tim Edwards for managing magic, updating it according to the demands of this project and for doing such a great job on the IHP pycells for magic
  - In addition, thanks to Tim for answering my questions which were approximately 3 per day since the beginning of this project! I'm sure I drove him nuts but he always gave an impactful answer to solve my issues

BlueGarden delivers convenience and freedom … now

long term dependable, reliable,
Docker-based engineering environment for

- Education
- Research
- professional design work

… in a scalable way at an affordable price.

Symbiotic EDA

edmund@symbioticeda.com