TWINRELECT

Efficient Capacitance Extraction for Accurate STA- based reliability Analysis

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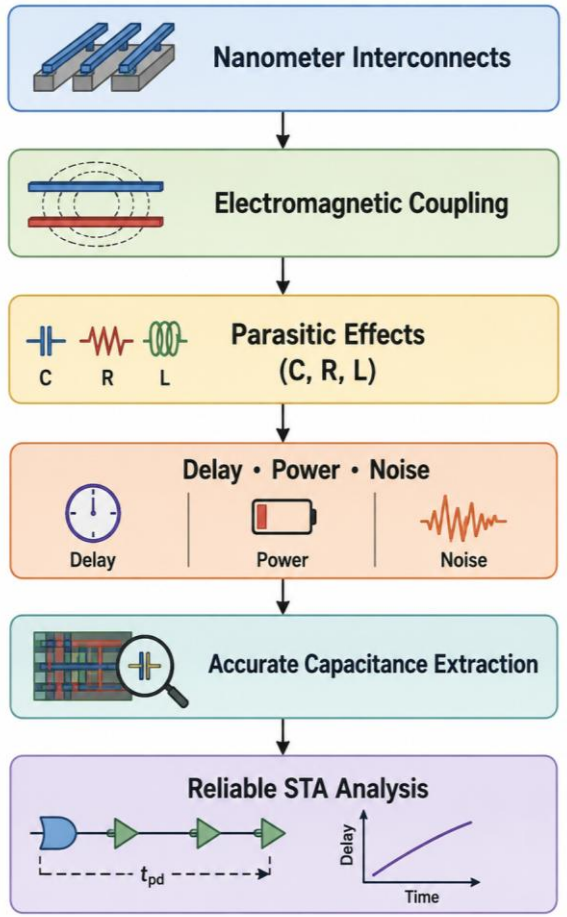
Motivation / Background

- Modern VLSI technology uses very small nanometer-scale interconnects making wires non-ideal.
- Electromagnetic coupling between adjacent wires introduces parasitic effects:

  Capacitance (C), Resistance (R), and Inductance (L).
- These parasitic effects impact circuit performance by increasing:
  - Signal delay
  - Power consumption
  - Signal distortion
  - Reliability problems
- Parasitic extraction is performed after layout and before simulation to accurately model the interconnect parasitics before circuit simulation.
- Among all parasitics effects, Capacitance is the dominant factor, significantly affecting:

  Speed, Signal Integrity.
- Accurate capacitance extraction is essential for reliable digital, analog, and mixed-signal IC design.



Field Solvers :

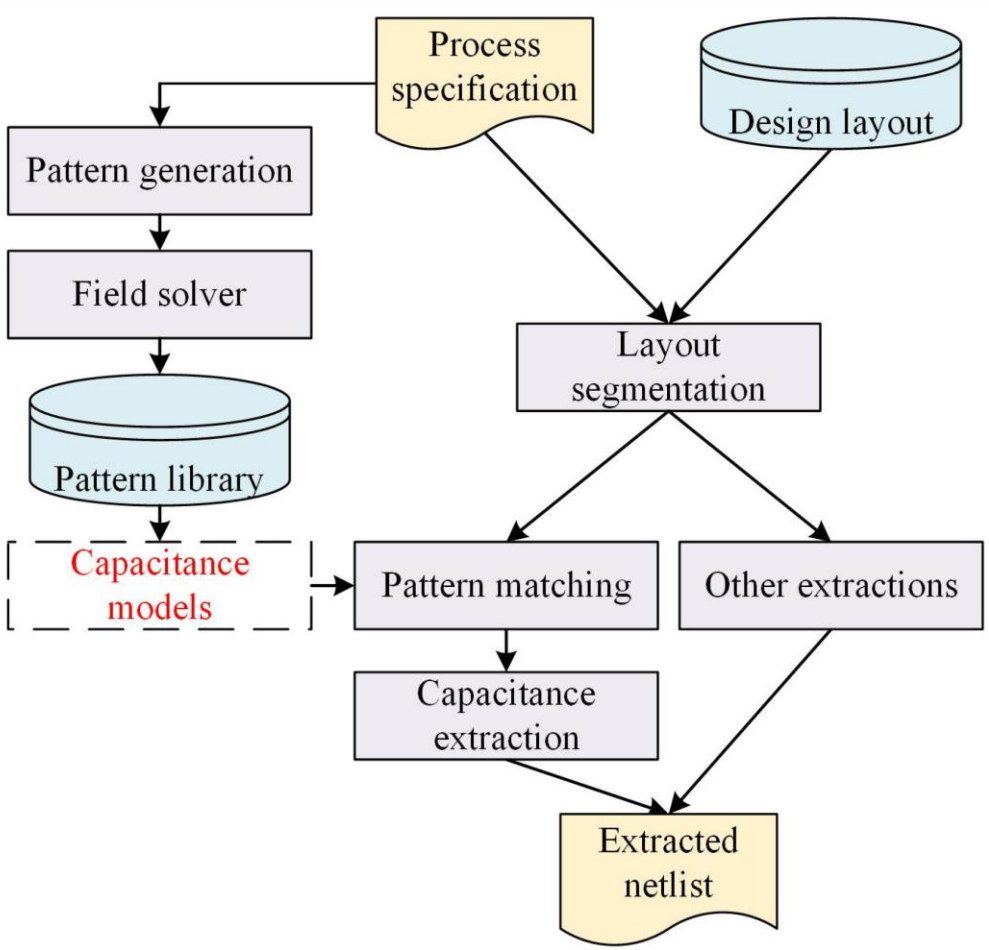
- To model these parasitic effects, VLSI tools use Field Solvers.
- Compute the electric and magnetic fields for interconnects.
- Field Solvers numerically solve **Maxwell's equations** to model
  - Electric Fields (Capacitance Extraction)
  - Magnetic Fields (Inductance Extraction)
  - Current Distributions (Resistance Extraction)

- Correlation with Parasitic Extraction
  - Parasitic Extraction tools **rely on Field Solvers** to compute the capacitance matrices for layout geometries
  - **Accuracy of extraction** depends on how well the solver handles:
    - Coupling between adjacent wires
    - Substrate effects (capacitance to ground planes)
    - Scaling trends (changes in parasitics with smaller process nodes)

Types of Field Solver

- Directly applying 3-D capacitance field solver to the design is more demanded.

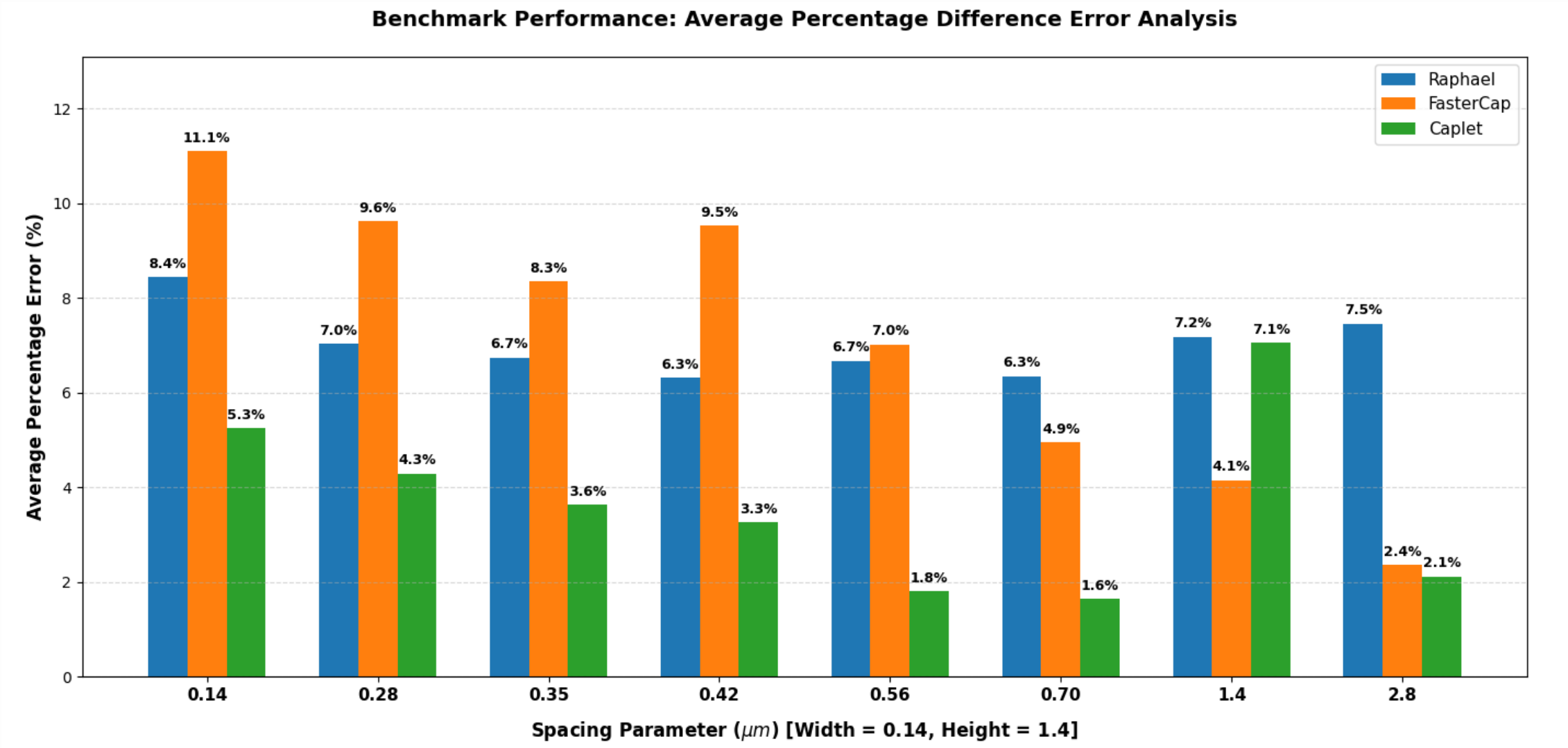
- Finite Difference / Finite Element Method **AX = b**
  - Stable, Versatile; slow
- Boundary Element Method (BEM) **XACT3D, Q3D, Act3D, Caplet, FastCap, QBEM / HBBEM**
  - Fast, handle complex geometry
  - Not Scalable; discretization quality affects accuracy
- Floating Random Walk Method (FRW) **QuickCap / Rapid3D, RWCap**
  - No discretization of problem domain (stable accuracy)
  - Suitable for large problem (low memory cost);scalability
  - Easy for Parallelization, Stochastic error; controllable
  - Restriction on geometry



Proposed Methodology: MATLAB BEM

- **Problem Statement** – Why existing methods are insufficient.
- **Proposed Method** – Developed a custom Boundary Element Method (BEM) solver
- Designed to handle complex multi-conductor geometries with high accuracy.
- **Implementation** – MATLAB solver architecture.
- **Comparison** – Verified against industrial tool "**Gold Standards**" like Raphael.
- Extensive benchmarking conducted against **Faster-Cap and CAPLET** for cross-validation.
- Focused on balancing extraction speed with sign-off quality precision.

Experimental Results

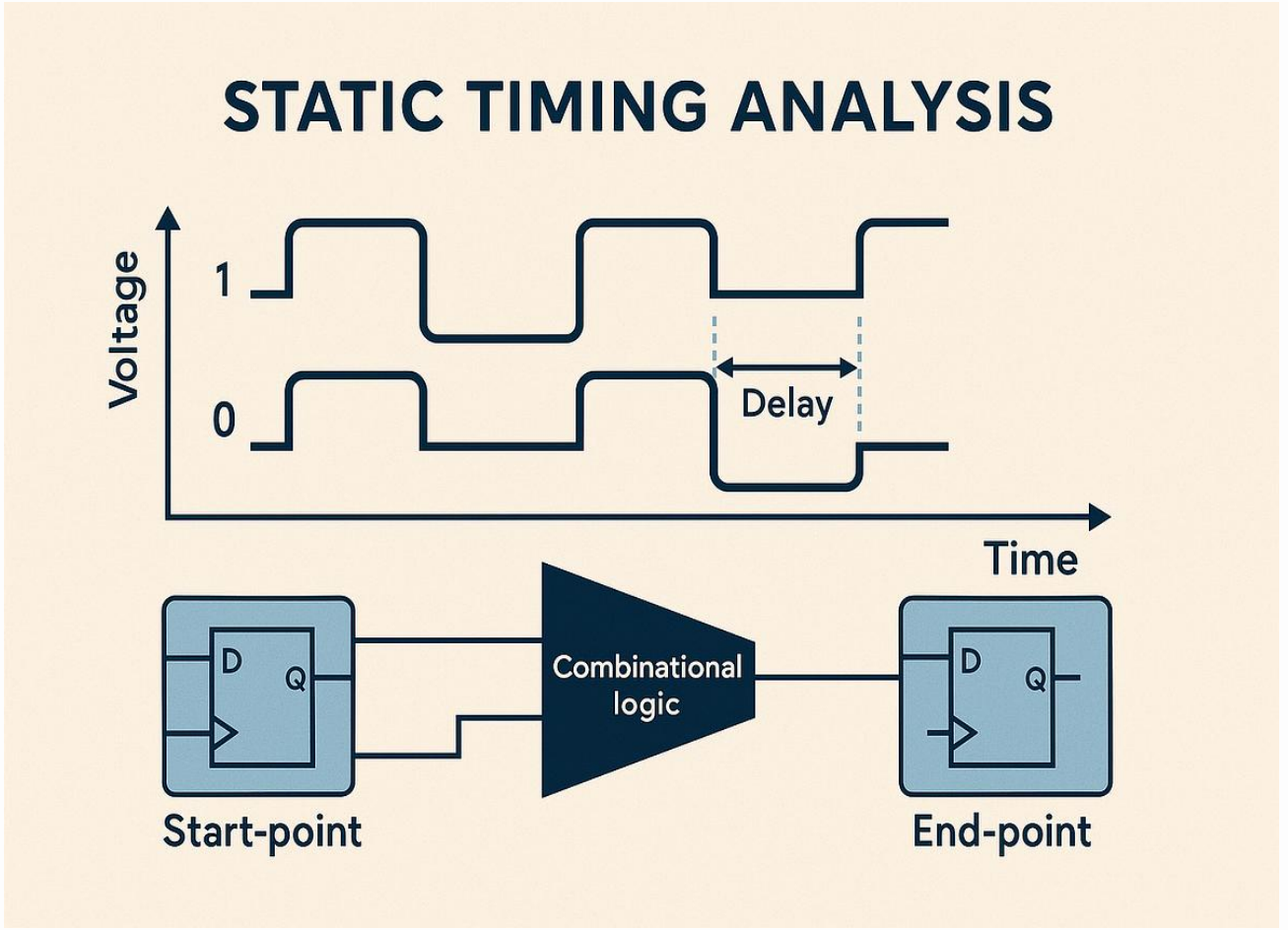


Discussion

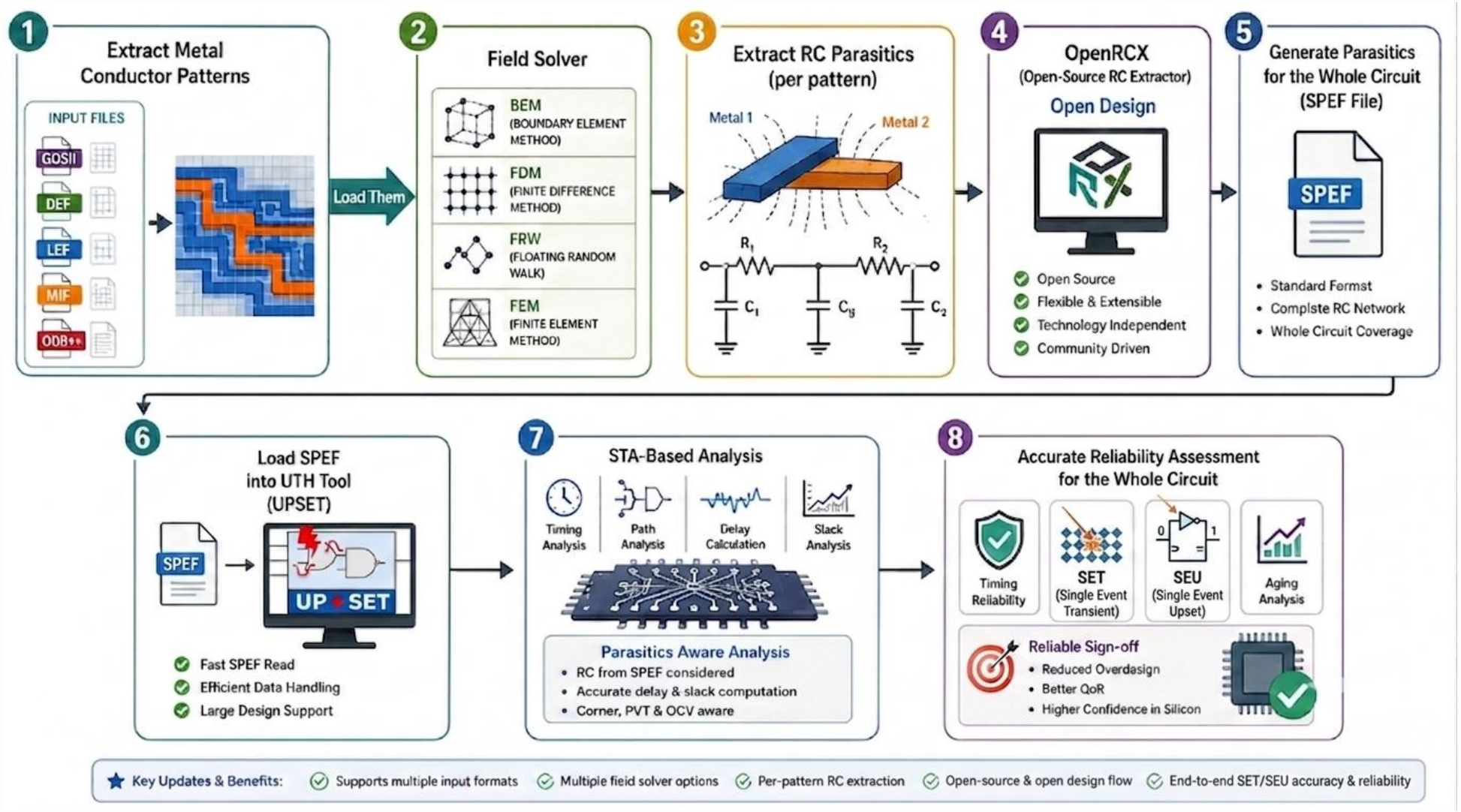
- Achieved the lowest Mean Relative Frobenius error (2.743e-02) across all benchmark cases, indicating the closest agreement with the Raphael reference solver.
- Highest mean cosine similarity was obtained by Faster-Cap (0.99992) and the highest Pearson correlation by Faster-Cap (0.99993).
- The lowest mean RMSE was recorded by Proposed method (8.993e-13 F) and the lowest mean MAE by Faster-Cap (6.088e-13 F).
- Overall ranking by mean Relative Frobenius error (lower is better): Proposed (2.743e-02) > Faster-Cap (2.818e-02) > CAPLET (5.020e-02).
- All comparison solvers reproduce the Raphael capacitance matrices to within a small fraction of the reference Frobenius norm, with cosine and Pearson values essentially equal to unity, confirming that the differences are confined to the third significant figure of the individual matrix entries.

Accurate Static Time Analysis

- Verifies whether a digital circuit meets its timing requirements **without input-vector simulation**.
- A **critical step** in ASIC and FPGA design flows.
- Checks timing constraints including **setup, hold, recovery, and removal** across all **Process, Voltage, and Temperature (PVT)** corners.
- **Accurate parasitic extraction** (R, C, and optionally L) enables more precise timing analysis and improves sign-off confidence.



SUMMARY


1
Extract Metal Conductor Patterns
INPUT FILES
GDSII
DEF
LEF
MIF
ODB++
Load Them
2
Field Solver
BEM (BOUNDARY ELEMENT METHOD)
FDM (FINITE DIFFERENCE METHOD)
FRW (FLOATING RANDOM WALK)
FEM (FINITE ELEMENT METHOD)
3
Extract RC Parasitics (per pattern)
Metal 1
Metal 2
R1
R2
C1
C12
C2
4
OpenRCX
(Open-Source RC Extractor)
Open Design
Open Source
Flexible & Extensible
Technology Independent
Community Driven
5
Generate Parasitics for the Whole Circuit (SPEF File)
SPEF
Standard Formst
Complste RC Network
Whole Circuit Coverage
6
Load SPEF into UTH Tool (UPSET)
SPEF
UP SET
Fast SPEF Read
Efficient Data Handling
Large Design Support
7
STA-Based Analysis
Timing Analysis
Path Analysis
Delay Calculation
Slack Analysis
Parasitics Aware Analysis
RC from SPEF considered
Accurate delay & slack computation
Corner, PVT & OCV aware
8
Accurate Reliability Assessment for the Whole Circuit
Timing Reliability
SET (Single Event Transient)
SEU (Single Event Upset)
Aging Analysis
Reliable Sign-off
Reduced Overdesign
Better QoR
Higher Confidence in Silicon
Key Updates & Benefits:
Supports multiple input formats
Multiple fieid solver options
Per-pattern RC extraction
Open-source & open design flow
End-to-end SET/SEU accuracy & reliability

Conclusion

- Efficient capacitance extraction improve accuracy and run time.
- (STA + Parasitic) where capacitance enters the time flow.
- Interconnects introduce capacitance (wire to ground coupling) that affects signals delay and transition time.
- Accurate data leads to precise STA and better silicon correlation.
- Inaccurate extraction leads to wrong delay, STA violations and reliability risks.
- Enable confident reliability analysis and tape-out.
- Capacitance extraction is essential for accurate STA.